

Si4412DY*

Single N-Channel Logic Level PowerTrench® MOSFET

General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

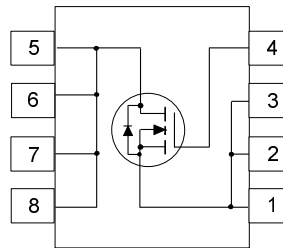
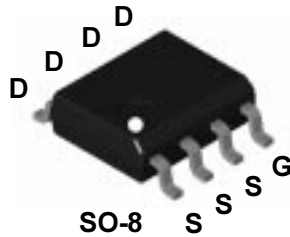
This device is well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Applications

- Battery switch
- Load switch
- Motor controls

Features

- 7 A, 30 V. $R_{DS(ON)} = 0.028 \Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 0.042 \Omega @ V_{GS} = 4.5 \text{ V}$
- Low gate charge.
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(ON)}$.
- High power and current handling capability.



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|-----------------------------------|--|-------------|-------|
| V _{DSS} | Drain-Source Voltage | 30 | V |
| V _{GSS} | Gate-Source Voltage | ±20 | V |
| I _D | Drain Current - Continuous (Note 1a) - Pulsed | 7.0 | A |
| | | 30 | |
| P _D | Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c) | 2.5 | W |
| | | 1.2 | |
| | | 1 | |
| T _J , T _{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | °C |

Thermal Characteristics

| | | | |
|------------------|---|----|------|
| R _{θJA} | Thermal Resistance, Junction-to-Ambient (Note 1a) | 50 | °C/W |
| R _{θJC} | Thermal Resistance, Junction-to-Case (Note 1) | 25 | °C/W |

Package Outlines and Ordering Information

| Device Marking | Device | Reel Size | Tape Width | Quantity |
|----------------|----------|-----------|------------|------------|
| 4412 | SI4412DY | 13" | 12mm | 2500 units |

* Die and manufacturing source subject to change without prior notification.

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------------------------------------|---|--|-----|-----|---------|----------------------|
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\ \mu\text{A}$, Referenced to 25°C | | 26 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$ | | | 2 25 | μA |
| I_{GSSF} | Gate-Body Leakage Current, Forward | $V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$ | | | 100 | nA |
| I_{GSSR} | Gate-Body Leakage Current, Reverse | $V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$ | | | -100 | nA |

On Characteristics (Note 2)

| | | | | | | |
|--|--|--|----|-------------------------|-------------------------|----------------------|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ | 1 | | | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D = 250\ \mu\text{A}$, Referenced to 25°C | | -4.3 | | mV/ $^\circ\text{C}$ |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS} = 10\text{ V}, I_D = 7\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 7\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 3.5\text{ A}$ | | 0.011 0.027 0.026 | 0.028 0.037 0.042 | Ω |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$ | 30 | | | A |
| g_{FS} | Forward Transconductance | $V_{DS} = 15\text{ V}, I_D = 7\text{ A}$ | | 19 | | S |

Dynamic Characteristics

| | | | | | | |
|------------|------------------------------|--|--|-----|--|----|
| C_{iss} | Input Capacitance | $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$ | | 830 | | pF |
| C_{oss} | Output Capacitance | | | 185 | | pF |
| C_{riss} | Reverse Transfer Capacitance | | | 80 | | pF |

Switching Characteristics (Note 2)

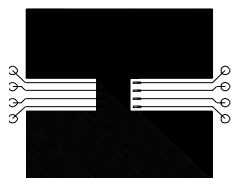
| | | | | | | |
|--------------|------------------------------------|---|--|-----|----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 25\text{ V}, I_D = 1\text{ A}, R_L = 25\ \Omega$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$ | | | 15 | ns |
| t_r | Turn-On Rise Time | | | | 20 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | | 55 | ns |
| t_f | Turn-Off Fall Time | | | | 28 | ns |
| t_{rr} | Drain-Source Reverse Recovery Time | $I_F = 2.0\text{ A}, di/dt = 100\text{A}/\mu\text{s}$ | | | 80 | nS |
| Q_g | Total Gate Charge | $V_{DS} = 15\text{ V}, I_D = 2\text{ A},$ $V_{GS} = 10\text{ V}$ | | 15 | 29 | nC |
| Q_{gs} | Gate-Source Charge | | | 2.8 | | nC |
| Q_{gd} | Gate-Drain Charge | | | 3.1 | | nC |

Drain-Source Diode Characteristics and Maximum Ratings

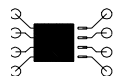
| | | | | | | |
|----------|---|--|--|------|-----|---|
| I_S | Maximum Continuous Drain-Source Diode Forward Current | | | 2.3 | | A |
| V_{SD} | Drain-Source Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = 2.0\text{ A}$ (Note 2) | | 0.75 | 1.1 | V |

Notes:

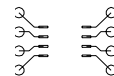
1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in^2 pad of 2 oz. copper.



b) 105°C/W when mounted on a 0.04 in^2 pad of 2 oz. copper.



c) 125°C/W on a minimum mounting pad.

Scale 1 : 1 on letter size paper

2: Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

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|--------------------------|------------------------|---|
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