

N-Channel 30-V (D-S) Fast Switching WFET®

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.0095 @ $V_{GS} = 10$ V	15
	0.0135 @ $V_{GS} = 4.5$ V	13

FEATURES

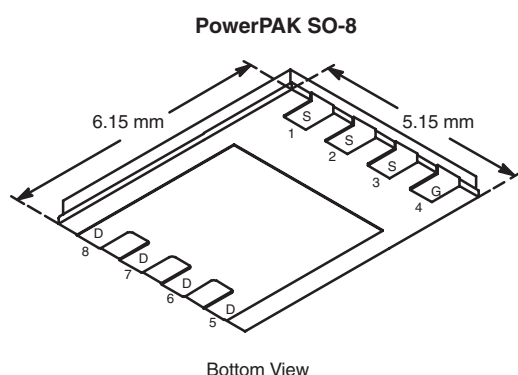
- Extremely Low Qgd WFET Technology for Low Switching Losses
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- 100 % R_g Tested



Available
RoHS*
COMPLIANT

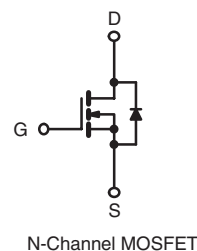
APPLICATIONS

- High-Side DC/DC Conversion
 - Notebook
 - Server
 - Workstation
- Point-of-Load Conversion



Bottom View

Ordering Information: Si7390DP-T1
Si7390DP-T1—E3 (Lead (Pb)-Free)



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted				
Parameter		Symbol	10 secs	Steady State
Drain-Source Voltage		V_{DS}	30	
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	$T_A = 25^\circ\text{C}$	I_D	15	9
	$T_A = 70^\circ\text{C}$		12	7
Pulsed Drain Current		I_{DM}	± 50	
Continuous Source Current (Diode Conduction) ^a		I_S	4.1	1.5
Maximum Power Dissipation ^a	$T_A = 25^\circ\text{C}$	P_D	5	1.8
	$T_A = 70^\circ\text{C}$		3.2	1.1
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	
Soldering Recommendations (Peak Temperature) ^{b,c}			260	

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Typical	Maximum
Maximum Junction-to-Ambient (MOSFET) ^a	$t \leq 10$ sec	R_{thJA}	20	25
	Steady State		53	70
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.1	3.2

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

* Pb containing terminations are not RoHS compliant, exemptions may apply.

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

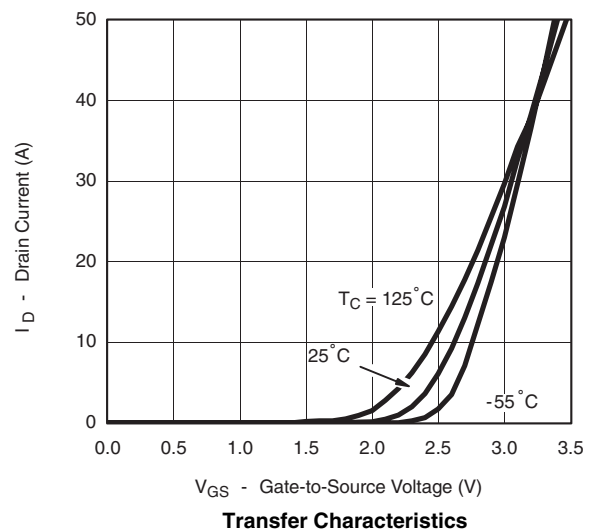
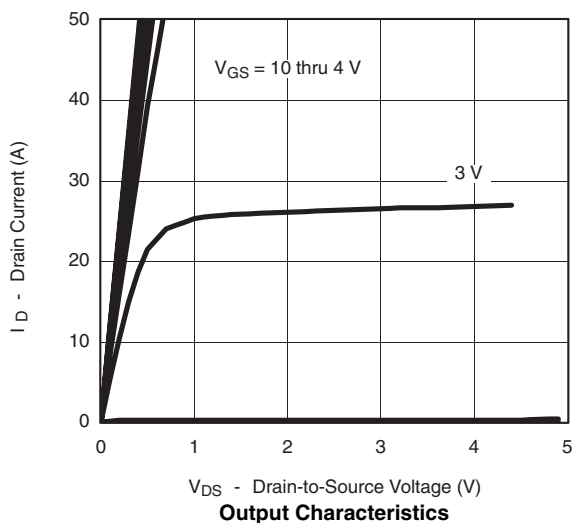
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	0.8		3.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 70^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	40			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 15\ \text{A}$		0.0075	0.0095	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 13\ \text{A}$		0.0105	0.0135	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 15\ \text{A}$		45		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 4.1\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.7	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 15\ \text{A}$		10	15	nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			2.1		
Gate Resistance	R_g		0.2	0.8	1.4	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}$, $R_L = 15\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		16	30	ns
Rise Time	t_r			7	12	
Turn-Off Delay Time	$t_{d(off)}$			43	70	
Fall Time	t_f			14	25	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.7\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		35	60	

Notes

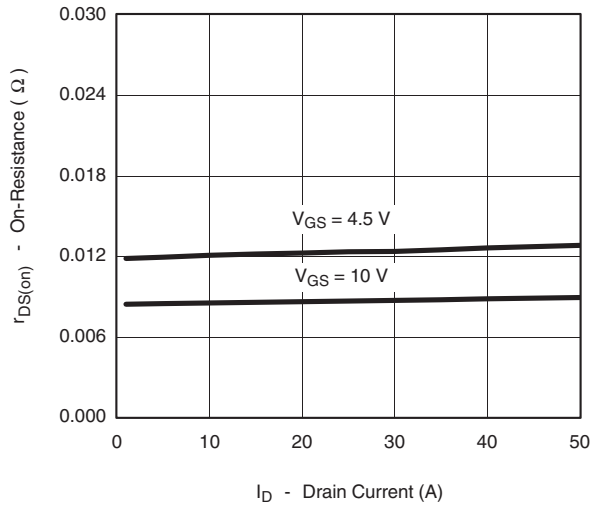
a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

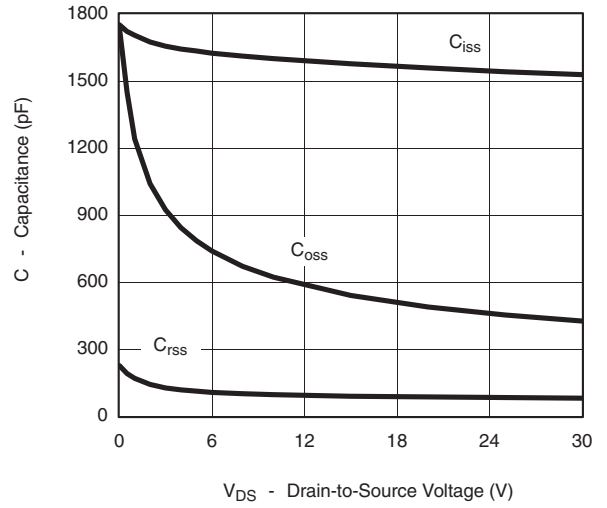
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25°C unless noted

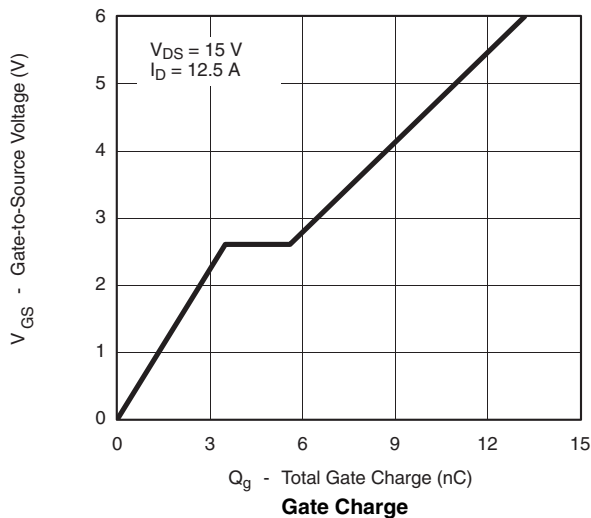
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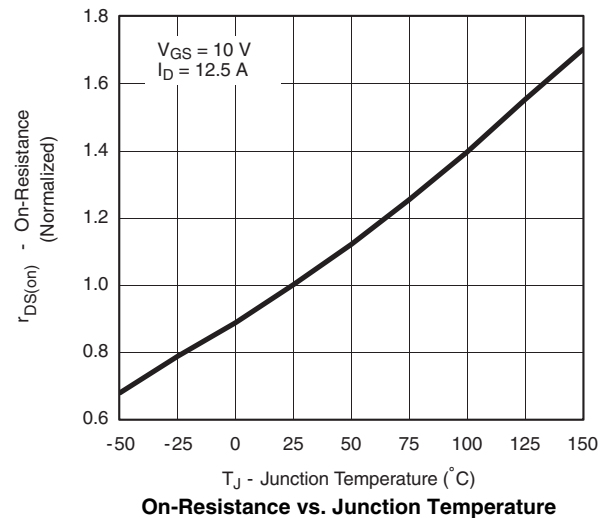
On-Resistance vs. Drain Current



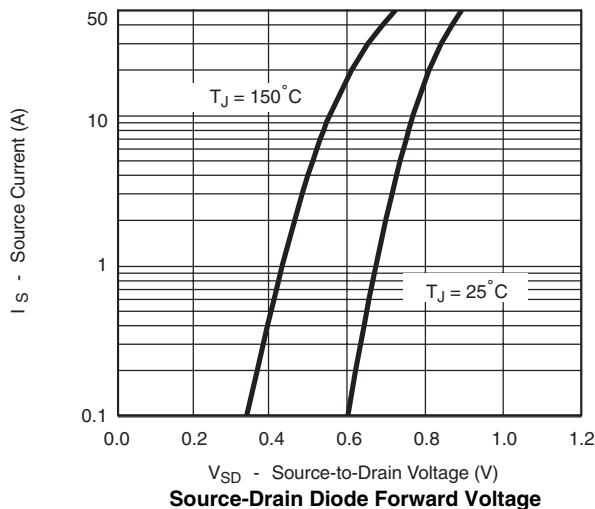
Capacitance



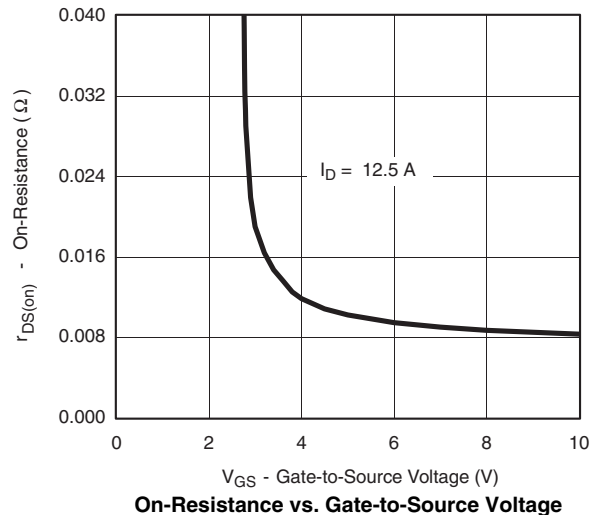
Gate Charge



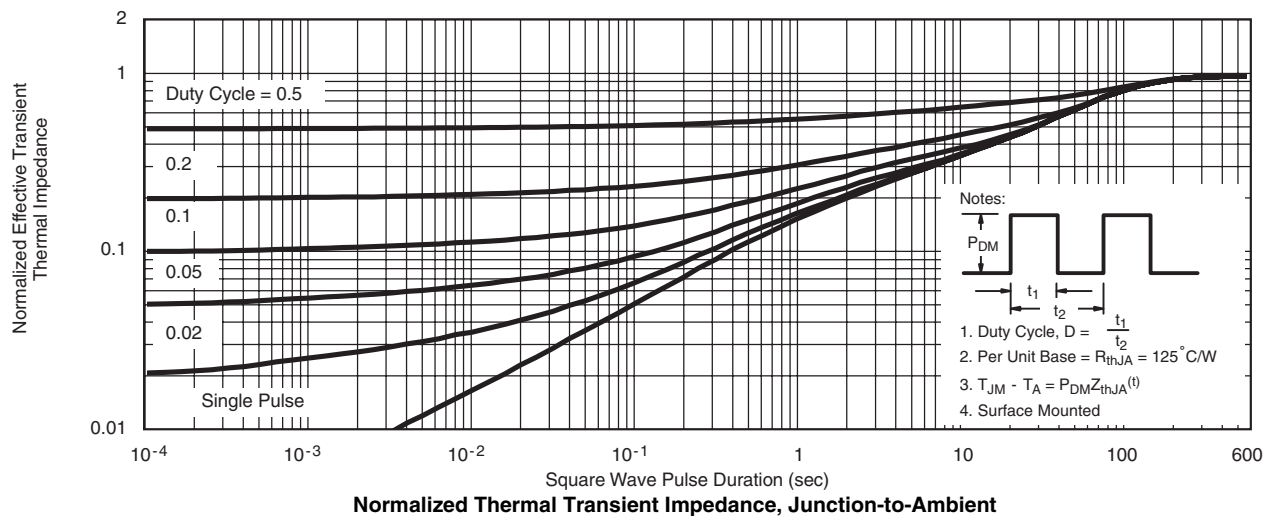
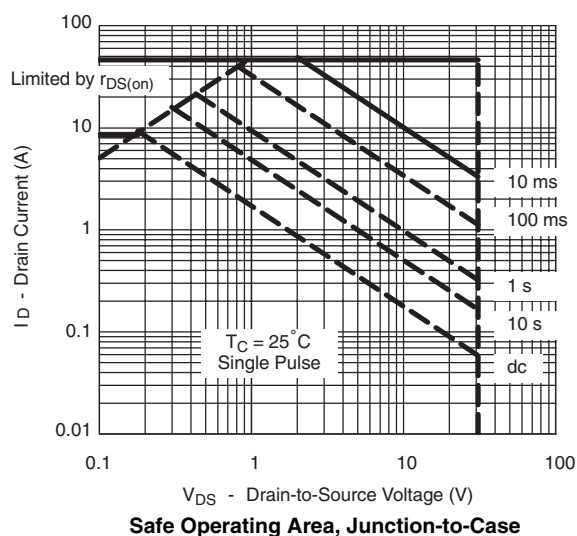
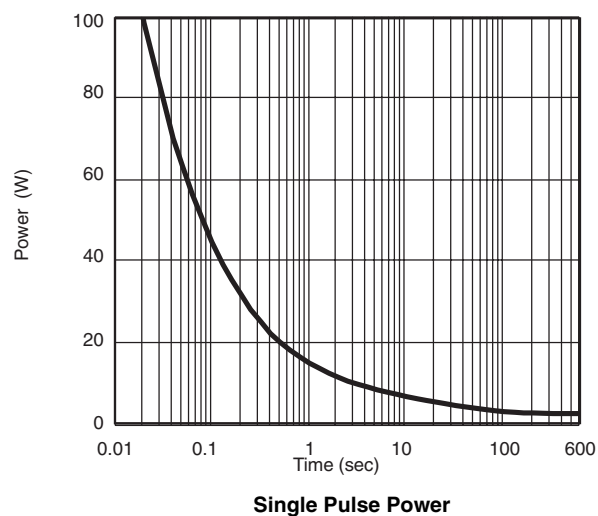
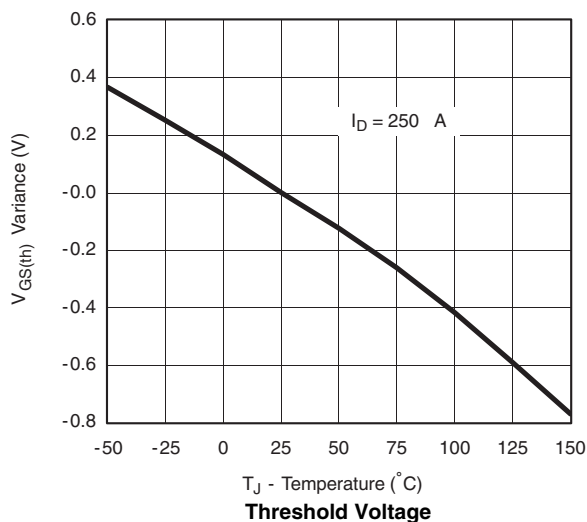
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

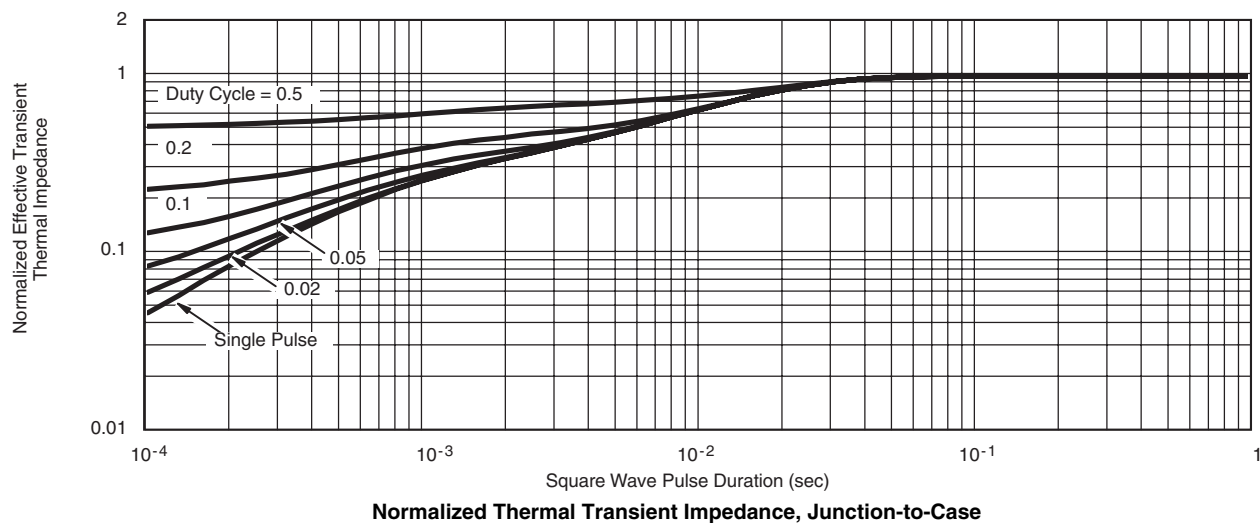


On-Resistance vs. Gate-to-Source Voltage

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TYPICAL CHARACTERISTICS 25 °C unless noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72214>.