N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ)
30	0.0095 @ V_{GS} = 10 V	35	9.2 nC
	0.014 @ V_{GS} = 4.5 V	35	

FEATURES

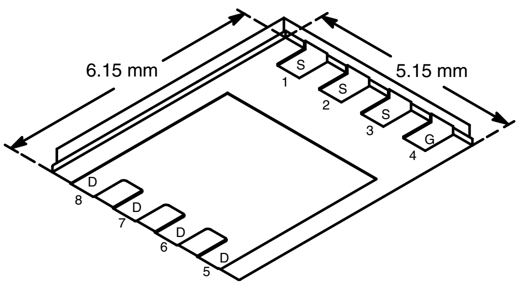
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07mm Profile
- Optimized for High-Side Synchronous Rectifier Operation
- 100% R_g Tested

Pb-free
RoHS COMPLIANT

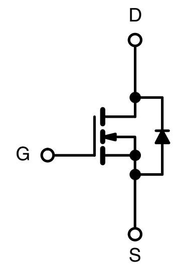
APPLICATIONS

- DC/DC Converters

PowerPAK SO-8



Bottom View
Ordering Information: Si7686DP-T1—E3 (Lead (Pb)-Free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)	T_C = 25°C	I_D	35[a]	A
	T_C = 70°C		35[a]	
	T_A = 25°C		17.9[b, c]	
	T_A = 70°C		14.3[b, c]	
Pulsed Drain Current		I_{DM}	50	
Continuous Source-Drain Diode Current	T_C = 25°C	I_S	31.5	
	T_A = 25°C		4.2[b, c]	
Maximum Power Dissipation	T_C = 25°C	P_D	37.9	W
	T_C = 70°C		24.2	
	T_A = 25°C		5[b, c]	
	T_A = 70°C		3.2[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[b, f]	t ≤ 10 sec	R_{thJA}	21	25	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.8	3.3	

Notes:
a. Package Limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 10 sec
d. See Solder Profile (http://www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 70 °C/W.

New Product

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA		31.3		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			–6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1		3	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	µA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55°C			10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	50			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 13.8 A		0.0078	0.0095	Ω
		V_{GS} = 4.5 V, I_D = 11.4 A		0.011	0.014	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 13.8 A		56		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		1220		pF
Output Capacitance	C_{oss}			230		
Reverse Transfer Capacitance	C_{rss}			98		
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 13.8 A		17	26	nC
		V_{DS} = 15 V, V_{GS} = 5 V, I_D= 13.8 A		9.2	14	
Gate-Source Charge	Q_{gs}			4.1		
Gate-Drain Charge	Q_{gd}			2.8		
Gate Resistance	R_g	f = 1 MHz		0.8	1.2	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1.5 Ω I_D ≅ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω		20	30	ns
Rise Time	t_r			20	30	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			8	15	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 1.5 Ω I_D ≅ 10 A, V_{GEN} = 10 V, R_g = 1 Ω		13	20	
Rise Time	t_r			16	25	
Turn-Off Delay Time	$t_{d(off)}$			23	35	
Fall Time	t_f			8	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25°C			31.5	A
Pulse Diode Forward Current[a]	I_{SM}				50	
Body Diode Voltage	V_{SD}	I_S = 2.6 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 2.6 A, di/dt = 100 A/µs, T_J = 25°C		25	50	ns
Body Diode Reverse Recovery Charge	Q_{rr}			15	30	nC
Reverse Recovery Fall Time	t_a			12.5		ns
Reverse Recovery Rise Time	t_b			12.5		

Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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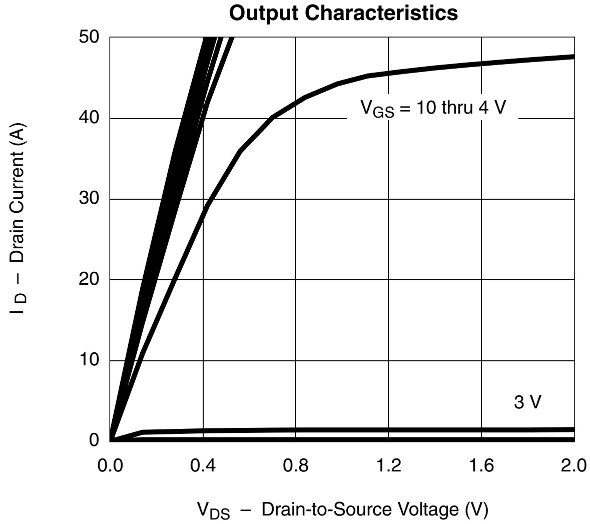
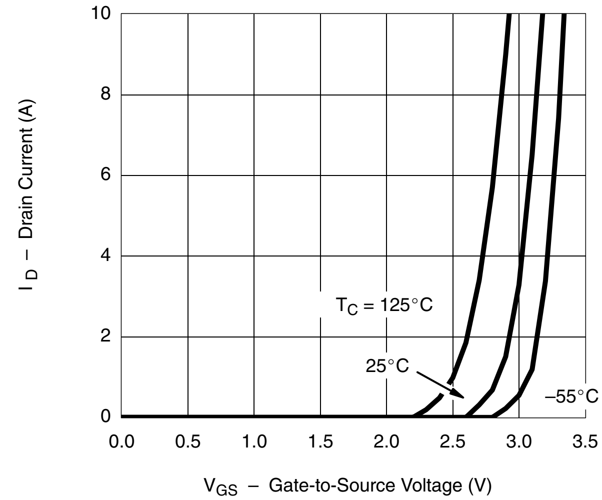
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

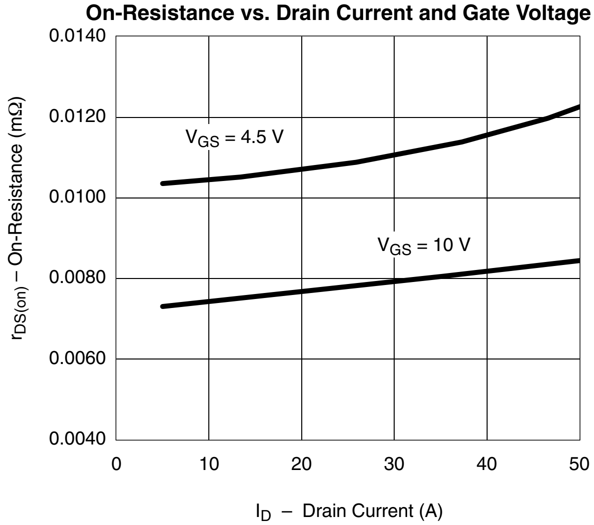
Output Characteristics



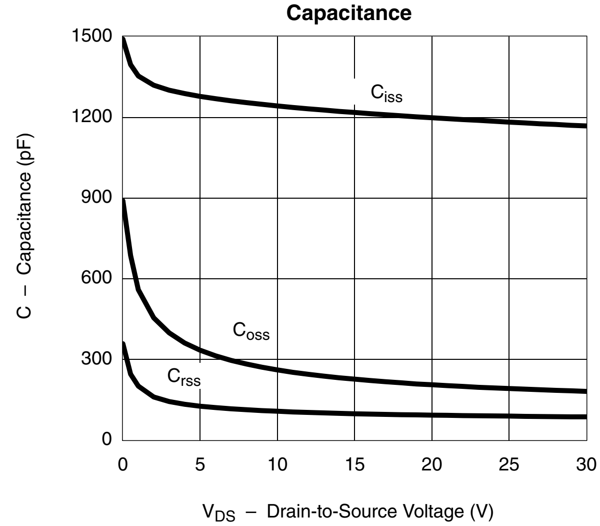
Transfer Characteristics



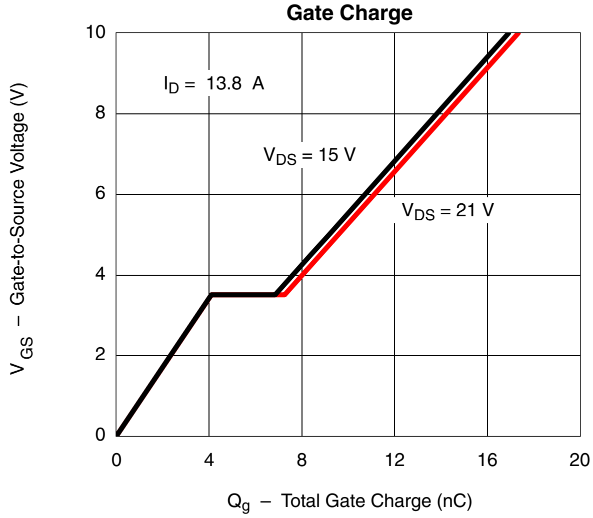
On-Resistance vs. Drain Current and Gate Voltage



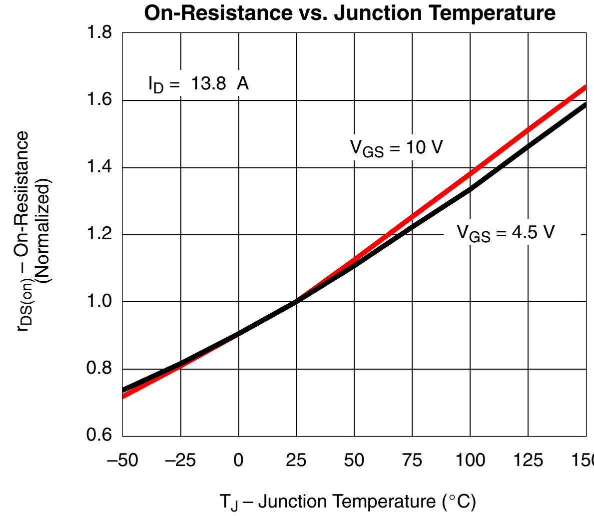
Capacitance



Gate Charge



On-Resistance vs. Junction Temperature



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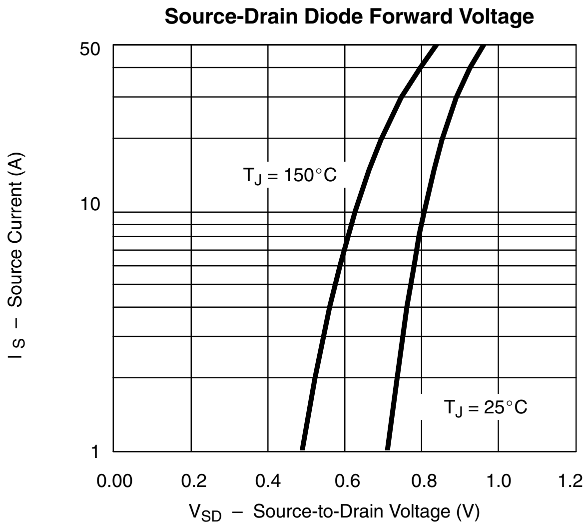

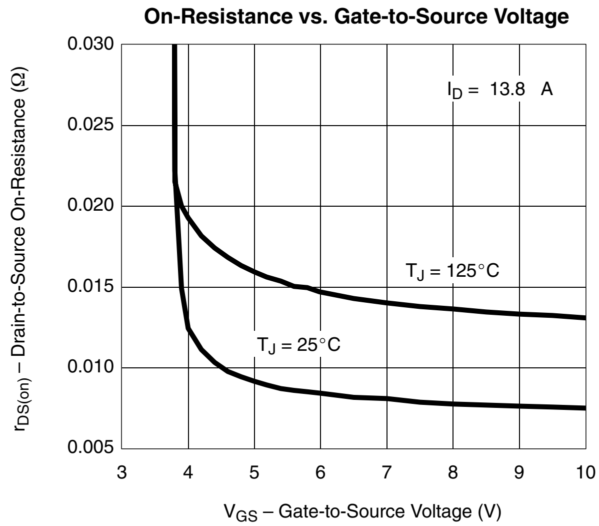

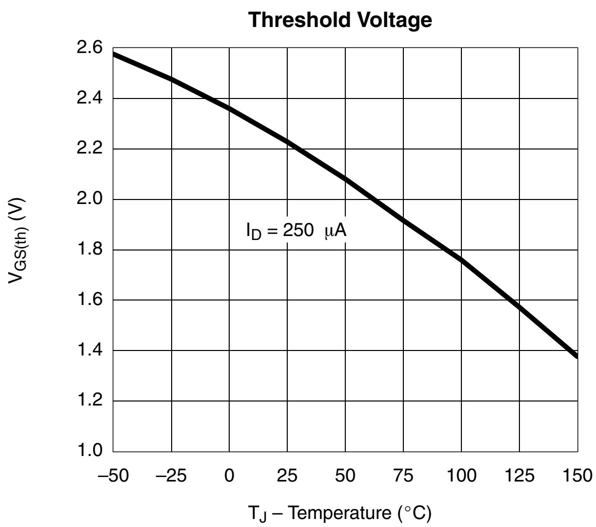

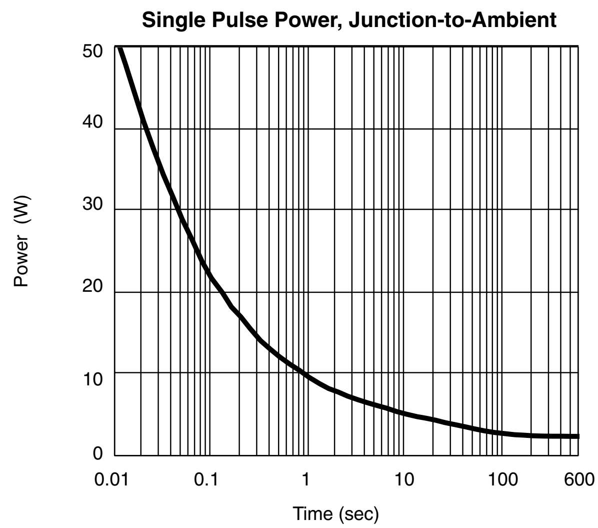

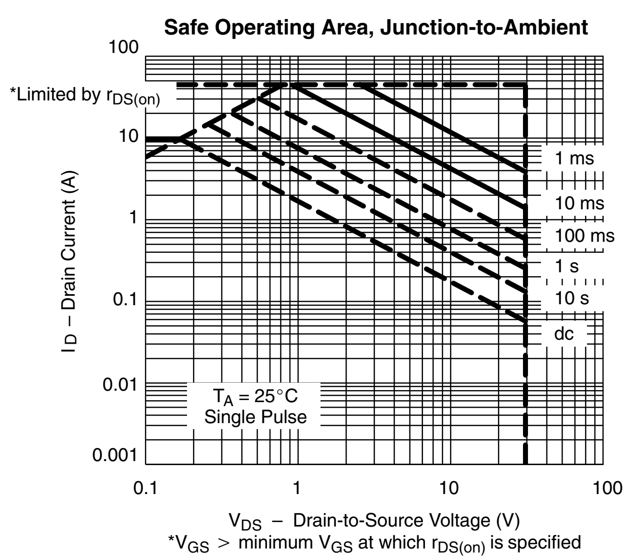

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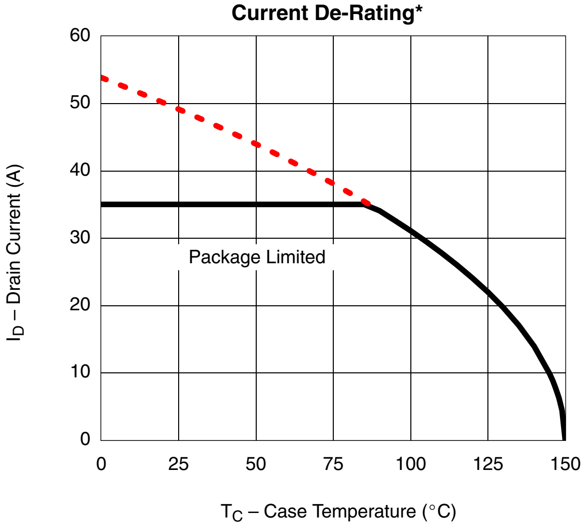
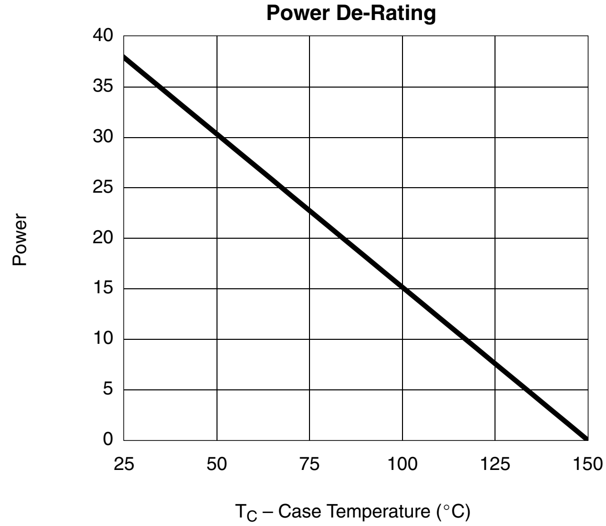
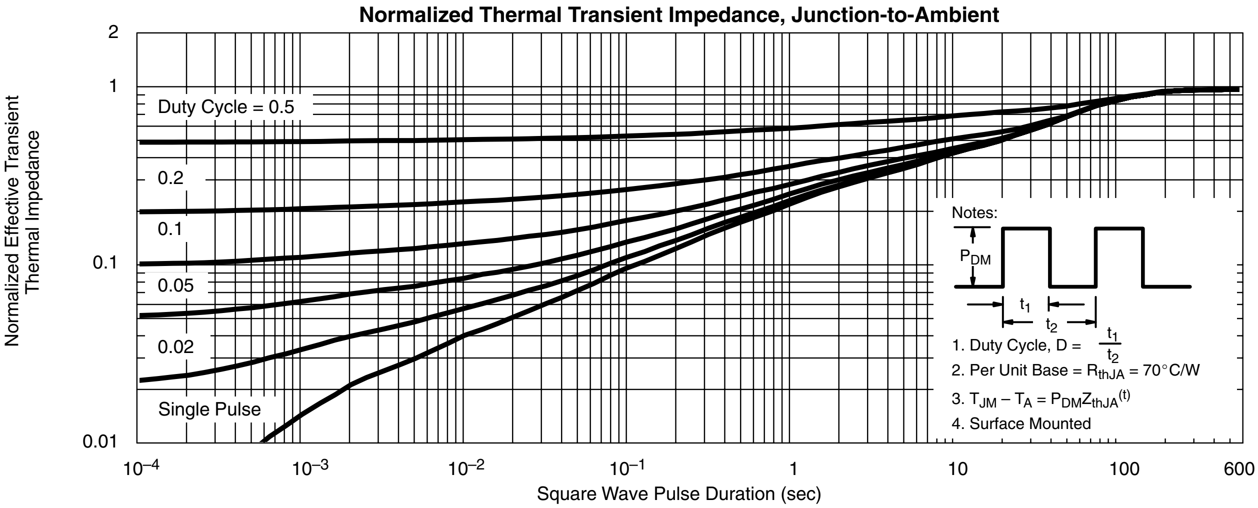
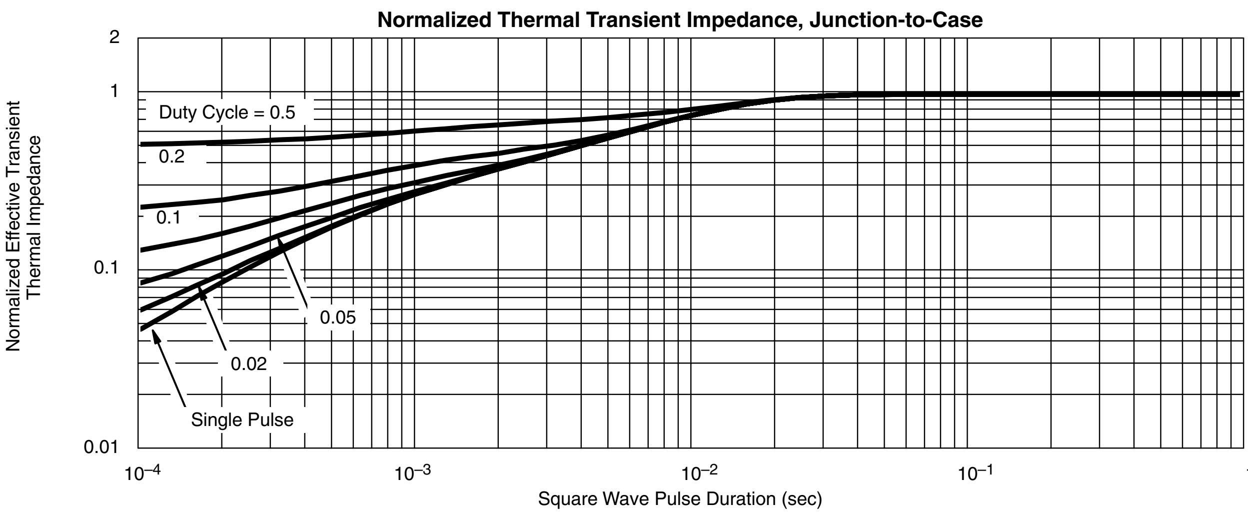




*The power dissipation P_D is based on $T_{J(max)}$ = 150°C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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