FAIRCHILD SEMICONDUCTOR TM

January 2001

SI9426DY

Single N-Channel, 2.5V Specified MOSFET

General Description

This N-Channel 2.5V specified MOSFET is produced using Fairchild Semiconductor's high cell density DMOS technology process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

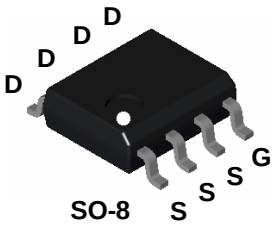
These devices have been designed to offer exceptional power dissipation in a very small footprint package.

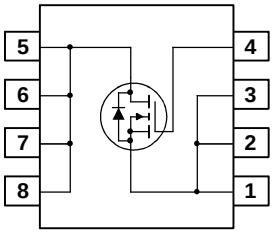
Applications

- DC/DC converter
- Load switch

Features

- 10.5 A, 20 V. $R_{DS(ON)}$ = 13.5 mΩ @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 16 mΩ @ V_{GS} = 2.7 V
- High cell density for extremely low $R_{DS(ON)}$
- High power and current handling capability in a widely used surface mount package





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		±8	V
I_D	Drain Current – Continuous	(Note 1a)	10.5	A
	– Pulsed		30	
P_D	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
9426	SI9426DY	13''	12mm	2500 units

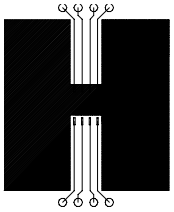
Electrical Characteristics

T_A = 25°C unless otherwise noted

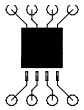
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250µA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V V_{DS} = 16 V, V_{GS} = 0 V, T_J=55°C			1 10	µA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –8 V V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA V_{DS} = V_{GS}, I_D = 250 µA,T_J=125°C	0.4 0.3	0.6 0.5	1.5 0.8	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 4.5 V, I_D = 10.5 A V_{GS} = 4.5 V,I_D = 10.5 A,T_J=125°C V_{GS}=2.7 V, I_D = 10 A		12 17 14	13.5 24 16	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	30			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 10.5 A		43		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		2150		pF
C_{oss}	Output Capacitance			890		pF
C_{rss}	Reverse Transfer Capacitance			165		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DS} = 5 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		11	30	ns
t_r	Turn–On Rise Time			26	55	ns
$t_{d(off)}$	Turn–Off Delay Time			145	220	ns
t_f	Turn–Off Fall Time			40	100	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 10.5 A, V_{GS} = 4.5 V		43	60	nC
Q_{gs}	Gate–Source Charge			7		nC
Q_{gd}	Gate–Drain Charge			8		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				2.1	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)		0.6	1.2	V

Notes:

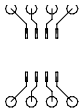
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 105°C/W when mounted on a .04 in^2 pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

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