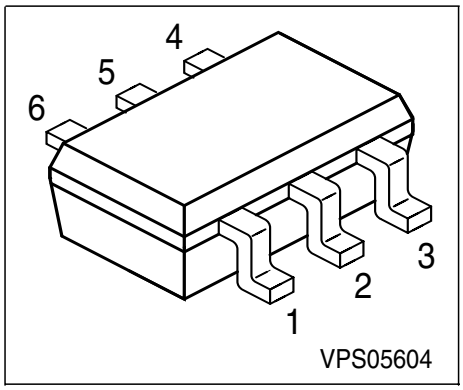
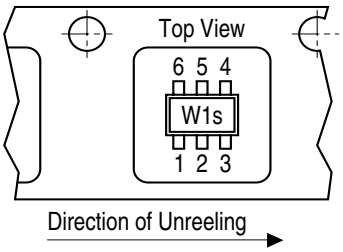
NPN/PNP Silicon Switching Transistor Array

- High current gain
- Low collector-emitter saturation voltage
- Two (galvanic) internal isolated NPN/PNP Transistors in one package



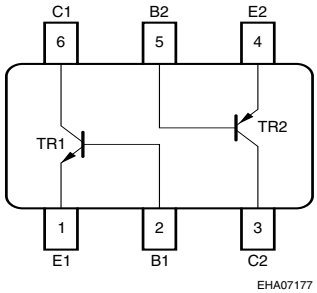
Tape loading orientation



Marking on SOT-363 package (for example W1s) corresponds to pin 1 of device

Position in tape: pin 1 opposite of feed hole side

EHA07193



Type	Marking	Pin Configuration						Package
SMBT3904PN	s3P	1 = E	2 = B	3 = C	4 = E	5 = B	6 = C	SOT363

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	40	V
Collector-base voltage	V_{CBO}	40	
Emitter-base voltage	V_{EBO}	5	
DC collector current	I_C	200	mA
Total power dissipation, T_S = 115 °C	P_{tot}	250	mW
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

Thermal resistance, chip case[1)]	R_{thJC}	≤ 140	K/W

[1]For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics at T_A=25°C, unless otherwise specified

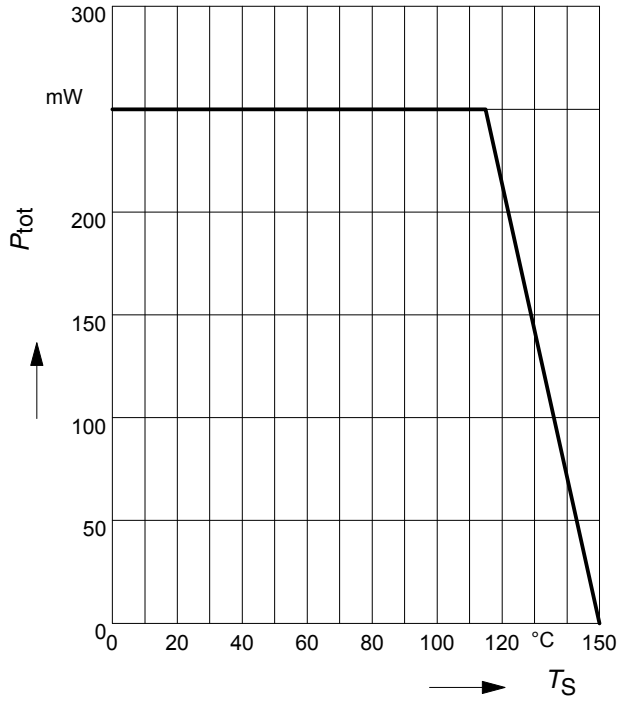
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics per Transistor					
Collector-emitter breakdown voltage I_C = 1 mA, I_B = 0	$V_{(BR)CEO}$	40	-	-	V
Collector-base breakdown voltage I_C = 10 µA, I_E = 0	$V_{(BR)CBO}$	40	-	-	
Emitter-base breakdown voltage I_E = 10 µA, I_C = 0	$V_{(BR)EBO}$	5	-	-	
Collector cutoff current V_{CB} = 30 V, I_E = 0	I_{CBO}	-	-	50	nA
DC current gain 1) I_C = 100 µA, V_{CE} = 1 V I_C = 1 mA, V_{CE} = 1 V I_C = 10 mA, V_{CE} = 1 V I_C = 50 mA, V_{CE} = 1 V I_C = 100 mA, V_{CE} = 1 V	h_{FE}	 40 70 100 60 30	 - - - - -	 - - 300 - -	-
Collector-emitter saturation voltage1) I_C = 10 mA, I_B = 1 mA I_C = 50 mA, I_B = 5 mA	V_{CEsat}	 - -	 - -	 0.25 0.4	V
Base-emitter saturation voltage 1) I_C = 10 mA, I_B = 1 mA I_C = 50 mA, I_B = 5 mA	V_{BEsat}	 0.65 -	 - -	 0.85 0.95	

1) Pulse test: t < 300µs; D < 2%

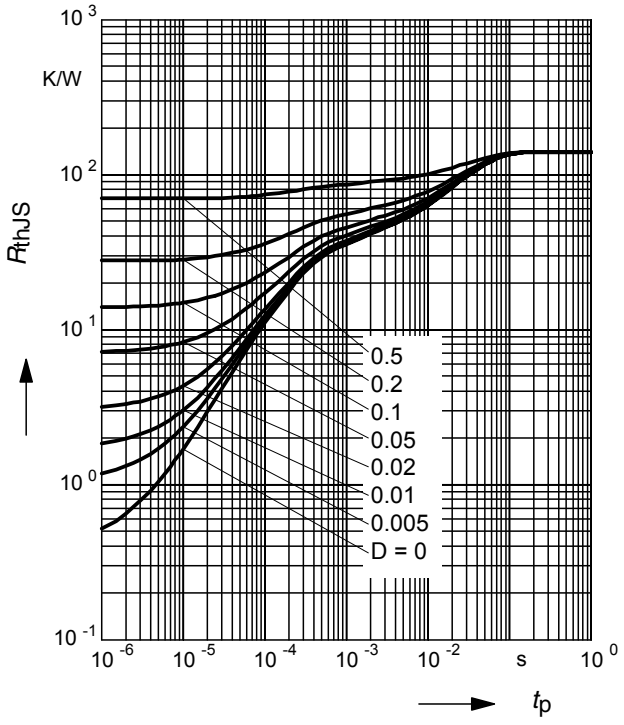
Electrical Characteristics at T_A=25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics per Transistor					
Transition frequency I_C = 10 mA, V_{CE} = 5 V, f = 100 MHz	f_T	250	-	-	MHz
Collector-base capacitance V_{CB} = 10 V, f = 1 MHz	C_{cb}	-	-	4.5	pF
Emitter-base capacitance V_{EB} = 0.5 V, f = 1 MHz	C_{eb}	-	-	10	
Short-circuit input impedance I_C = 2 mA, V_{CE} = 5 V, f = 1 kHz	h_{11e}	2	-	12	kΩ
Open-circuit reverse voltage transf.ratio I_C = 2 mA, V_{CE} = 5 V, f = 1 kHz	h_{12e}	0.1	-	10	10^{-4}
Short-circuit forward current transf.ratio I_C = 2 mA, V_{CE} = 5 V, f = 1 kHz	h_{21e}	100	-	400	-
Open-circuit output admittance I_C = 2 mA, V_{CE} = 5 V, f = 1 kHz	h_{22e}	1	-	60	µS
Noise figure I_C = 100 µA, V_{CE} = 5 V, R_S = 1 kΩ, f = 1 kHz, Δ f = 200 Hz	F	-	-	5	dB
Delay time V_{CC} = 3 V, I_C = 10 mA, I_{B1} = 1 mA, $V_{BE(off)}$ = 0.5 V	t_d	-	-	35	ns
Rise time V_{CC} = 3 V, I_C = 10 mA, I_{B1} = 1 mA, $V_{BE(off)}$ = 0.5 V	t_r	-	-	35	
Storage time V_{CC} = 3 V, I_C = 10 mA, I_{B1}=I_{B2} = 1mA	t_{stg}	-	-	225	
Fall time V_{CC} = 3 V, I_C = 10 mA, I_{B1}=I_{B2} = 1mA	t_f	-	-	75	

Total power dissipation $P_{tot} = f(T_S)$

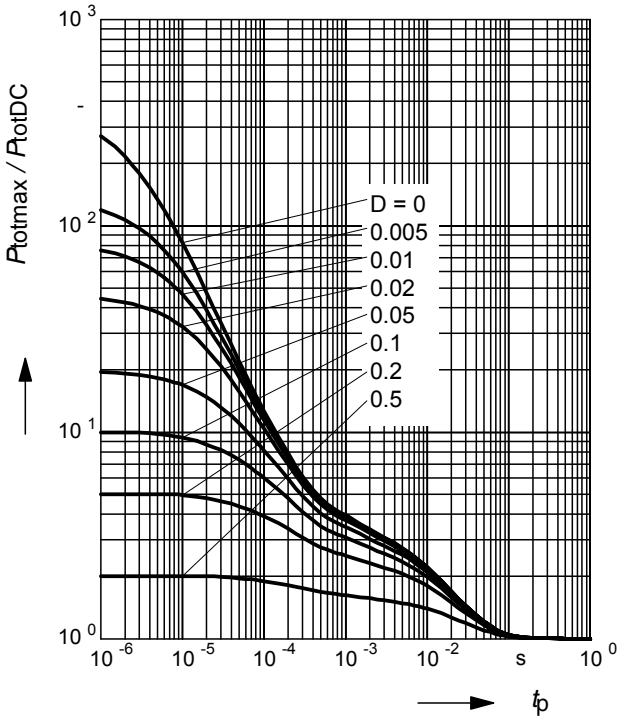


Permissible Pulse Load $R_{thJS} = f(t_p)$



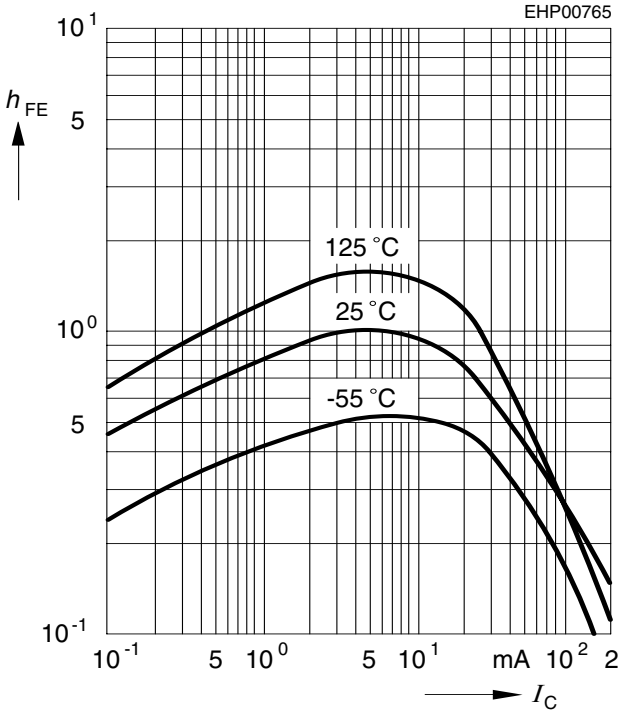
Permissible Pulse Load

$P_{totmax} / P_{totDC} = f(t_p)$



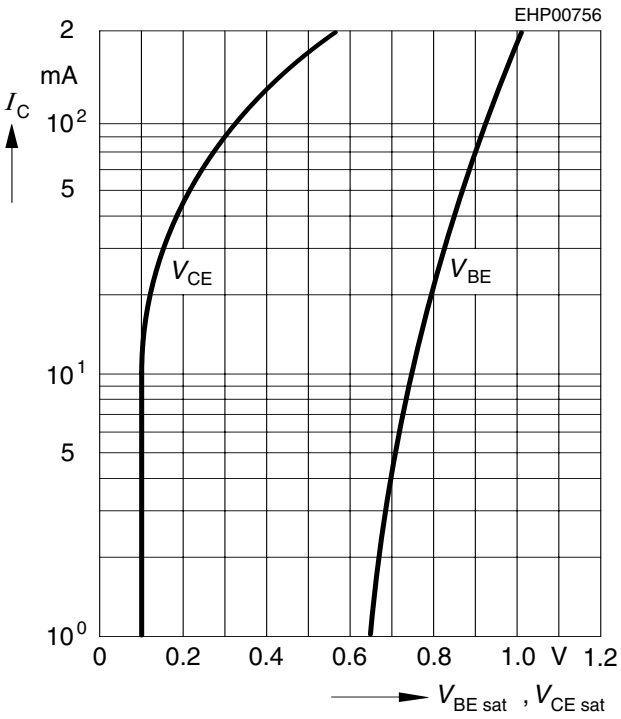
DC current gain $h_{FE} = f(I_C)$

V_{CE} = 10V, normalized



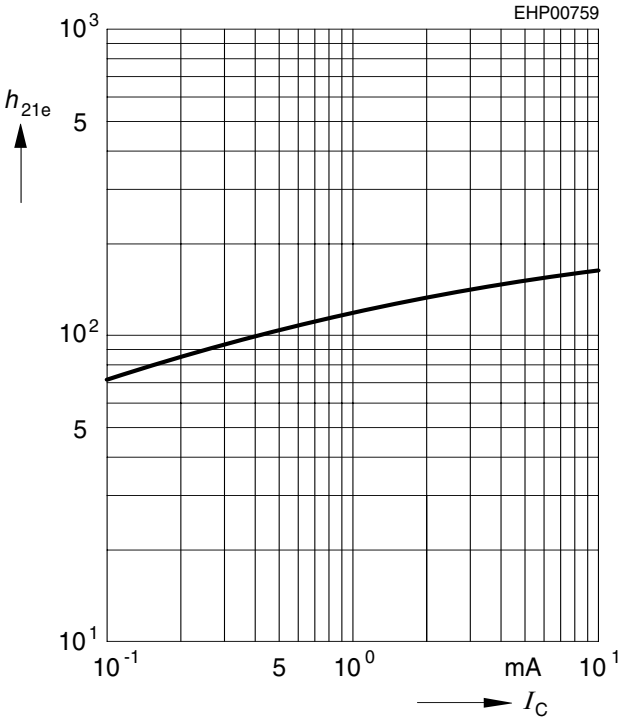
Saturation voltage $I_C = f(V_{BEsat}, V_{CEsat})$

h_{FE} = 10



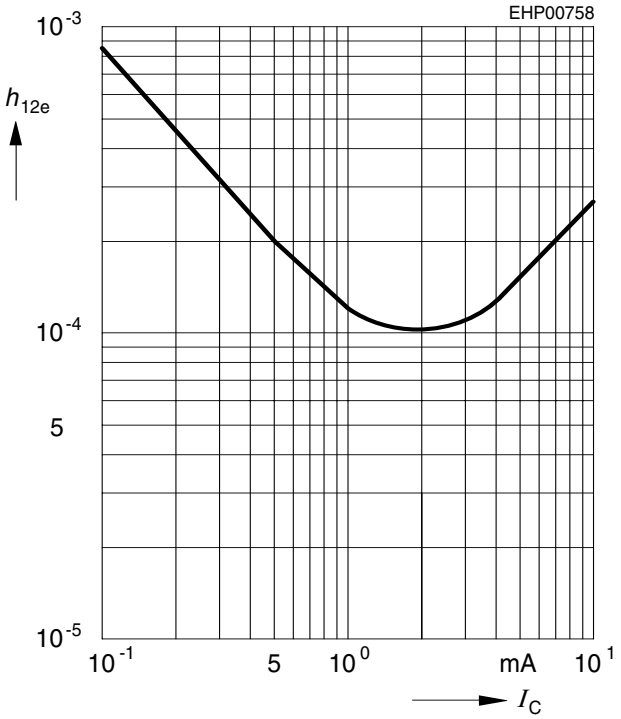
Short-circuit forward current transfer ratio $h_{21e} = f(I_C)$

V_{CE} = 10V, f = 1MHz

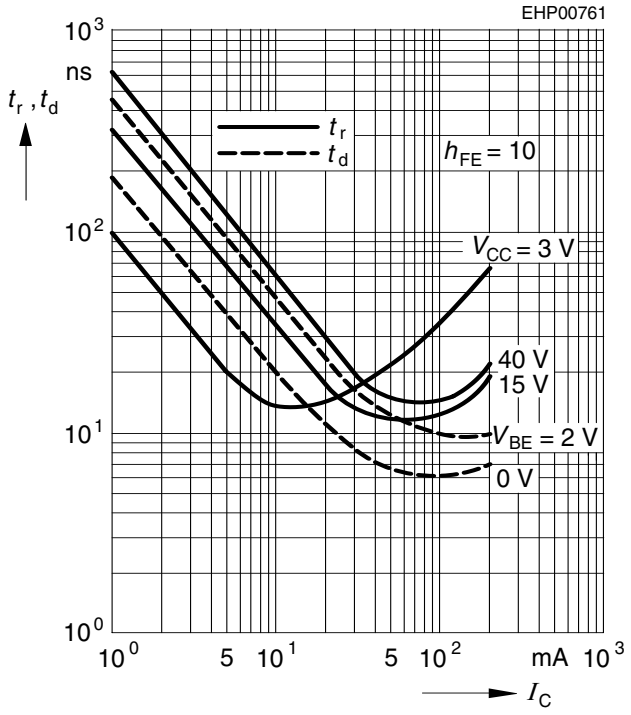


Open-circuit reverse voltage transfer ratio $h_{12e} = f(I_C)$

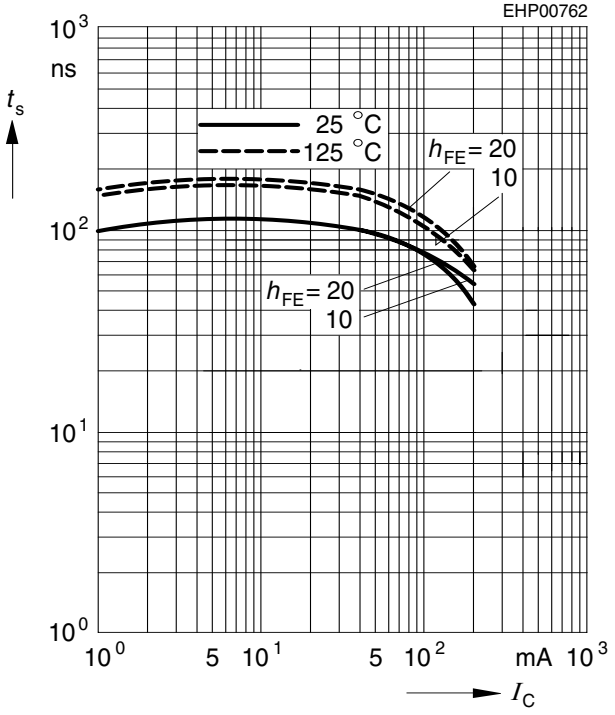
V_{CE} = 10V, f = 1kHz



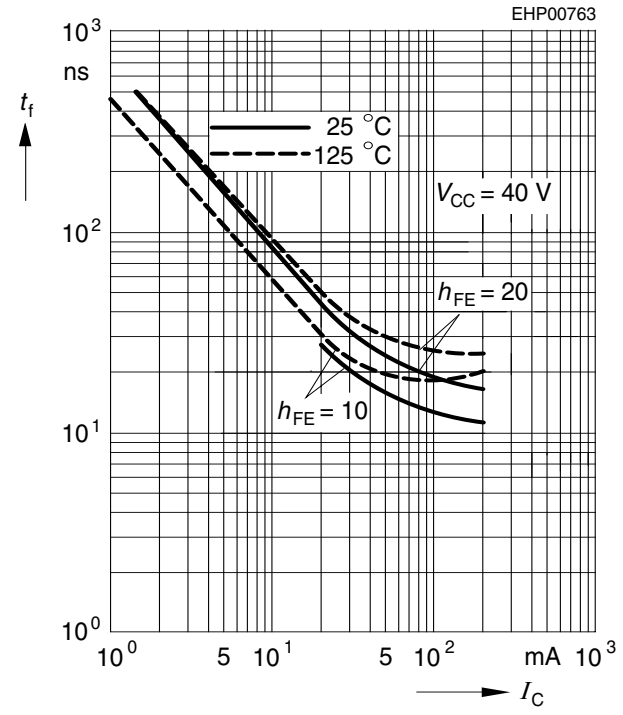
Delay time $t_d = f(I_C)$
Rise time $t_r = f(I_C)$



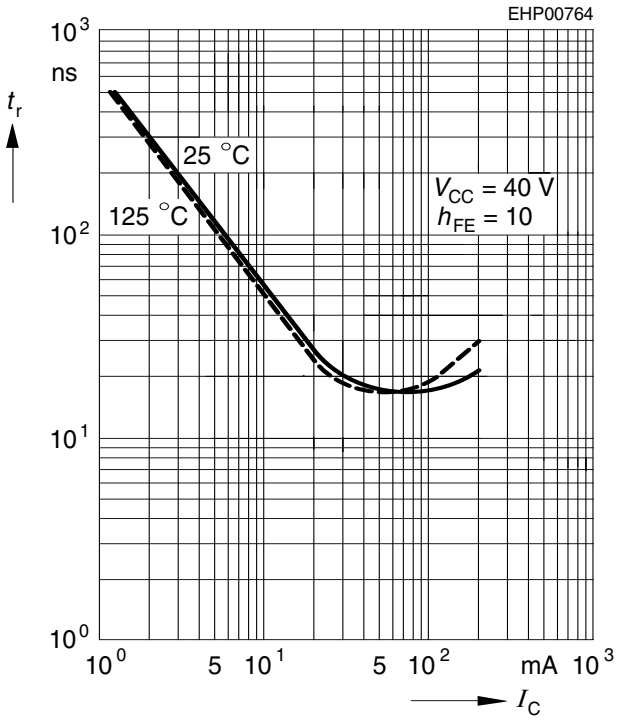
Storage time $t_{stg} = f(I_C)$



Fall time $t_f = f(I_C)$



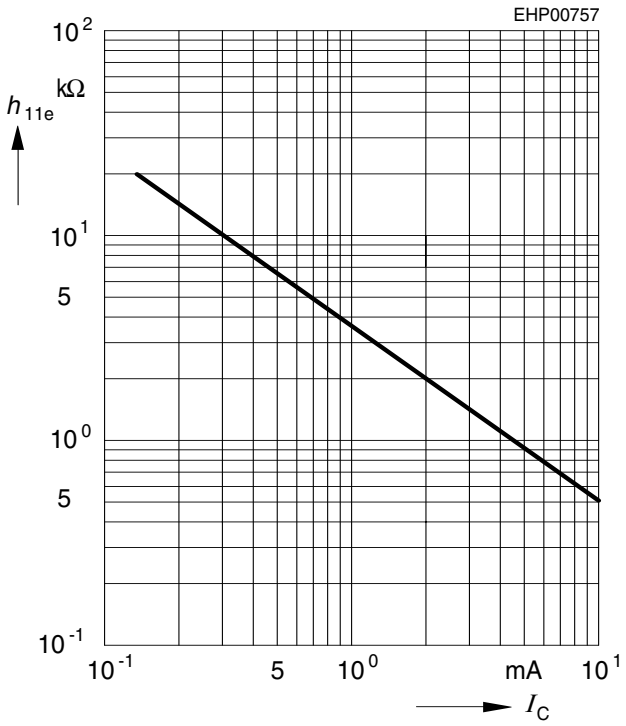
Rise time $t_r = f(I_C)$



Input impedance

$h_{11e} = f(I_C)$

V_{CE} = 10V, f = 1kHz



Open-circuit output admittance

$h_{22e} = f(I_C)$

V_{CE} = 10V, f = 1MHz