

# SN54ALS746, SN54ALS747, SN74ALS746, SN74ALS747 OCTAL BUFFERS AND LINE DRIVERS WITH INPUT PULL-UP RESISTORS

AUGUST 1984 — REVISED MAY 1986

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Input Pull-Up Resistors Added for Data Bus Termination
- Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

## description

These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240A/SN74ALS240A series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout. In addition, 20 kilohm resistors have been added between all inputs and  $V_{CC}$ . This eliminates adding external resistors in applications where the data bus must be at a high level whenever all other connecting devices are at a high impedance state.

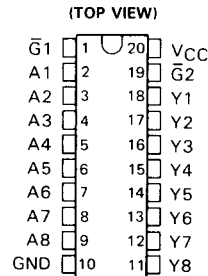
The three-state control gate is a 2-input NOR such that if either  $\bar{G}1$  or  $\bar{G}2$  is high, all eight outputs are in the high-impedance state.

The 'ALS746 provides inverted data and the 'ALS747 provides true data at the outputs.

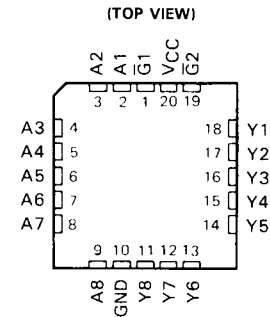
The -1 versions of the SN74ALS746 and SN74ALS747 parts are identical to the standard versions except that the recommended maximum  $I_{OL}$  is increased to 48 milliamperes. There are no -1 versions of the SN54ALS746 and SN54ALS747.

The SN54ALS746 and SN54ALS747 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN54ALS746 and SN74ALS747 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS746, SN54ALS747 . . . J PACKAGE  
SN74ALS746, SN74ALS747 . . . DW OR N PACKAGE

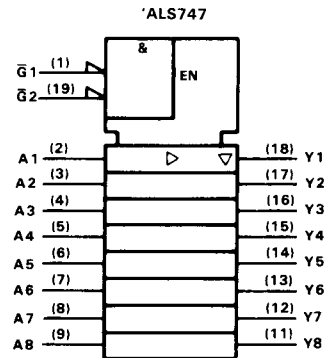
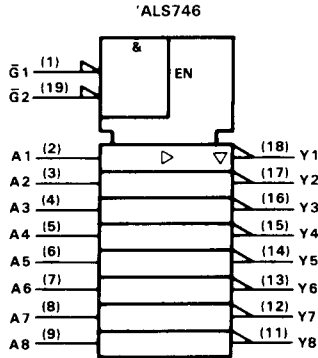


SN54ALS746, SN54ALS747 . . . FK PACKAGE



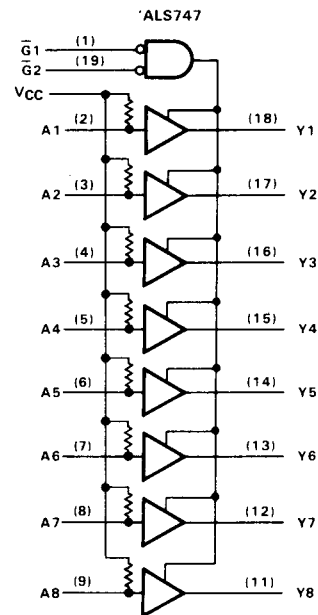
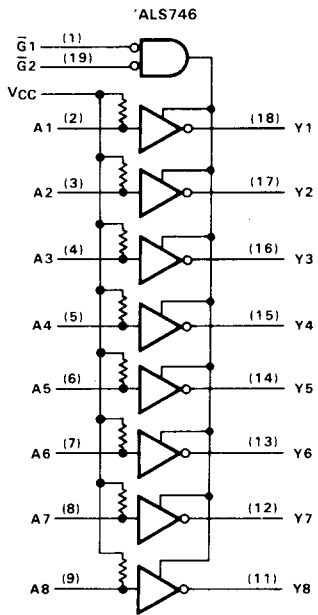
**SN54ALS746, SN54ALS747, SN74ALS746, SN74ALS747**  
**OCTAL BUFFERS AND LINE DRIVERS WITH INPUT PULL-UP RESISTORS**

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)



All input pull-up resistors are 20 kΩ

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# SN54ALS746, SN54ALS747, SN74ALS746, SN74ALS747

## OCTAL BUFFERS AND LINE DRIVERS WITH INPUT PULL-UP RESISTORS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ .....	7 V
Input voltage .....	7 V
Operating free-air temperature range: SN54ALS746, SN54ALS747 .....	-55°C to 125°C
SN74ALS746, SN74ALS747 .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

recommended operating conditions

		SN54ALS746			SN74ALS746			UNIT
		SN54ALS747			SN74ALS747			
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.7			0.8	V
$I_{OH}$	High-level output current			-12			-15	mA
$I_{OL}$	Low-level output current			12			24	mA
							48 <sup>†</sup>	
$T_A$	Operating free-air temperature	-55		125	0		70	°C

<sup>†</sup>The extended limit applies only if  $V_{CC}$  is maintained between 4.75 V and 5.25 V.  
The 48 mA limit applies for the SN74ALS746-1 and SN74ALS747-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS746			SN74ALS746			UNIT
		SN54ALS747			SN74ALS747			
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IK}$	$V_{CC} = 4.5 V, I_I = -18 mA$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 4.5 V \text{ to } 5.5 V, I_{OH} = -0.4 mA$	$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5 V, I_{OH} = -3 mA$	2.4	3.2		2.4	3.2		
	$V_{CC} = 4.5 V, I_{OH} = -12 mA$	2						
	$V_{CC} = 4.5 V, I_{OH} = -15 mA$				2			
$V_{OL}$	$V_{CC} = 4.5 V, I_{OL} = 12 mA$		0.25	0.4		0.25	0.4	V
	$V_{CC} = 4.5 V, I_{OL} = 24 mA^{\dagger}$					0.35	0.5	
$I_{OZH}$	$V_{CC} = 5.5 V, V_O = 2.7 V$			20			20	$\mu A$
$I_{OZL}$	$V_{CC} = 5.5 V, V_O = 0.4 V$			-20			-20	$\mu A$
$I_I$	A	$V_{CC} = 5.5 V, V_I = 5.5 V$		0.1			0.1	mA
	$\bar{G}1, \bar{G}2$	$V_{CC} = 5.5 V, V_I = 7 V$		0.1			0.1	
$I_{IH}$	A	$V_{CC} = 5.5 V, V_I = 2.7 V$		-0.2			-0.2	mA
	$\bar{G}1, \bar{G}2$			20			20	
$I_{IL}$	A	$V_{CC} = 5.5 V, V_I = 0.4 V$		-0.6			-0.6	mA
	$\bar{G}1, \bar{G}2$			-0.1			-0.1	
$I_O^{\S}$	$V_{CC} = 5.5 V, V_O = 2.25 V$	-30		-112	-30		-112	mA
$I_{CC}$	'ALS746	$V_{CC} = 5.5 V,$	Outputs high	7	12	7	12	mA
			Outputs low	13	22	13	22	
			Outputs disabled	11	19	11	19	
	'ALS747	$V_{CC} = 5.5 V,$	Outputs high	6	14	6	14	mA
			Outputs low	18	30	18	30	
			Outputs disabled	12.5	22	12.5	22	

<sup>‡</sup>All typical values are at  $V_{CC} = 5 V, T_A = 25^\circ C$ .

<sup>\S</sup>The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

<sup>\dagger</sup> $I_{OL} = 48 mA$  for -1 versions.

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**SN54ALS746, SN54ALS747, SN74ALS746, SN74ALS747**  
**OCTAL BUFFERS AND LINE DRIVERS WITH INPUT PULL-UP RESISTORS**

**ALS746 switching characteristics (see Note 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 5 V, CL = 50 pF, R1 = 500 Ω, R2 = 500 Ω, TA = 25°C		VCC = 4.5 V to 5.5 V, CL = 50 pF, R1 = 500 Ω, R2 = 500 Ω, TA = MIN to MAX		UNIT		
			ALS746		SN54ALS746			SN74ALS746	
			TYP	MIN	MAX	MIN		MAX	
tPLH	A	Y	7.5	3	14 $\checkmark$	3	12	$\checkmark$	
tPHL	A	Y	5.6	2	11 $\checkmark$	2 $\checkmark$	9	ns	
tPZH	$\bar{G}$	Y	9	5	18 $\checkmark$	5 $\checkmark$	15	$\checkmark$	
tPZL	$\bar{G}$	Y	12.5	8	24 $\checkmark$	8 $\checkmark$	20	ns	
tPHZ	$\bar{G}$	Y	4	1	12 $\checkmark$	1 $\checkmark$	10	$\checkmark$	
tPLZ	$\bar{G}$	Y	7	2	14 $\checkmark$	2 $\checkmark$	12	ns	

**ALS747 switching characteristics (see Note 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 5 V, CL = 50 pF, R1 = 500 Ω, R2 = 500 Ω, TA = 25°C		VCC = 4.5 V to 5.5 V, CL = 50 pF, R1 = 500 Ω, R2 = 500 Ω, TA = MIN to MAX		UNIT		
			ALS747		SN54ALS747			SN74ALS747	
			TYP	MIN	MAX	MIN		MAX	
tPLH	A	Y	8.7	4 $\checkmark$	17	4	14	$\checkmark$ ns	
tPHL	A	Y	7.4	2 $\checkmark$	12	2	10	$\checkmark$ ns	
tPZH	$\bar{G}$	Y	9	5 $\checkmark$	18	5	15	$\checkmark$ ns	
tPZL	$\bar{G}$	Y	12.5	8 $\checkmark$	24	8	20	$\checkmark$ ns	
tPHZ	$\bar{G}$	Y	4	1 $\checkmark$	12	1	10	$\checkmark$ ns	
tPLZ	$\bar{G}$	Y	7	2 $\checkmark$	14	2	12	$\checkmark$ ns	

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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