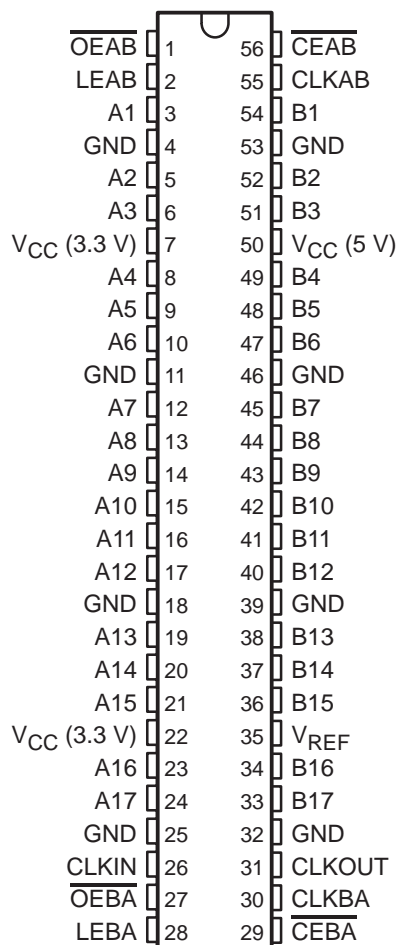


SN54GTL16616, SN74GTL16616 17-BIT LVTTTL-TO-GTL/GTL+ UNIVERSAL BUS TRANSCEIVERS WITH BUFFERED CLOCK OUTPUTS

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- **Members of the Texas Instruments Widebus™ Family**
- **Universal Bus Transceiver (UBT™) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, Clocked, or Clock-Enabled Mode**
- **GTL Buffered CLKAB Signal (CLKOUT)**
- **Translate Between GTL/GTL+ Signal Levels and LVTTTL Logic Levels**
- **Support Mixed-Mode (3.3 V and 5 V) Signal Operation on A-Port and Control Inputs**
- **Equivalent to '16601 Function**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors on A Port**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **Distributed V_{CC} and GND-Pin Configuration Minimizes High-Speed Switching Noise**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Ceramic Flat (WD) Packages**

SN54GTL16616 . . . WD PACKAGE
SN74GTL16616 . . . DGG OR DL PACKAGE
(TOP VIEW)



description

The 'GTL16616 devices are 17-bit universal bus transceivers (UBTs) that provide LVTTTL-to-GTL/GTL+ and GTL/GTL+-to-LVTTTL signal-level translation. They combine D-type flip-flops and D-type latches to allow for transparent, latched, clocked, and clocked-enabled modes of data transfer identical to the '16601 function. Additionally, they provide for a copy of CLKAB at GTL/GTL+ signal levels (CLKOUT) and conversion of a GTL/GTL+ clock to LVTTTL logic levels (CLKIN). The devices provide an interface between cards operating at LVTTTL logic levels and a backplane operating at GTL/GTL+ signal levels. Higher-speed operation is a direct result of the reduced output swing (<1 V), reduced input threshold levels, and output edge control (OEC™).

The user has the flexibility of using this device at either GTL ($V_{TT} = 1.2\text{ V}$ and $V_{REF} = 0.8\text{ V}$) or the preferred higher noise margin GTL+ ($V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$) signal levels. GTL+ is the Texas Instruments derivative of the Gunning transceiver logic (GTL) JEDEC standard JESD 8-3. The B port normally operates at GTL or GTL+ signal levels, while the A-port and control inputs are compatible with LVTTTL logic levels and are 5-V tolerant. V_{REF} is the reference input voltage for the B port. $V_{CC} (5\text{ V})$ supplies the internal and GTL circuitry while $V_{CC} (3.3\text{ V})$ supplies the LVTTTL output buffers.



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**TEXAS
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description (continued)

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable (\overline{CEAB} and \overline{CEBA}) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if \overline{CEAB} is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if \overline{CEAB} also is low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B, but uses \overline{OEBA} , LEBA, CLKBA, and \overline{CEBA} .

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven LVTTTL inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54GTL16616 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74GTL16616 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS					OUTPUT B	MODE
\overline{CEAB}	\overline{OEAB}	LEAB	CLKAB	A		
X	H	X	X	X	Z	Isolation
L	L	L	H or L	X	B_0^{\ddagger}	Latched storage of A data
L	L	L	H or L	X	B_0^{\S}	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	\uparrow	L	L	Clocked storage of A data
L	L	L	\uparrow	H	H	
H	L	L	X	X	B_0^{\S}	Clock inhibit

† A-to-B data flow is shown. B-to-A data flow is similar, but uses \overline{OEBA} , LEBA, \overline{CLKBA} , and \overline{CEBA} .

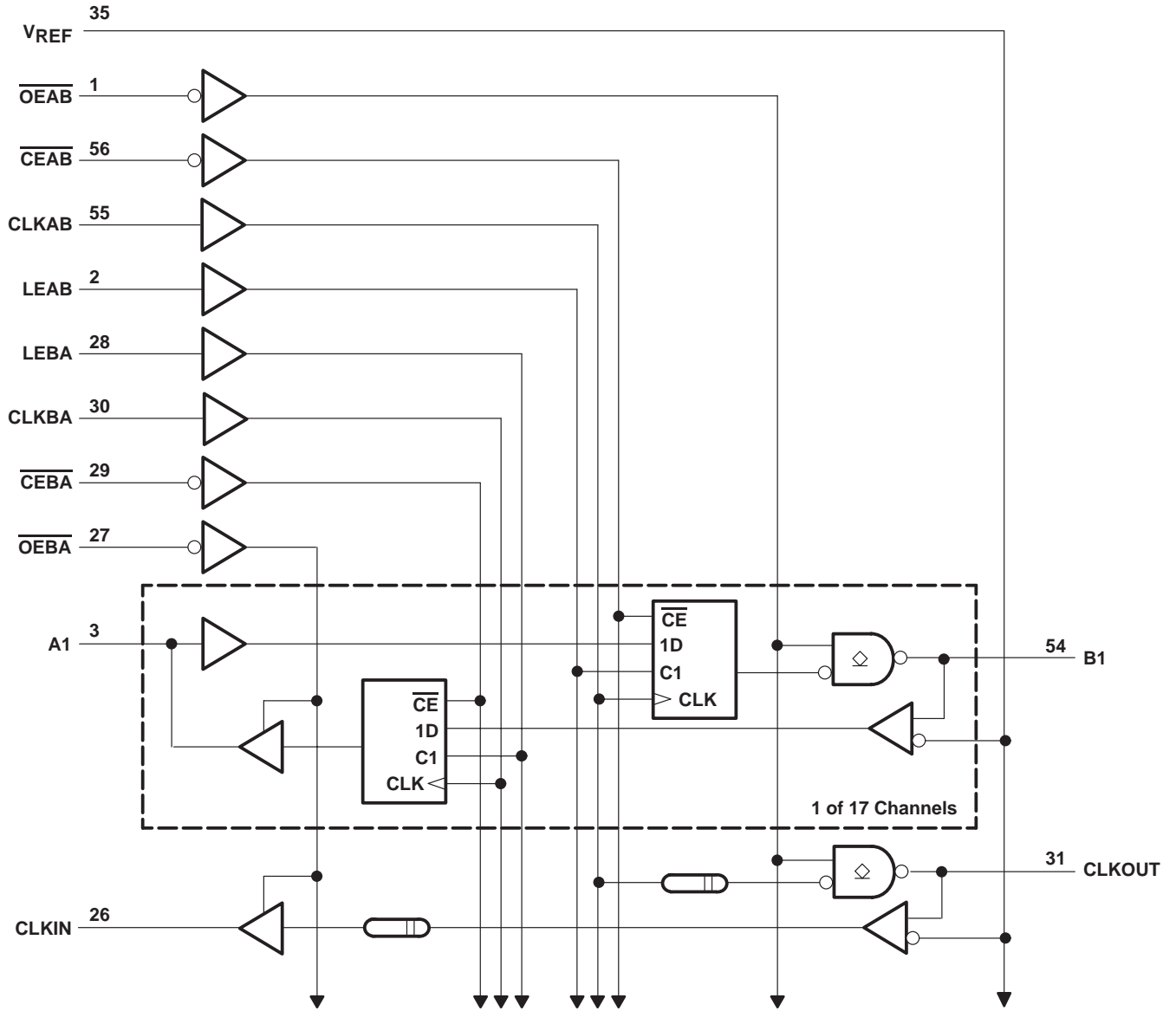
‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established

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logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} : 3.3 V	-0.5 V to 4.6 V
5 V	-0.5 V to 7 V
Input voltage range, V_I (see Note 1): A-port and control inputs	-0.5 V to 7 V
B port and V_{REF}	-0.5 V to 4.6 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1): A port	-0.5 V to 7 V
B port	-0.5 V to 4.6 V
Current into any output in the low state, I_O : A port	128 mA
B port	80 mA
Current into any A-port output in the high state, I_O (see Note 2)	64 mA
Continuous current through each V_{CC} or GND	± 100 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	64°C/W
DL package	56°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Notes 4 through 6)

		SN54GTL16616			SN74GTL16616			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	3.3 V	3.15	3.3	3.45	3.15	3.3	3.45	V
	5 V	4.75	5	5.25	4.75	5	5.25	
V_{TT} Termination voltage	GTL	1.14	1.2	1.26	1.14	1.2	1.26	V
	GTL+	1.35	1.5	1.65	1.35	1.5	1.65	
V_{REF} Supply voltage	GTL	0.74	0.8	0.87	0.74	0.8	0.87	V
	GTL+	0.87	1	1.1	0.87	1	1.1	
V_I Input voltage	B port	V_{TT}			V_{TT}			V
	Except B port	5.5			5.5			
V_{IH} High-level input voltage	B port	$V_{REF}+50$ mV			$V_{REF}+50$ mV			V
	Except B port	2			2			
V_{IL} Low-level input voltage	B port	$V_{REF}-50$ mV			$V_{REF}-50$ mV			V
	Except B port	0.8			0.8			
I_{IK} Input clamp current		-18			-18			mA
I_{OH} High-level output current	A port	-32			-32			mA
I_{OL} Low-level output current	A port	64			64			mA
	B port	40			40			
T_A Operating free-air temperature		-55		125	-40		85	°C

- NOTES: 4. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
5. Normal connection sequence is GND first, $V_{CC} = 5$ V second, and $V_{CC} = 3.3$ V, I/O, control inputs, V_{TT} and V_{REF} (any order) last.
6. V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances as long as they do not exceed the DC absolute I_{OL} ratings. Similarly, V_{REF} can be adjusted to optimize noise margins, but normally is $2/3 V_{TT}$.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54GTL16616			SN74GTL16616			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} (3.3 V) = 3.15 V, V _{CC} (5 V) = 4.75 V, I _I = -18 mA		-1.2			-1.2			V
V _{OH}	A port	V _{CC} (3.3 V) = 3.15 V to 3.45 V, V _{CC} (5 V) = 4.75 V to 5.25 V	I _{OH} = -100 μA	V _{CC} -0.2			V _{CC} -0.2			V
			I _{OH} = -8 mA	2.4			2.4			
		I _{OH} = -32 mA	2			2				
V _{OL}	A port	V _{CC} (3.3 V) = 3.15 V, V _{CC} (5 V) = 4.75 V	I _{OL} = 100 μA				0.2			V
			I _{OL} = 16 mA				0.4			
			I _{OL} = 32 mA				0.5			
			I _{OL} = 64 mA				0.55			
	B port	V _{CC} (3.3 V) = 3.15 V, V _{CC} (5 V) = 4.75 V	I _{OL} = 40 mA				0.4			
I _I	Control inputs	V _{CC} = 0 or 3.45 V, V _{CC} (5 V) = 0 or 5.25 V	V _I = 5.5 V				10			μA
	A port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V	V _I = 5.5 V				20			
			V _I = V _{CC} (3.3 V)				1			
			V _I = 0				-30			
	B port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V	V _I = V _{CC} (3.3 V)				5			
V _I = 0						-5				
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V					100			μA
I _I (hold)	A port	V _{CC} (3.3 V) = 3.15 V, V _{CC} (5 V) = 4.75 V	V _I = 0.8 V	75			75			μA
			V _I = 2 V	-75			-75			
			V _I = 0 to V _{CC} (3.3 V)‡	±500			±500			
I _{OZH}	A port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V, V _O = 3 V				1			μA	
	B port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V, V _O = 1.2 V				10				
I _{OZL}	A port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V, V _O = 0.5 V				-1			μA	
	B port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V, V _O = 0.4 V				-10				
I _{CC} (3.3 V)	A or B port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V, I _O = 0, V _I = V _{CC} (3.3 V) or GND	Outputs high	1			1			mA
			Outputs low	5			5			
			Outputs disabled	1			1			
I _{CC} (5 V)	A or B port	V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V, I _O = 0, V _I = V _{CC} (3.3 V) or GND	Outputs high	120			120			mA
			Outputs low	120			120			
			Outputs disabled	120			120			
ΔI _{CC} §		V _{CC} (3.3 V) = 3.45 V, V _{CC} (5 V) = 5.25 V, A-port or control inputs at V _{CC} (3.3 V) or GND, One input at 2.7 V					1			mA
C _i	Control inputs	V _I = 3.15 V or 0		3.5			3.5			pF
C _{io}	A port	V _O = 3.15 V or 0		12			12			pF
	B port	Per IEEE Std 1194.1		5			5			

† All typical values are at V_{CC} (3.3 V) = 3.3 V, V_{CC} (5 V) = 5 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.2\text{ V}$ and $V_{REF} = 0.8\text{ V}$ for GTL (unless otherwise noted) (see Figure 1)

		SN54GTL16616		SN74GTL16616		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	95		95		MHz
t_w	Pulse duration	LEAB or LEBA high		3.3		ns
		CLKAB or CLKBA high or low		5.5		
t_{su}	Setup time	A before CLKAB \uparrow		1.3		ns
		B before CLKBA \uparrow		2.5		
		A before LEAB \downarrow		0		
		B before LEBA \downarrow		1.1		
		\overline{CEAB} before CLKAB \uparrow		2.2		
		\overline{CEBA} before CLKBA \uparrow		2.7		
t_h	Hold time	A after CLKAB \uparrow		1.6		ns
		B after CLKBA \uparrow		0.4		
		A after LEAB \downarrow		4		
		B after LEBA \downarrow		3.5		
		\overline{CEAB} after CLKAB \uparrow		1.1		
		\overline{CEBA} after CLKBA \uparrow		0.9		

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.2\text{ V}$ and $V_{REF} = 0.8\text{ V}$ for GTL (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16616			SN74GTL16616			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			95			95			MHz
t_{PLH}	A	B	1.4	3	4.6	1.7	3	4.4	ns
t_{PHL}			1.2	2.8	4.7	1.4	2.8	4.5	
t_{PLH}	LEAB	B	2.1	3.8	5.6	2.3	3.8	5.4	ns
t_{PHL}			1.9	3.7	5.6	2.2	3.7	5.3	
t_{PLH}	CLKAB	B	2.2	4	5.9	2.4	4	5.7	ns
t_{PHL}			1.8	3.7	5.7	2.1	3.7	5.4	
t_{PLH}	CLKAB	CLKOUT	4.5	6.1	8.2	4.7	6.1	8.1	ns
t_{PHL}			5.5	7.9	11.4	5.7	7.9	11.3	
t_{dis}	\overline{OEAB}	B or CLKOUT	2	3.8	5.8	2.1	3.8	5.6	ns
t_{en}			2	3.6	5.2	2.1	3.6	5.1	
t_r	Transition time, B outputs (0.5 V to 1 V)		1.2			1.2			ns
t_f	Transition time, B outputs (1 V to 0.5 V)		0.7			0.7			ns
t_{PLH}	B	A	1.6	4	6.8	1.7	4	6.7	ns
t_{PHL}			1.3	2.9	4.7	1.4	2.9	4.7	
t_{PLH}	LEBA	A	2.3	3.8	6.1	2.4	3.8	5.8	ns
t_{PHL}			1.9	3	4.8	2	3	4.6	
t_{PLH}	CLKBA	A	2.5	4	6.3	2.6	4	6	ns
t_{PHL}			2.1	3.4	5.1	2.2	3.4	4.9	
t_{PLH}	CLKOUT	CLKIN	7.2	10	14.7	7.4	10	14.4	ns
t_{PHL}			5.9	8.1	11.8	6.1	8.1	11.7	
t_{en}	\overline{OEBA}	A or CLKIN	2.7	5.3	8.1	2.8	5.3	7.8	ns
t_{dis}			2.6	4.3	6.7	2.7	4.3	6.4	

† All typical values are at $V_{CC} (3.3\text{ V}) = 3.3\text{ V}$, $V_{CC} (5\text{ V}) = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$ for GTL+ (unless otherwise noted) (see Figure 1)

		SN54GTL16616		SN74GTL16616		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	95		95		MHz
t_w	Pulse duration	LEAB or LEBA high		3.3		ns
		CLKAB or CLKBA high or low		5.5		
t_{su}	Setup time	A before CLKAB \uparrow		1.3		ns
		B before CLKBA \uparrow		2.3		
		A before LEAB \downarrow		0		
		B before LEBA \downarrow		1.3		
		CEAB before CLKAB \uparrow		2.2		
		CEBA before CLKBA \uparrow		2.7		
t_h	Hold time	A after CLKAB \uparrow		1.6		ns
		B after CLKBA \uparrow		0.6		
		A after LEAB \downarrow		4		
		B after LEBA \downarrow		3.5		
		CEAB after CLKAB \uparrow		1.1		
		CEBA after CLKBA \uparrow		0.9		

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$ for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16616			SN74GTL16616			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			95			95			MHz
t_{PLH}	A	B	1.4	3	4.6	1.7	3	4.4	ns
t_{PHL}			1.2	2.9	4.8	1.4	2.9	4.6	
t_{PLH}	LEAB	B	2.1	3.8	5.6	2.3	3.8	5.4	ns
t_{PHL}			1.9	3.7	5.7	2.2	3.7	5.4	
t_{PLH}	CLKAB	B	2.2	4	5.9	2.4	4	5.7	ns
t_{PHL}			1.8	3.8	5.8	2.1	3.8	5.5	
t_{PLH}	CLKAB	CLKOUT	4.5	6.1	8.2	4.7	6.1	8.1	ns
t_{PHL}			5.5	8	11.5	5.7	8	11.4	
t_{PLH}	\overline{OEAB}	B or CLKOUT	2	3.6	5.2	2.1	3.6	5.1	ns
t_{PHL}			2	3.8	5.9	2.1	3.8	5.7	
t_r	Transition time, B outputs (0.5 V to 1 V)		1.4			1.4			ns
t_f	Transition time, B outputs (1 V to 0.5 V)		1			1			ns
t_{PLH}	B	A	1.5	3.9	6.8	1.6	3.9	6.6	ns
t_{PHL}			1.2	2.8	4.5	1.3	2.8	4.5	
t_{PLH}	LEBA	A	2.3	3.8	6.1	2.4	3.8	5.8	ns
t_{PHL}			1.9	3	4.8	2	3	4.6	
t_{PLH}	CLKBA	A	2.5	4	6.3	2.6	4	6	ns
t_{PHL}			2.1	3.4	5.1	2.2	3.4	4.9	
t_{PLH}	CLKOUT	CLKIN	7.1	9.9	14.7	7.3	9.9	14.3	ns
t_{PHL}			5.8	8	11.6	6	8	11.5	
t_{en}	\overline{OEBA}	A or CLKIN	2.7	5.3	8.1	2.8	5.3	7.8	ns
t_{dis}			2.6	4.3	6.7	2.7	4.3	6.4	

† All typical values are at $V_{CC}(3.3\text{ V}) = 3.3\text{ V}$, $V_{CC}(5\text{ V}) = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

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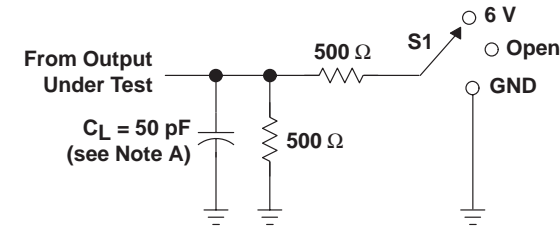
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SN54GTL16616, SN74GTL16616 17-BIT LVTTTL-TO-GTL/GTL+ UNIVERSAL BUS TRANSCEIVERS WITH BUFFERED CLOCK OUTPUTS

SCBS481F – JUNE 1994 – REVISED NOVEMBER 1999

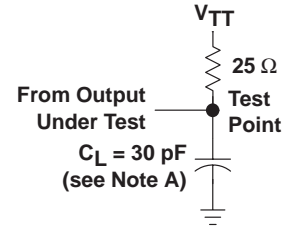
PARAMETER MEASUREMENT INFORMATION

$V_{TT} = 1.2\text{ V}$, $V_{REF} = 0.8\text{ V}$ FOR GTL AND $V_{TT} = 1.5\text{ V}$, $V_{REF} = 1\text{ V}$ FOR GTL+

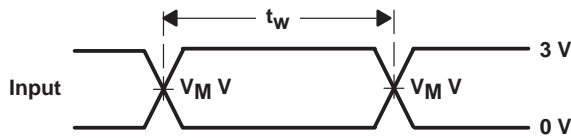


LOAD CIRCUIT FOR A OUTPUTS

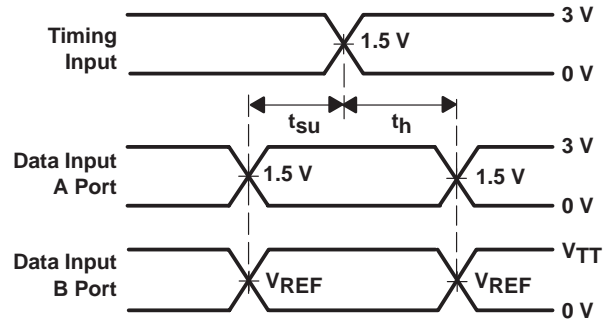
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



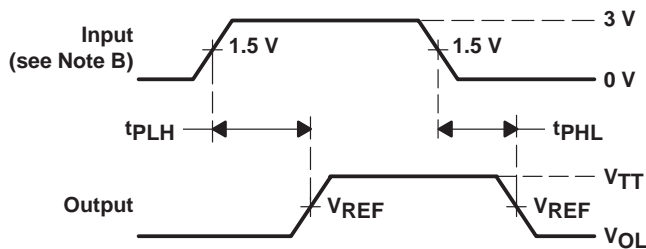
LOAD CIRCUIT FOR B OUTPUTS



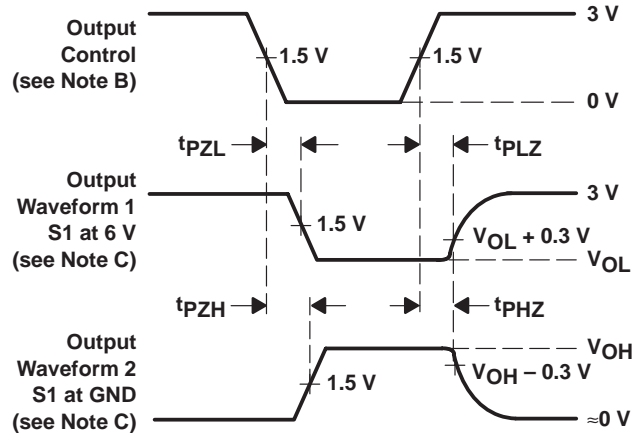
VOLTAGE WAVEFORMS
PULSE DURATION
($V_M = 1.5\text{ V}$ for A port and V_{REF} for B port)†



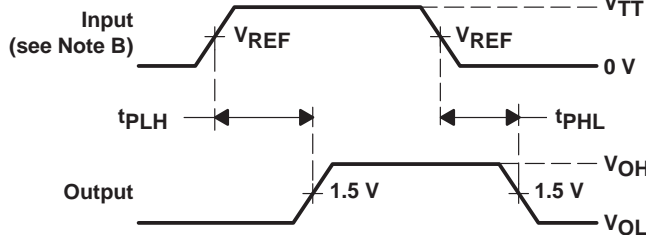
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)†



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port and CLKIN)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

† All control inputs are TTL levels.

NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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