REVISED DECEMBER 1983

- **Package Options Include Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These monolithic J-K flip-flops are negative-edge-triggered. They feature gated J-K inputs and an asynchronous clear input. The AND gate inputs are inhibited while the clock input is low; when the clock goes high, the inputs are enabled and data will be accepted. Logical state of J and K inputs may be allowed to change when the clock pulse is in a high state and bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative edge of the clock pulse.

The SN54H102 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74H102 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

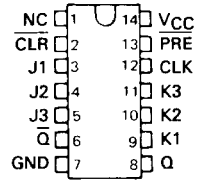
† This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

positive logic

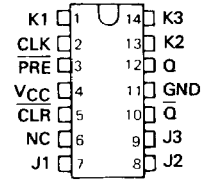
$$J = J1 \cdot J2 \cdot J3$$

$$K = K1 \cdot K2 \cdot K3$$

SN54H102 . . . J PACKAGE
SN74H102 . . . J OR N PACKAGE
(TOP VIEW)

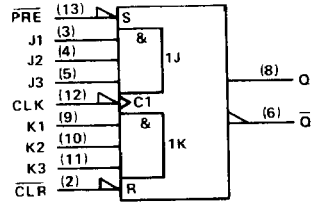


SN54H102 . . . W PACKAGE
(TOP VIEW)



NC – No internal connection

logic symbol

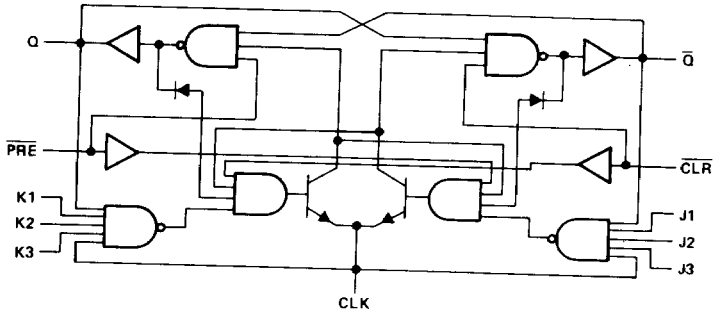


Pin numbers shown are for J and N packages.

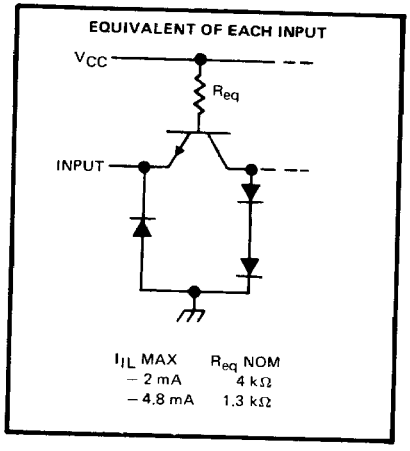
3 TTL DEVICES

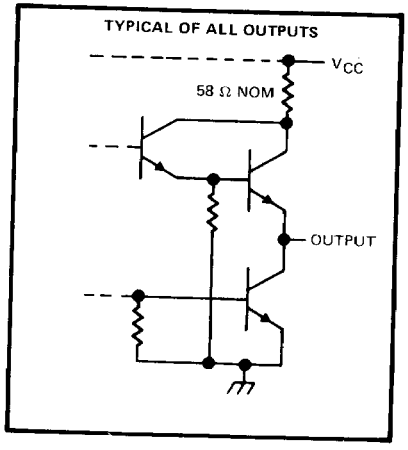
PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

logic diagram



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54H' . . . . . −55°C to 125°C
SN74H' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

TEXAS INSTRUMENTS
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recommended operating conditions

			SN54H102			SN74H102			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.5			−0.5	mA
I_{OL}	Low-level output current				20			20	mA
t_w	Pulse duration	CLK high	10			10			ns
		CLK low	15			15			
		$\overline{CLR}$ or $\overline{PRE}$ low	16			16			
t_{su}	Setup time before CLK↓	High-level data	10			10			ns
		Low-level data	13			13			
t_h	Hold time-data after CLK↓		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54H102			SN74H102			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −8 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = −0.5 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4		V
V_{OL}		V_{CC} = MIN, I_{OL} = 20 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,		0.2	0.4		0.2	0.4	V
I_I		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	Any J or K	V_{CC} = MAX,	V_I = 2.4 V				50			50	μA
	$\overline{CLR}$						100			100	
	$\overline{PRE}$						100			100	
	CLK				0		−1	0		−1	mA
I_{IL}	Any J or K	V_{CC} = MAX,	V_I = 0.4 V			−1	−2		−1	−2	mA
	$\overline{CLR}$					−1	−2		−1	−2	
	$\overline{PRE}$					−1	−2		−1	−2	
	CLK					−3	−4.8		−3	−4.8	
I_{OS}§		V_{CC} = MAX			−40		−100	−40		−100	mA
I_{CC}		V_{CC} = MAX,	See Note 2			20	38		20	38	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.
NOTE 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			R_L = 280 Ω, C_L = 25 pF	40	50		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$			8	12	ns
t_{PHL}	$\overline{PRE}$ or $\overline{CLR}$ (CLK high)	$\overline{Q}$ or Q			15	20	ns
	$\overline{PRE}$ or $\overline{CLR}$ (CLK low)				23	35	
t_{PLH}	CLK	Q or $\overline{Q}$			10	15	ns
t_{PHL}					16	20	

NOTE 3: See General Information Section for load circuits and voltage waveforms.