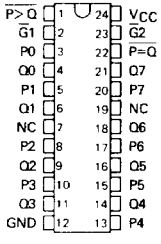
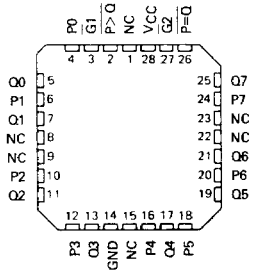
- Compares Two 8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 and 'LS683 have 20-kΩ Pullup Resistors on the Q Inputs
- 'LS686 and 'LS687 . . . New JT and NT 24-Pin, 3000-Mil Packages

TYPE	$\overline{P=Q}$	$\overline{P>Q}$	OUTPUT ENABLE	OUTPUT CONFIGURATION	20-kΩ PULLUP
'LS682	yes	yes	no	totem-pole	yes
'LS683	yes	yes	no	open-collector	yes
'LS684	yes	yes	no	totem-pole	no
'LS685	yes	yes	no	open-collector	no
'LS686	yes	yes	yes	totem-pole	no
'LS687	yes	yes	yes	open-collector	no
'LS688	yes	no	yes	totem-pole	no
'LS689	yes	no	yes	open-collector	no

SN54LS686, SN54LS687 . . . JT PACKAGE
SN74LS686, SN74LS687 . . . DW, JT OR NT PACKAGE
(TOP VIEW)

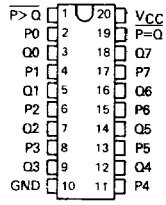


SN54LS686, SN54LS687 . . . FK PACKAGE
SN74LS686, SN74LS687 . . . FN PACKAGE
(TOP VIEW)

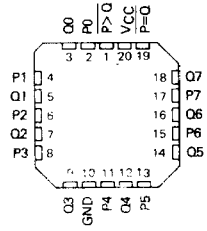


NC – No internal connection

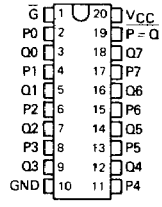
SN54LS682 THRU SN54LS685 . . . J PACKAGE
SN74LS682 THRU SN74LS685 . . . DW, J OR N PACKAGE
(TOP VIEW)



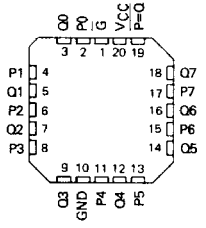
SN54LS682 THRU SN54LS685 . . . FK PACKAGE
SN74LS682 THRU SN74LS685 . . . FN PACKAGE
(TOP VIEW)



SN54LS688, SN54LS689 . . . J PACKAGE
SN74LS688, SN74LS689 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS688, SN54LS689 . . . FK PACKAGE
SN74LS688, SN74LS689 . . . FN PACKAGE
(TOP VIEW)



3 TTL DEVICES

description

These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide $\overline{P = Q}$ outputs and the 'LS682 thru 'LS687 provide $\overline{P > Q}$ outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS683, 'LS685, 'LS687, and 'LS689 have open-collector outputs. The 'LS682 and 'LS683 feature 20-kΩ pullup termination resistors on the Q inputs for analog or switch data.

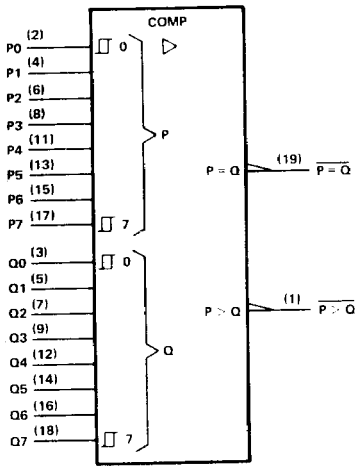
FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLES			
P, Q	$\overline{G}$, $\overline{G1}$	$\overline{G2}$	$\overline{P = Q}$	$\overline{P > Q}$
P = Q	L	X	L	H
P > Q	X	L	H	L
P < Q	X	X	H	H
P = Q	H	X	H	H
P > Q	X	H	H	H
X	H	H	H	H

NOTES: 1. The last three lines of the function table applies only to the devices having enable inputs, i.e., 'LS686 thru 'LS689.
2. The P < Q function can be generated by applying the P = Q and P > Q outputs to a 2-input NAND gate.
3. For 'LS686, 'LS687 G1 enables P = Q, and G2 enables P > Q.

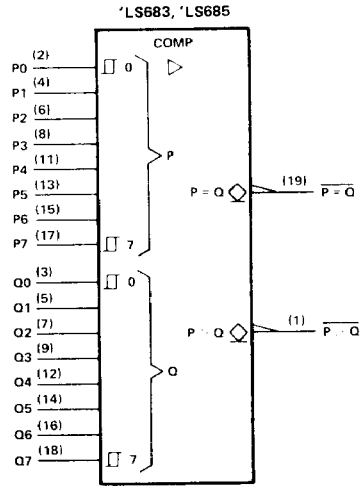
logic symbols

'LS682, 'LS684

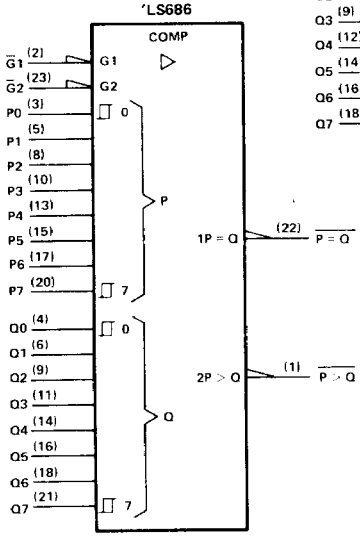


Pin numbers shown on logic notation are for DW, J, JT, N or NT packages.

'LS683, 'LS685



'LS686



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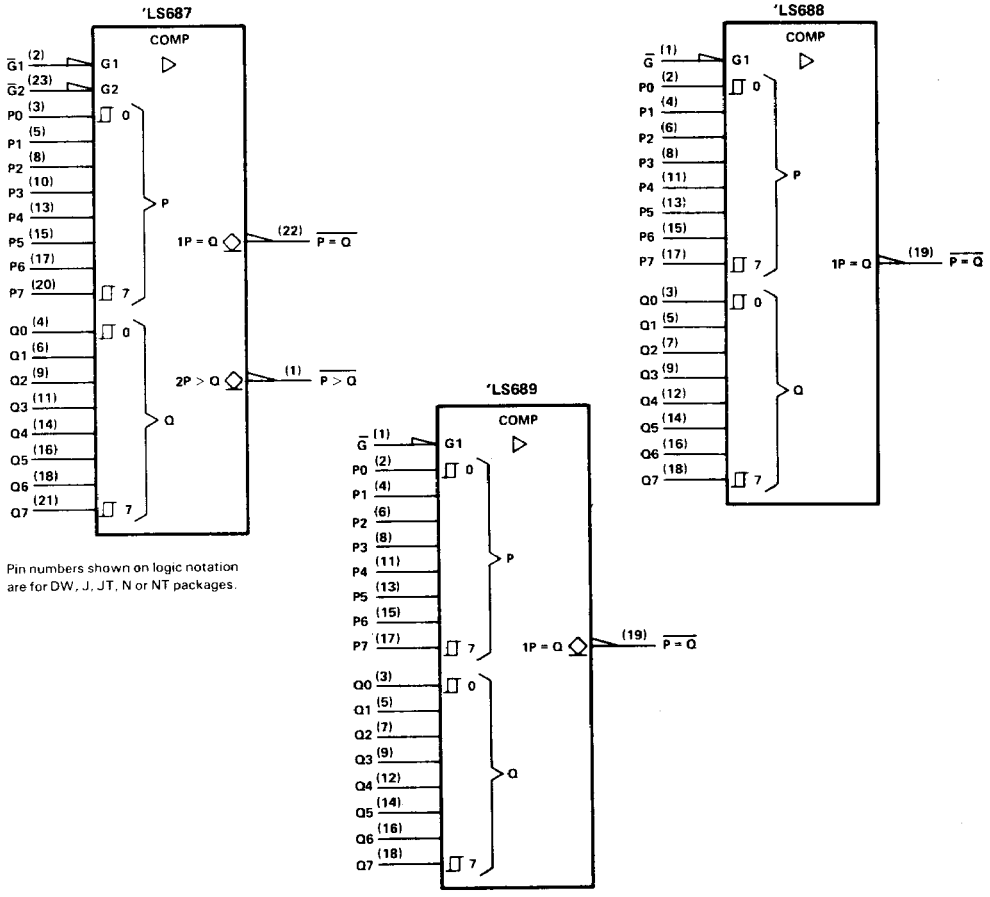
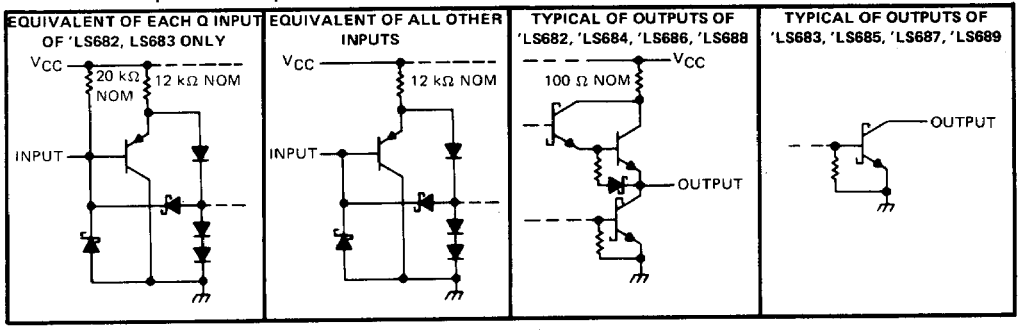
logic symbols (continued)

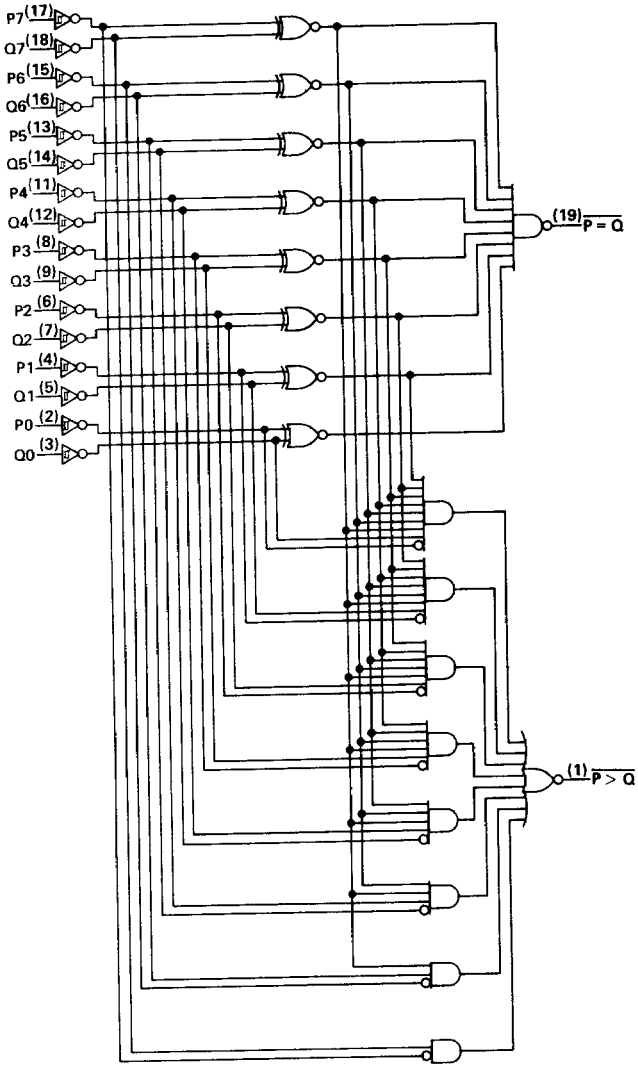


Pin numbers shown on logic notation are for DW, J, JT, N or NT packages.

schematics of inputs and outputs



'LS682 thru 'LS685 logic diagram (positive logic)



Pin numbers shown on logic notation are for DW, J or N packages

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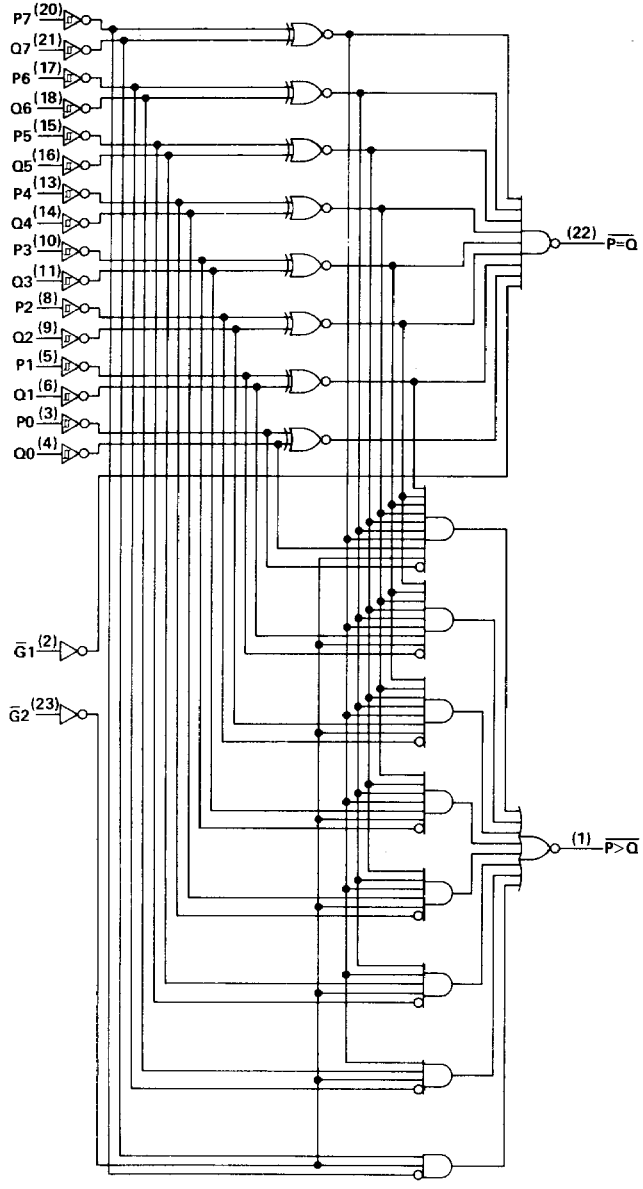
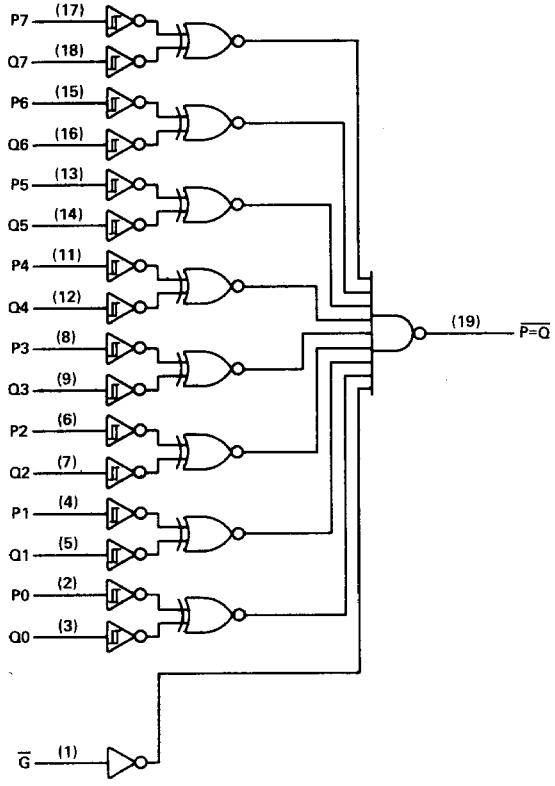
'LS686, 'LS687 logic diagram (positive logic)



Pin numbers shown on logic notation are for DW, JT, or NT packages.

'LS688, 'LS689 logic diagram (positive logic)



Pin numbers shown on logic notation are for DW, J or N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)		7 V
Input voltage: Q inputs of 'LS682 and 'LS683		5.5 V
All other inputs		7 V
Off-state output voltage: 'LS683, 'LS685, 'LS687, 'LS689		7 V
Operating free-air temperature range:	SN54LS682 thru SN54LS689	−55°C to 125°C
	SN74LS682 thru SN74LS689	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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'LS682, 'LS684, 'LS686, 'LS688

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs	V_{CC} = MIN			0.4			0.4		V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5			2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Q inputs, 'LS682	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		All other inputs	V_{CC} = MAX,	V_I = 7 V							
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Q inputs, 'LS682	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All other inputs					−0.2			−0.2	
I_{OS}§	Short-circuit output current		V_{CC} = MAX,	V_O = 0	−20		−100	−20		−100	mA
I_{CC}	Supply current	'LS682	V_{CC} = MAX,	See Note 2		42	70		42	70	mA
		'LS684				40	65		40	65	
		'LS686				44	75		44	75	
		'LS688				40	65		40	65	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with any $\overline{G}$ inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER#	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS682			'LS684			'LS686			'LS688			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	P	$\overline{P=Q}$	R_L = 667 Ω, C_L = 45 pF, All other inputs low, See Note 3		13	25		15	25		13	25		18	27	ns
t_{PHL}					15	25		17	25		20	30		20	30	
t_{PLH}	Q	$\overline{P=Q}$			14	25		16	25		13	25		18	27	ns
t_{PHL}					15	25		15	25		21	30		20	30	
t_{PLH}	$\overline{G}$, $\overline{G}1$	$\overline{P=Q}$									11	20		12	18	ns
t_{PHL}											19	30		13	20	
t_{PLH}	P	$\overline{P>Q}$			20	30		22	30		19	30				ns
t_{PHL}					15	30		17	30		15	30				
t_{PLH}	Q	$\overline{P>Q}$			21	30		24	30		18	30				ns
t_{PHL}					19	30		20	30		19	30				
t_{PLH}	$\overline{G}2$	$\overline{P>Q}$									21	30				ns
t_{PHL}											16	25				

#t_{PLH} ≡ propagation delay time, low-to-high-level outputs; t_{PHL} ≡ propagation delay time, high-to-low-level output.
NOTE 3: See General Information Section for load circuits and voltage waveforms.

recommended operating conditions 'LS683, 'LS685, 'LS687, 'LS689

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs	V_{CC} = MIN			0.4			0.4		V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_{OH} = 5.5 V			250			100	µA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Q inputs, 'LS683	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		All other inputs	V_{CC} = MAX,	V_I = 7 V							
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	µA
I_{IL}	Low-level input current	Q inputs, 'LS683	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All other inputs					−0.2			−0.2	
I_{CC}	Supply current	'LS683	V_{CC} = MAX,	See Note 2		42	70		42	70	mA
		'LS685				40	65		40	65	
		'LS687				44	75		44	75	
		'LS689				40	65		40	65	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with any $\overline{G}$ inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS683			'LS685			'LS687			'LS689			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	P	$\overline{P=Q}$	R_L = 667 Ω, C_L = 45 pF, All other inputs low, See Note 3		30	45		30	45		24	35		24	40	ns
t_{PHL}					20	30		19	35		20	30		22	35	
t_{PLH}	Q	$\overline{P=Q}$			24	35		24	45		24	35		24	40	ns
t_{PHL}					23	35		23	35		20	30		22	35	
t_{PLH}	$\overline{G}$, $\overline{G1}$	$\overline{P=Q}$									21	35		22	35	ns
t_{PHL}											18	30		19	30	
t_{PLH}	P	$P > \overline{Q}$			31	45		32	45		24	35				ns
t_{PHL}					17	30		16	35		16	30				
t_{PLH}	Q	$P > \overline{Q}$			30	45		30	45		24	35				ns
t_{PHL}					21	30		20	35		16	30				
t_{PLH}	$\overline{G2}$	$\overline{P} > \overline{Q}$									24	35				ns
t_{PHL}											15	30				

¶ t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output.
NOTE 3: See General Information Section for load circuits and voltage waveforms.

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