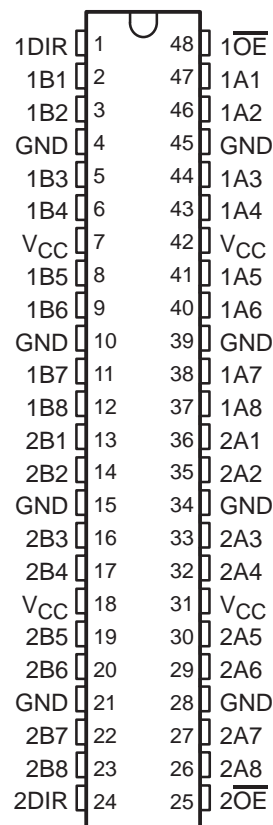


# SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS260K – JUNE 1993 – REVISED APRIL 1999

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- A-Port Outputs Have Equivalent 22- $\Omega$  Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH162245 . . . WD PACKAGE  
SN74LVTH162245 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## description

The 'LVTH162245 devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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## description (continued)

The A-port outputs, which are designed to source or sink up to 12 mA, include equivalent 22- $\Omega$  series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH162245 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LVTH162245 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

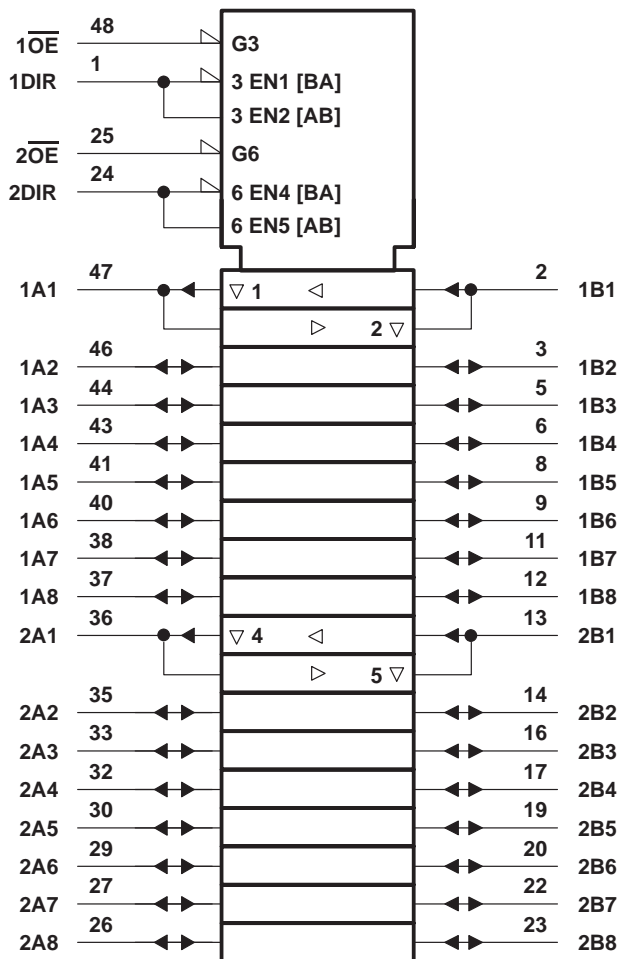
**FUNCTION TABLE**  
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

# SN54LVTH162245, SN74LVTH162245 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

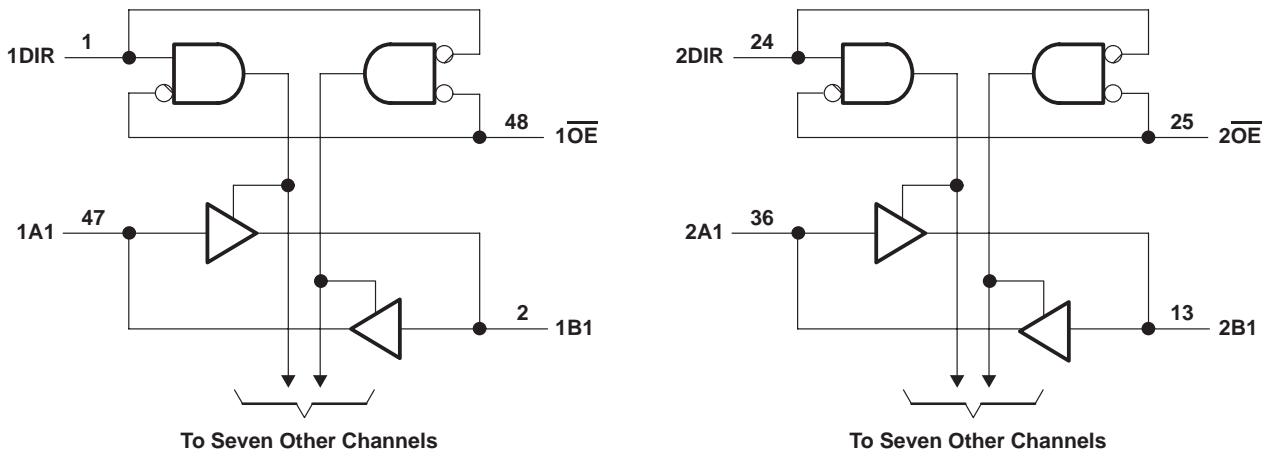
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



# SN54LVTH162245, SN74LVTH162245

## 3.3-V ABT 16-BIT BUS TRANSCEIVERS

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_O$ : SN54LVTH162245 (B port) .....	96 mA
SN74LVTH162245 (B port) .....	128 mA
A port .....	30 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH162245 (B port) .....	48 mA
SN74LVTH162245 (B port) .....	64 mA
A port .....	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package .....	89°C/W
DL package .....	94°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JESD 51.

#### recommended operating conditions (see Note 4)

		SN54LVTH162245		SN74LVTH162245		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current	A port		-12		mA
		B port		-24		
$I_{OL}$	Low-level output current	A port		12		mA
		B port		48		
$\Delta t/\Delta v$	Input transition rise or fall rate			10		ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu$ s/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



**SN54LVTH162245, SN74LVTH162245**  
**3.3-V ABT 16-BIT BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	SN54LVTH162245		SN74LVTH162245		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V <sub>IK</sub>		V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = -18 mA	-1.2		-1.2		V	
V <sub>OH</sub>	A port	V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OH</sub> = -100 μA	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		V	
		V <sub>CC</sub> = 3 V, I <sub>OH</sub> = -12 mA	2		2			
	B port	V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OH</sub> = -100 μA	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2			
		V <sub>CC</sub> = 2.7 V, I <sub>OH</sub> = -8 mA	2.4		2.4			
		V <sub>CC</sub> = 3 V	I <sub>OH</sub> = -24 mA	2				
I <sub>OH</sub> = -32 mA			2					
V <sub>OL</sub>	A port	V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OL</sub> = 100 μA	0.2		0.2		V	
		V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 12 mA	0.8		0.8			
	B port	V <sub>CC</sub> = 2.7 V	I <sub>OL</sub> = 100 μA	0.2		0.2		
			I <sub>OL</sub> = 24 mA	0.5		0.5		
		V <sub>CC</sub> = 3 V	I <sub>OL</sub> = 16 mA	0.4		0.4		
			I <sub>OL</sub> = 32 mA	0.5		0.5		
			I <sub>OL</sub> = 48 mA	0.55		0.55		
			I <sub>OL</sub> = 64 mA			0.55		
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND	±1		±1		μA	
		V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V	10		10			
	A or B ports‡	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = 5.5 V	20		20			
		V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub>	5		5			
		V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = 0	-10		-10			
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V			±100		μA		
I <sub>I</sub> (hold)	A or B ports	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0.8 V	75		75		μA
			V <sub>I</sub> = 2 V	-75		-75		
		V <sub>CC</sub> = 3.6 V§, V <sub>I</sub> = 0 to 3.6 V			500		-750	
I <sub>OZPU</sub>	V <sub>CC</sub> = 0 to 1.5 V, V <sub>O</sub> = 0.5 V to 3 V, OE = don't care		±100*		±100		μA	
I <sub>OZPD</sub>	V <sub>CC</sub> = 1.5 V to 0, V <sub>O</sub> = 0.5 V to 3 V, OE = don't care		±100*		±100		μA	
I <sub>CC</sub>	V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high	0.19		0.19		mA	
		Outputs low	5		5			
		Outputs disabled	0.19		0.19			
ΔI <sub>CC</sub> ¶	V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND		0.3		0.2		mA	
C <sub>i</sub>	V <sub>I</sub> = 3 V or 0		4		4		pF	
C <sub>io</sub>	V <sub>O</sub> = 3 V or 0		10		10		pF	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ Unused pins at V<sub>CC</sub> or GND.

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



**SN54LVTH162245, SN74LVTH162245**  
**3.3-V ABT 16-BIT BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

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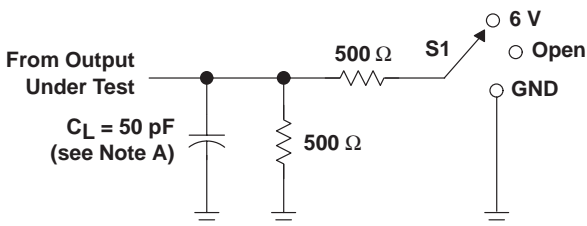
switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162245				SN74LVTH162245				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
$t_{PLH}$	A	B	1	3.5	4		1	2.3	3.3	3.7		ns
$t_{PHL}$			1	3.5	3.9		1	2.2	3.3	3.5		
$t_{PLH}$	B	A	1	4.3	5.3		1	2.8	4	4.6		ns
$t_{PHL}$			1	4.2	4.5		1	2.5	3.4	3.6		
$t_{PZH}$	$\overline{OE}$	B	1	4.8	5.9		1	2.8	4.6	5.4		ns
$t_{PZL}$			1	4.8	5.5		1	3	4.6	5.2		
$t_{PZH}$	$\overline{OE}$	A	1	5.5	7.2		1	3.3	5.3	6.3		ns
$t_{PZL}$			1	5.4	6.4		1	3.3	5.1	5.8		
$t_{PHZ}$	$\overline{OE}$	B	1.5	5.5	5.8		1.5	3.8	5.2	5.5		ns
$t_{PLZ}$			1.5	5.5	5.8		1.5	3.5	5.1	5.4		
$t_{PHZ}$	$\overline{OE}$	A	1.5	5.8	6.5		1.5	4	5.6	5.9		ns
$t_{PLZ}$			1.2	6.3	6.3		1.5	3.8	5.5	5.5		
$t_{sk(o)}$								0.5			ns	

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

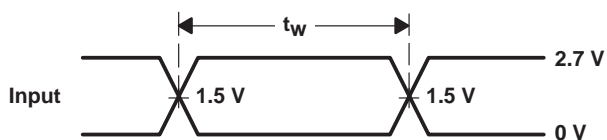


PARAMETER MEASUREMENT INFORMATION

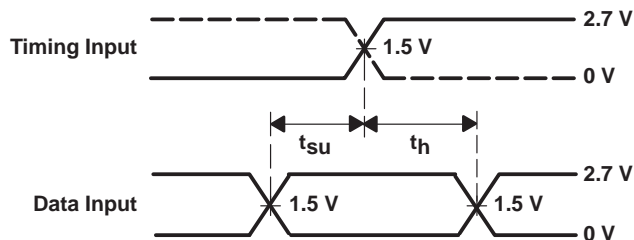


LOAD CIRCUIT

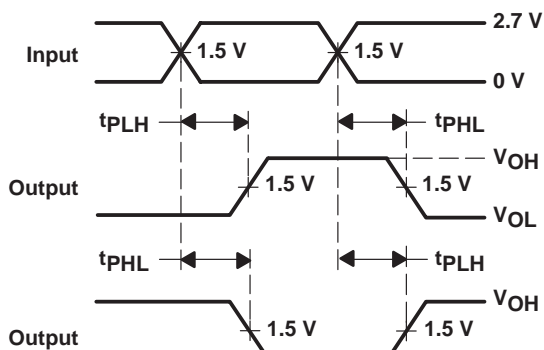
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



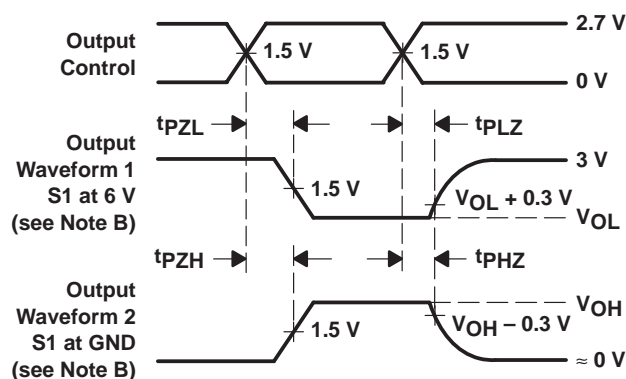
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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