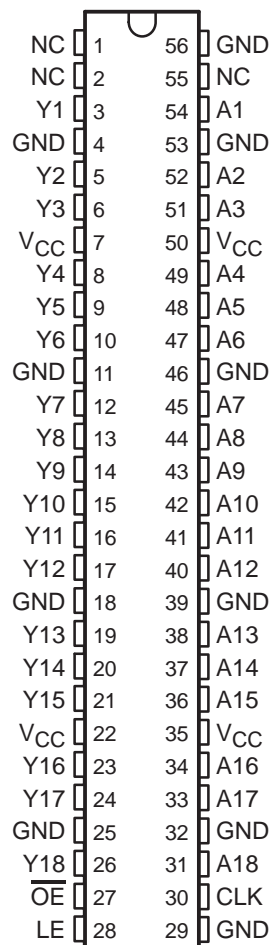


# SN54LVTH16835, SN74LVTH16835 3.3-V ABT 18-BIT UNIVERSAL BUS DRIVERS WITH 3-STATE OUTPUTS

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- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **$I_{off}$  and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )**
- **Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54LVTH16835 . . . WD PACKAGE  
SN74LVTH16835 . . . DGG OR DL PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

The LVTH16835 devices are 18-bit universal bus drivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

Data flow from A to Y is controlled by the output-enable ( $\overline{OE}$ ) input. These devices operate in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of the clock. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



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 **TEXAS  
INSTRUMENTS**

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# SN54LVTH16835, SN74LVTH16835

## 3.3-V ABT 18-BIT UNIVERSAL BUS DRIVERS

### WITH 3-STATE OUTPUTS

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#### description (continued)

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH16835 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LVTH16835 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{\text{OE}}$	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	$Y_0^{\dagger}$
L	L	L	X	$Y_0^{\ddagger}$

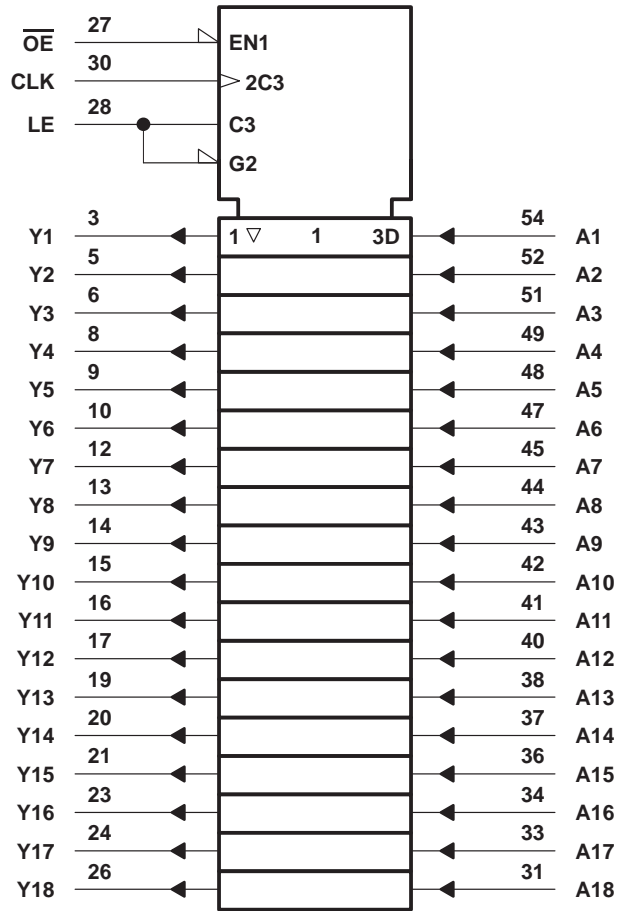
† Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes low

‡ Output level before the indicated steady-state input conditions were established

SN54LVTH16835, SN74LVTH16835  
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WITH 3-STATE OUTPUTS

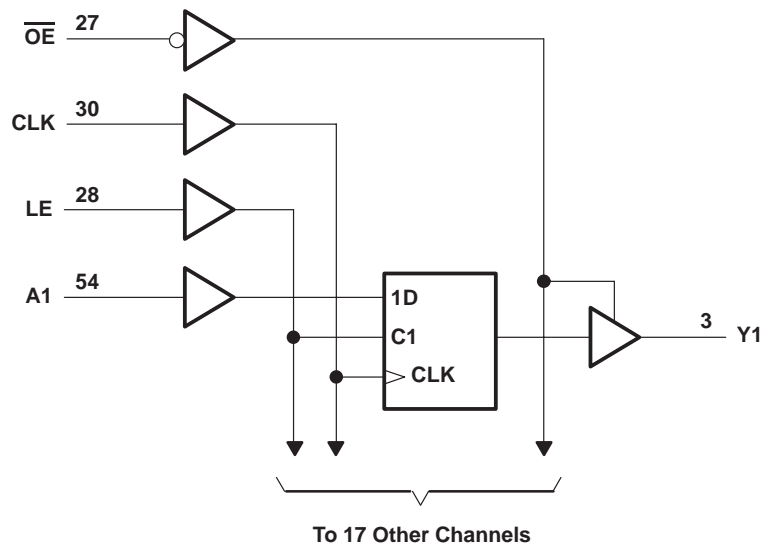
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



# SN54LVTH16835, SN74LVTH16835

## 3.3-V ABT 18-BIT UNIVERSAL BUS DRIVERS

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_O$ : SN54LVTH16835 .....	96 mA
SN74LVTH16835 .....	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH16835 .....	48 mA
SN74LVTH16835 .....	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package .....	81°C/W
DL package .....	74°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JESD 51.

#### recommended operating conditions (see Note 4)

		SN54LVTH16835		SN74LVTH16835		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		SN54LVTH16835		SN74LVTH16835		UNIT	
				MIN	TYP†	MAX	MIN		TYP†
$V_{IK}$		$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$		-1.2		-1.2		V	
$V_{OH}$		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$		$V_{CC}-0.2$		V	
		$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$		2.4		2.4			
		$V_{CC} = 3\text{ V}$		2		2			
		$I_{OH} = -24\text{ mA}$							
				$I_{OH} = -32\text{ mA}$					
$V_{OL}$		$V_{CC} = 2.7\text{ V}$		$I_{OL} = 100\text{ }\mu\text{A}$		0.2		0.2	
				$I_{OL} = 24\text{ mA}$		0.5		0.5	
		$V_{CC} = 3\text{ V}$		$I_{OL} = 16\text{ mA}$		0.4		0.4	
				$I_{OL} = 32\text{ mA}$		0.5		0.5	
				$I_{OL} = 48\text{ mA}$		0.55			
				$I_{OL} = 64\text{ mA}$				0.55	
$I_I$		Control inputs $V_{CC} = 0\text{ or }3.6\text{ V}$ , $V_I = 5.5\text{ V}$ $V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$		10		10		$\mu\text{A}$	
				A inputs $V_{CC} = 3.6\text{ V}$		$\pm 1$			$\pm 1$
$V_I = V_{CC}$		1				1			
$V_I = 5.5\text{ V}$		10				10			
				$V_I = 0$		-5		-5	
$I_{off}$		$V_{CC} = 0$ , $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$				$\pm 100$		$\mu\text{A}$	
$I_I(\text{hold})$		$V_{CC} = 3\text{ V}$		$V_I = 0.8\text{ V}$		75		$\mu\text{A}$	
				$V_I = 2\text{ V}$		-75			-75
		$V_{CC} = 3.6\text{ V}\ddagger$ , $V_I = 0\text{ to }3.6\text{ V}$							$\pm 500$
$I_{OZH}$		$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$		5		5		$\mu\text{A}$	
$I_{OZL}$		$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$		-5		-5		$\mu\text{A}$	
$I_{OZPU}$		$V_{CC} = 0\text{ to }1.5\text{ V}$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $OE = \text{don't care}$		$\pm 100^*$		$\pm 100$		$\mu\text{A}$	
$I_{OZPD}$		$V_{CC} = 1.5\text{ V to }0$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $OE = \text{don't care}$		$\pm 100^*$		$\pm 100$		$\mu\text{A}$	
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$		Outputs high		0.19		0.19	
				Outputs low		5		5	
				Outputs disabled		0.19		0.19	
$\Delta I_{CC}\S$		$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$		0.2		0.2		mA	
$C_i$		$V_I = 3\text{ V or }0$		3.5		3.5		pF	
$C_o$		$V_O = 3\text{ V or }0$		9		9		pF	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

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**WITH 3-STATE OUTPUTS**

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

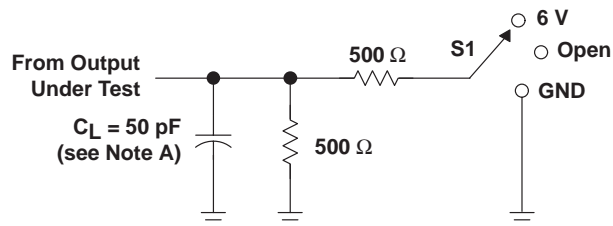
		SN54LVTH16835				SN74LVTH16835				UNIT		
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$				
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
$f_{\text{clock}}$	Clock frequency	150		150		150		150		MHz		
$t_w$	Pulse duration	LE high		3.3		3.3		3.3		ns		
		CLK high or low		3.3		3.3		3.3				
$t_{\text{su}}$	Setup time	Data before CLK $\uparrow$		2.2		2.5		2.1		2.4		
		Data before LE $\downarrow$	CLK high		2.5		1.7		2.3		1.5	
			CLK low		1.5		0.5		1.5		0.5	
$t_h$	Hold time	Data after CLK $\uparrow$		1		0		1		0		
		Data after LE $\downarrow$		0.8		0.8		0.8		0.8		

switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16835				SN74LVTH16835				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP $\dagger$	MAX	MIN		MAX
$f_{\text{max}}$			150		150		150			150		MHz
$t_{\text{PLH}}$	A	Y	1.2	3.9	4.3		1.3	2.6	3.7	4		ns
$t_{\text{PHL}}$			1.2	3.9	4.3		1.3	2.4	3.7	4		
$t_{\text{PLH}}$	LE	Y	1.4	5.3	5.9		1.5	3.2	5.1	5.7		ns
$t_{\text{PHL}}$			1.4	5.3	5.9		1.5	3.3	5.1	5.7		
$t_{\text{PLH}}$	CLK	Y	1.4	5.3	5.9		1.5	3.5	5.1	5.7		ns
$t_{\text{PHL}}$			1.4	5.3	5.9		1.5	3.4	5.1	5.7		
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Y	1.2	5	5.9		1.3	2.9	4.6	5.5		ns
$t_{\text{PZL}}$			1.2	5	5.9		1.3	3	4.6	5.5		
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Y	1.6	6	6.5		1.7	4.2	5.8	6.3		ns
$t_{\text{PLZ}}$			1.6	6	6.5		1.7	3.7	5.8	6.3		

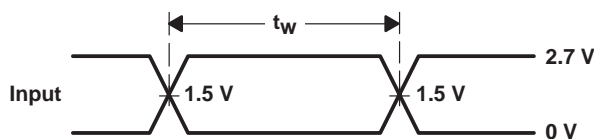
$\dagger$  All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

PARAMETER MEASUREMENT INFORMATION

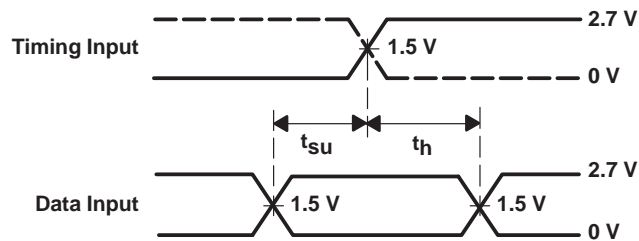


LOAD CIRCUIT

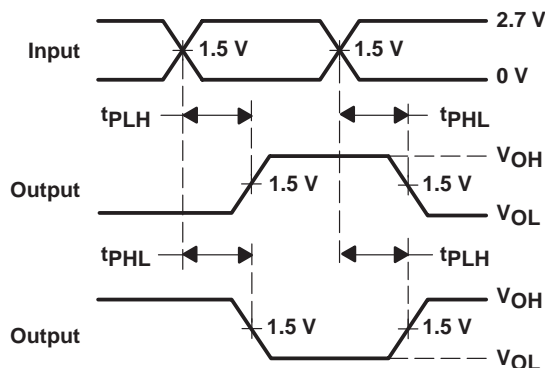
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



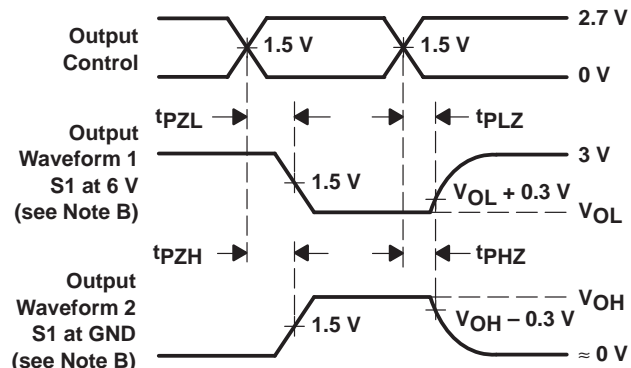
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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