

SN54LVTH2952, SN74LVTH2952 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS710D – OCTOBER 1997 – REVISED APRIL 1999

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus-Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages, Ceramic Chip Carriers (FK), and Ceramic (JT) DIPs

description

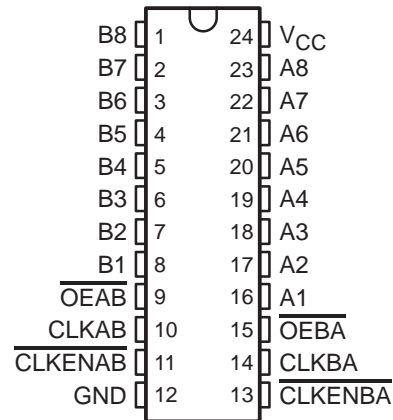
These octal bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTH2952 devices consist of two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Data on the A or B bus is stored in the registers on the low-to-high transition of the clock (CLKAB or CLKBA) input, provided that the clock-enable ($\overline{\text{CLKENAB}}$ or $\overline{\text{CLKENBA}}$) input is low. Taking the output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) input low accesses the data on either port.

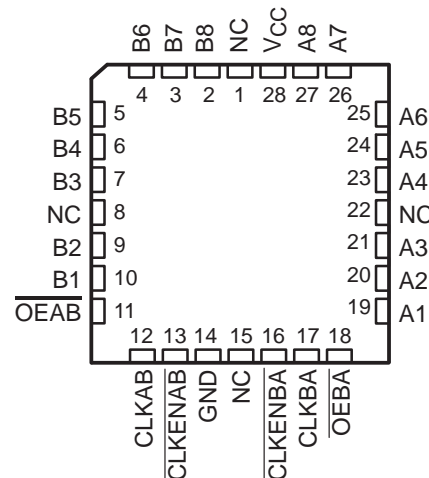
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54LVTH2952 . . . JT PACKAGE
SN74LVTH2952 . . . DB, DGV, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH2952 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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 **TEXAS
INSTRUMENTS**

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description (continued)

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH2952 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTH2952 is characterized for operation from -40°C to 85°C .

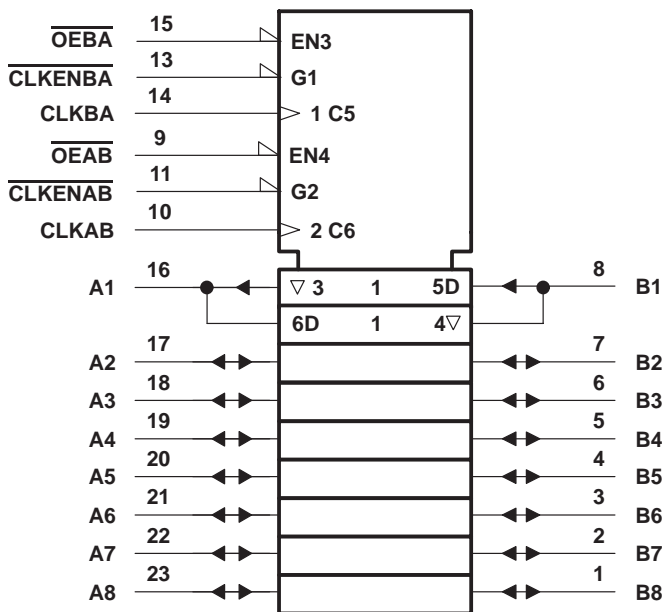
FUNCTION TABLE†

INPUTS				OUTPUT
CLKENAB	CLKAB	OEAB	A	B
H	X	L	X	B_0^{\ddagger}
X	H or L	L	X	B_0^{\ddagger}
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established

logic symbols§



§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DGV, DW, JT, and PW packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, I_O : SN54LVTH2952	96 mA
SN74LVTH2952	128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH2952	48 mA
SN74LVTH2952	64 mA
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	104°C/W
DGV package	139°C/W
DW package	81°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

		SN54LVTH2952		SN74LVTH2952		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage		5.5		5.5	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		µs/V
T_A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH2952		SN74LVTH2952		UNIT		
				MIN	TYP†	MAX	MIN		TYP†	MAX
V _{IK}		V _{CC} = 2.7 V, I _I = -18 mA		-1.2		-1.2		V		
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OH} = -100 μA		V _{CC} -0.2		V _{CC} -0.2		V		
		V _{CC} = 2.7 V, I _{OH} = -8 mA		2.4		2.4				
		V _{CC} = 3 V		2		2				
V _{OL}		V _{CC} = 2.7 V		I _{OL} = 100 μA		0.2		V		
				I _{OL} = 24 mA		0.5				
		V _{CC} = 3 V		I _{OL} = 16 mA		0.4				
				I _{OL} = 32 mA		0.5				
				I _{OL} = 48 mA		0.55				
				I _{OL} = 64 mA		0.55				
I _I		V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1		±1		μA		
		Control inputs		V _{CC} = 0 or 3.6 V, V _I = 5.5 V		10			10	
		A or B ports‡		V _{CC} = 3.6 V, V _I = 5.5 V		20			20	
				V _{CC} = 3.6 V, V _I = V _{CC}		1			1	
		V _{CC} = 3.6 V, V _I = 0		-5		-5				
I _{off}		V _{CC} = 0, V _I or V _O = 0 to 4.5 V				±100		μA		
I _I (hold)		V _{CC} = 3 V		V _I = 0.8 V		75		μA		
				V _I = 2 V		-75				
		V _{CC} = 3.6 V§, V _I = 0 to 3.6 V				±500				
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care		±100*		±100		μA		
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care		±100*		±100		μA		
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		0.19		mA		
				Outputs low		5				
				Outputs disabled		0.19				
ΔI _{CC} ¶		V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND		0.2		0.2		mA		
C _i		V _I = 3 V or 0		4		4		pF		
C _{io}		V _O = 3 V or 0		9		9		pF		

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ Unused terminals at V_{CC} or GND

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirement over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVTH2952				SN74LVTH2952				UNIT
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	150		150		150		150		MHz
t_w	Pulse duration	CLK high	3.3	3.3	3.3	3.3	3.3	3.3	3.3	ns
		CLK low	3.3	3.3	3.3	3.3	3.3	3.3	3.3	
t_{su}	Setup time	A or B before CLK \uparrow	Data high	1.6	2.2	1.5	2.1	1.5	2.1	ns
			Data low	1.6	2.2	1.5	2.1	1.5	2.1	
	$\overline{\text{CE}}$ before CLK \uparrow	Data high	1.6	1.9	1.5	1.8	1.5	1.8		
		Data low	2	2.6	1.9	2.5	1.9	2.5		
t_h	Hold time	A or B after CLK \uparrow	1	0.2	1	0.2	1	0.2	ns	
		$\overline{\text{CE}}$ after CLK \uparrow	1.2	0.2	1.2	0.2	1.2	0.2		

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

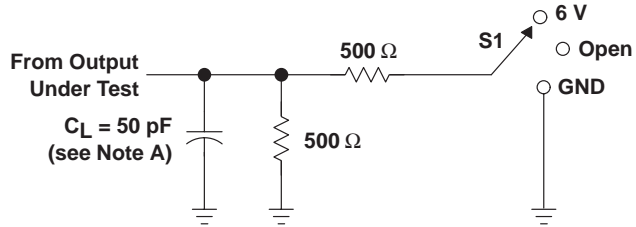
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH2952				SN74LVTH2952				UNIT	
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$			
			MIN	MAX	MIN	MAX	MIN	TYP \dagger	MAX	MIN		MAX
f_{max}			150		150		150		150		MHz	
t_{PLH}	CLKBA or CLKAB	A or B	1.2	4.8	5.5		1.3	2.9	4.6	5.3		ns
t_{PHL}			1.2	4.8	5.5		1.3	3.1	4.6	5.3		
t_{PZH}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	1	4.8	5.9		1.1	2.6	4.6	5.8		ns
t_{PZL}			1	4.8	5.9		1.1	3	4.6	5.8		
t_{PHZ}	$\overline{\text{OEBA}}$ or $\overline{\text{OEAB}}$	A or B	1.2	5.6	6		1.3	3.6	5.4	5.9		ns
t_{PLZ}			1.5	5.4	5.6		1.6	3.6	5.1	5.3		

\dagger All typical values are at $T_A = 25^\circ\text{C}$.

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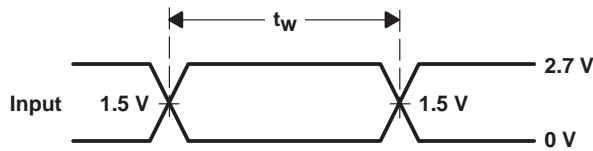
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PARAMETER MEASUREMENT INFORMATION

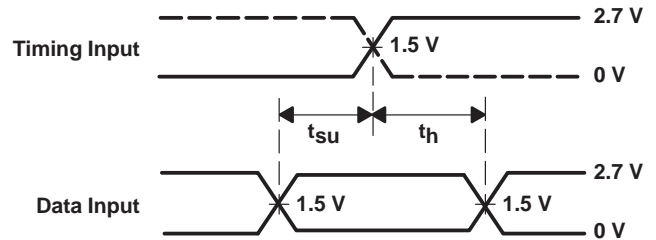


LOAD CIRCUIT FOR OUTPUTS

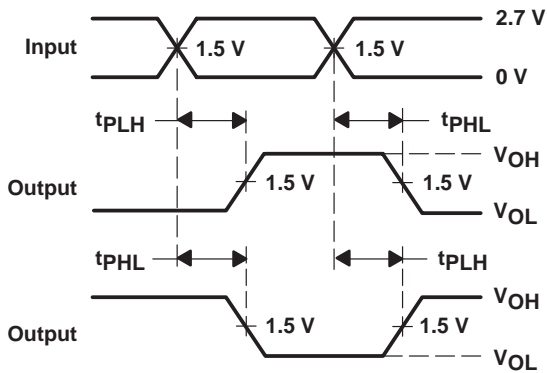
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



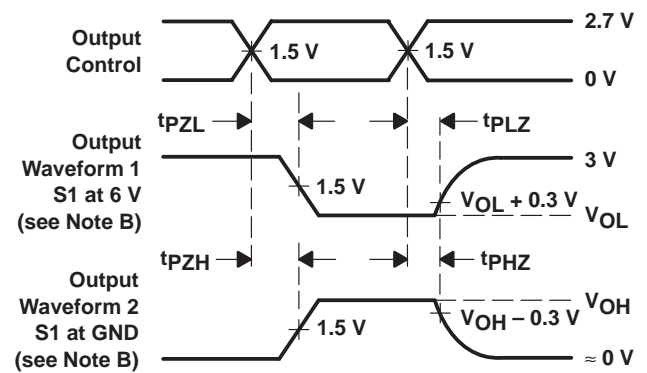
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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