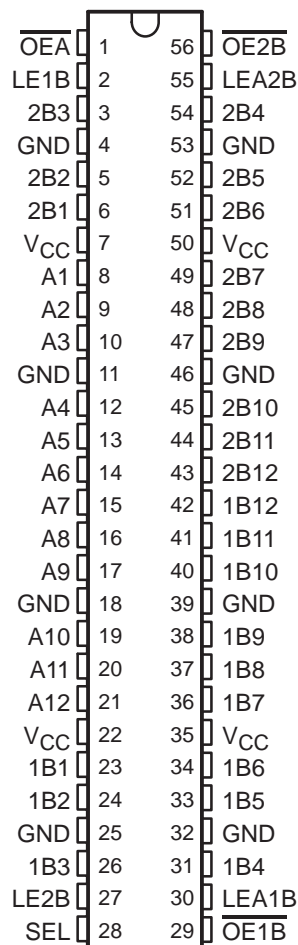


# SN54ABTH162260, SN74ABTH162260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH SERIES-DAMPING RESISTORS AND 3-STATE OUTPUTS

SCBS240D – JUNE 1992 – REVISED MAY 1997

- **Members of the Texas Instruments Widebus™ Family**
- **B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required**
- **State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V<sub>OLP</sub> (Output Ground Bounce) < 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **Distributed V<sub>CC</sub> and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

SN54ABTH162260 . . . WD PACKAGE  
SN74ABTH162260 . . . DL PACKAGE  
(TOP VIEW)



## description

The 'ABTH162260 are 12-bit to 24-bit multiplexed D-type latches used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. These devices are also useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable ( $\overline{OE1B}$ ,  $\overline{OE2B}$ , and  $\overline{OEA}$ ) inputs control the bus-transceiver functions. The  $\overline{OE1B}$  and  $\overline{OE2B}$  control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

The B-port outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.



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 **TEXAS  
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**SN54ABTH162260, SN74ABTH162260**  
**12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES**  
**WITH SERIES-DAMPING RESISTORS AND 3-STATE OUTPUTS**

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**description (continued)**

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABTH162260 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ABTH162260 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**Function Tables**

**B TO A ( $\overline{OEB} = \text{H}$ )**

INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\overline{OEA}$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A <sub>0</sub>
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A <sub>0</sub>
X	X	X	X	X	H	Z

**A TO B ( $\overline{OEA} = \text{H}$ )**

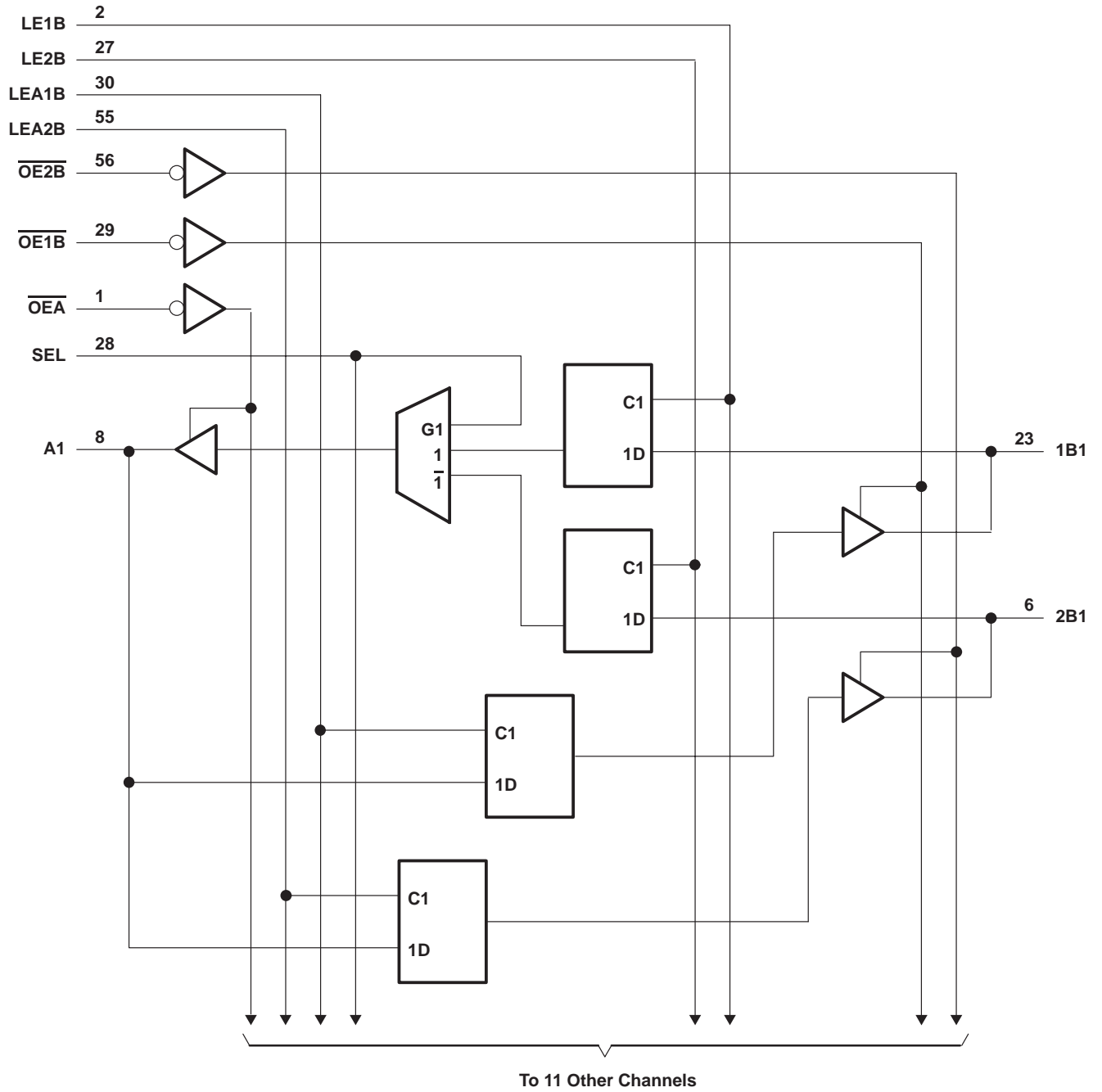
INPUTS					OUTPUTS	
A	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	2B <sub>0</sub>
L	H	L	L	L	L	2B <sub>0</sub>
H	L	H	L	L	1B <sub>0</sub>	H
L	L	H	L	L	1B <sub>0</sub>	L
X	L	L	L	L	1B <sub>0</sub>	2B <sub>0</sub>
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active



**SN54ABTH162260, SN74ABTH162260**  
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**logic diagram (positive logic)**



# SN54ABTH162260, SN74ABTH162260

## 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES

### WITH SERIES-DAMPING RESISTORS AND 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABTH162260 (A port)	96 mA
SN74ABTH162260 (A port)	128 mA
B port	30 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DL package	74°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

#### recommended operating conditions (see Note 3)

		SN54ABTH162260		SN74ABTH162260		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current	A port	48		64	mA
		B port	12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

**SN54ABTH162260, SN74ABTH162260**  
**12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES**  
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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABTH162260		SN74ABTH162260		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA			2.5		2.5		2.5	V
		V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA			3		3		3	
		V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA			2		2		
									2	
V <sub>OL</sub>	A port	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA				0.55		0.55	V
			I <sub>OL</sub> = 64 mA				0.55*		0.55	
	B port		I <sub>OL</sub> = 12 mA				0.8		0.8	
V <sub>hys</sub>					100					mV
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±1		±1		±1	μA
	A or B ports	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND			±20		±20		±20	
I <sub>I</sub> (hold)	A or B ports	V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0.8 V						100	μA
			V <sub>I</sub> = 2 V						-100	
I <sub>OZPU</sub> ‡		V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I <sub>OZPD</sub> ‡		V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I <sub>OZH</sub> §		V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V			10		10		10	μA
I <sub>OZL</sub> §		V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V			-10		-10		-10	μA
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V			±100				±100	μA
I <sub>CEX</sub>	Outputs high	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V			50		50		50	μA
I <sub>O</sub> ¶		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V	-50	-100	-225	-50	-225	-50	-225	mA
I <sub>CC</sub>	Outputs high	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND			1.5		1.5		1.5	mA
	Outputs low				63		63		63	
	Outputs disabled				1		1		1	
ΔI <sub>CC</sub> #		V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			1		1.5		1	mA
C <sub>i</sub>		V <sub>I</sub> = 2.5 V or 0.5 V			3					pF
C <sub>o</sub>		V <sub>O</sub> = 2.5 V or 0.5 V			11.5					pF

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ This parameter is characterized but not tested.

§ The parameters I<sub>OZH</sub> and I<sub>OZL</sub> include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

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**SN54ABTH162260, SN74ABTH162260**  
**12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES**  
**WITH SERIES-DAMPING RESISTORS AND 3-STATE OUTPUTS**

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54ABTH162260		SN74ABTH162260		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1.5		1.5		1.5		ns
t <sub>h</sub>	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		1		1		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C			SN54ABTH162260		SN74ABTH162260		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	B	1.4	3.6	5.2	1.4	6.3	1.4	6.1	ns
t <sub>PHL</sub>			2.7	4.8	6.4	2.7	7.4	2.7	7.1	
t <sub>PLH</sub>	B	A	1.6	3.6	5.2	1.6	6.4	1.6	6	ns
t <sub>PHL</sub>			1.7	3.8	5.5	1.7	6.5	1.7	6.2	
t <sub>PLH</sub>	LE	A	1.8	3.9	5.3	1.8	6.6	1.8	6.3	ns
t <sub>PHL</sub>			2.3	4.1	5.4	2.3	6.1	2.3	5.8	
t <sub>PLH</sub>	LE	B	1.6	3.7	5.4	1.6	6.4	1.6	6.1	ns
t <sub>PHL</sub>			2.8	4.9	6.4	2.8	7.5	2.8	7.1	
t <sub>PLH</sub>	SEL (1B)	A	1.5	3.6	5	1.5	5.9	1.5	5.6	ns
t <sub>PHL</sub>			1.8	3.5	4.8	1.8	5.2	1.8	5	
t <sub>PLH</sub>	SEL (2B)	A	1.2	3.6	5.1	1.2	6.5	1.2	6.3	ns
t <sub>PHL</sub>			1.7	4	5.5	1.7	6.5	1.7	6.2	
t <sub>PZH</sub>	$\overline{OE}$	A	1.1	3.5	5.2	1.1	6.5	1.1	6.3	ns
t <sub>PZL</sub>			2.1	4.2	5.7	2.1	6.6	2.1	6.5	
t <sub>PZH</sub>	$\overline{OE}$	B	1	3.4	4.9	1	6.4	1	6.3	ns
t <sub>PZL</sub>			2.9	5.5	6.8	2.9	8.3	2.9	8.2	
t <sub>PHZ</sub>	$\overline{OE}$	A	2.5	4.5	5.9	2.5	6.9	2.5	6.7	ns
t <sub>PLZ</sub>			1.8	3.4	4.8	1.8	5.6	1.8	5.2	
t <sub>PHZ</sub>	$\overline{OE}$	B	2.1	4.4	5.7	2.1	7.7	2.1	7.5	ns
t <sub>PLZ</sub>			1.7	3.9	5.4	1.7	6.3	1.7	6.2	

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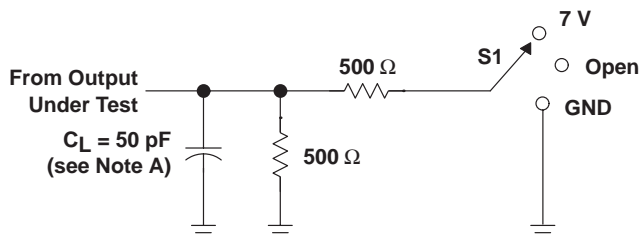


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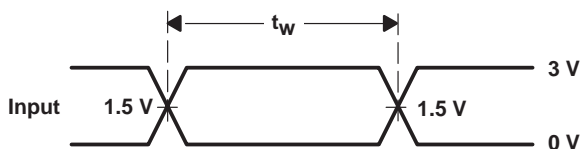
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**PARAMETER MEASUREMENT INFORMATION**

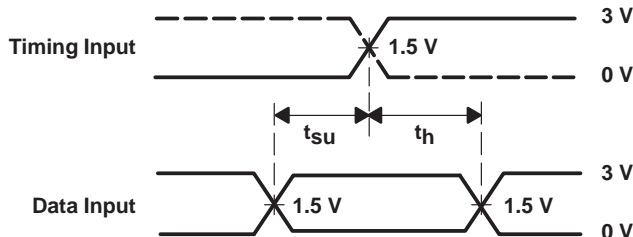


**LOAD CIRCUIT**

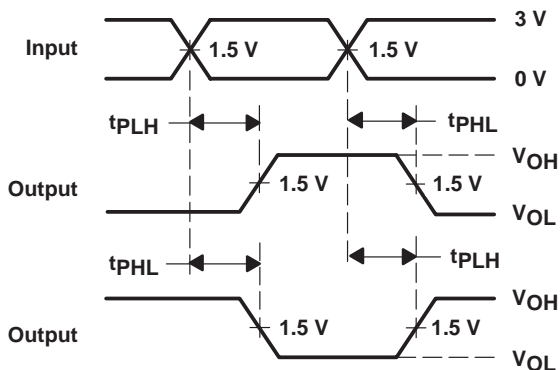
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



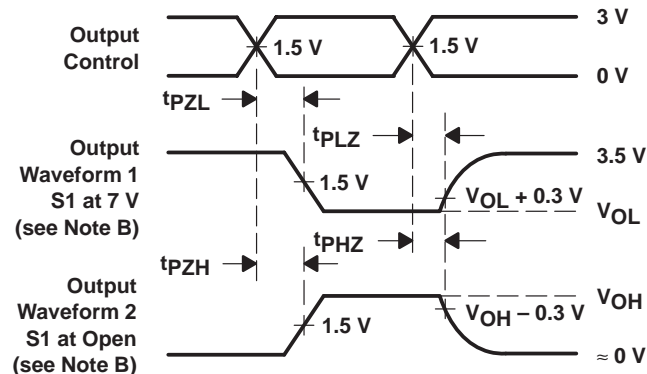
**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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