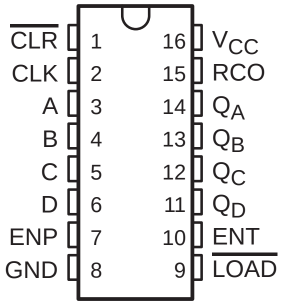
SN74F161A
SYNCHRONOUS 4-BIT BINARY COUNTER

SDFS056A – D2932, MARCH 1987 – REVISED OCTOBER 1993

- **Internal Look-Ahead Circuitry for Fast Counting**
- **Carry Output for N-Bit Cascading**
- **Fully Synchronous Operation for Counting**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

This synchronous, presettable, 4-bit binary counter features an internal carry look-ahead circuitry for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable (ENP, ENT) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple-clock) counters; however, counting spikes may occur on the ripple-carry (RCO) output. A buffered clock (CLK) input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, it may be preset to any number between 0 and 15. As presetting is synchronous, setting up a low level at the load ($\overline{\text{LOAD}}$) input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

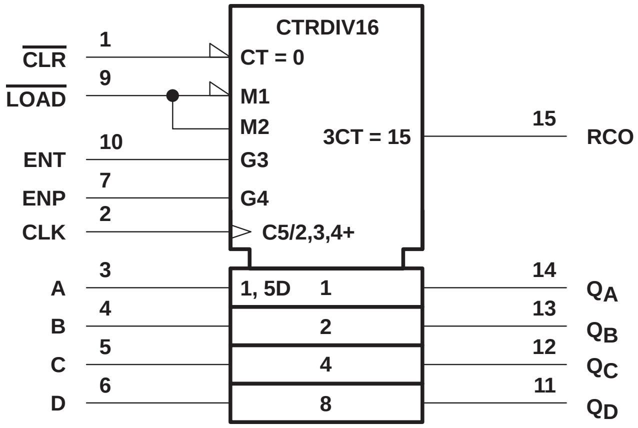
The clear function for the SN74F161A is asynchronous and a low level at the clear ($\overline{\text{CLR}}$) input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable (ENP, ENT) inputs and a ripple-carry (RCO) output. Both ENP and ENT must be high to count, and ENT if fed forward to enable RCO. RCO thus enabled will produce a high-level pulse while the count is 15 (HHHH). The high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed regardless of the level of the clock input.

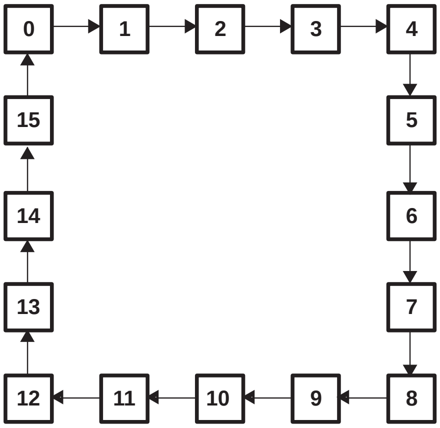
The SN74F161A features a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the setup and hold times.

The SN74F161A is characterized for operation from 0°C to 70°C.

logic symbol[†]

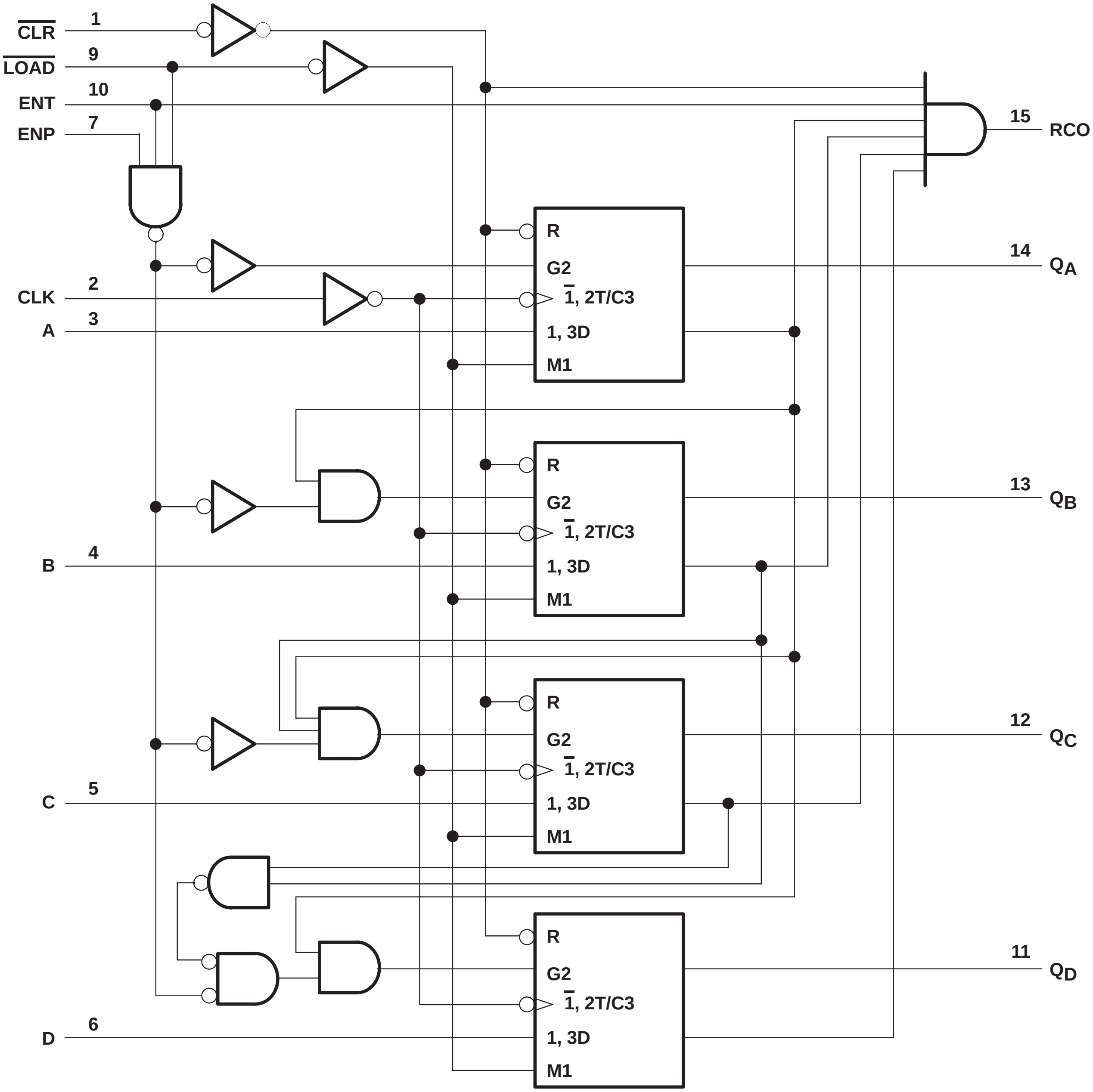


state diagram

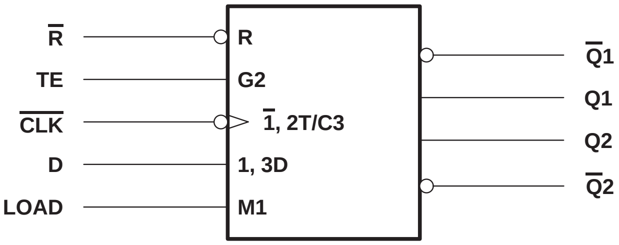


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

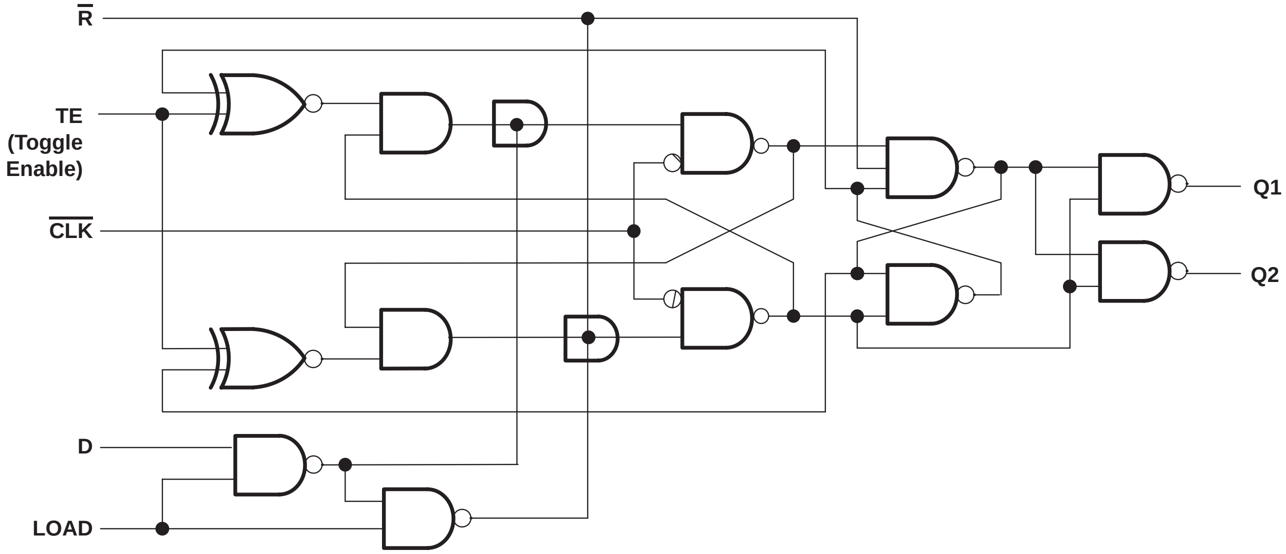
logic diagram (positive logic)



logic symbol, each flip-flop



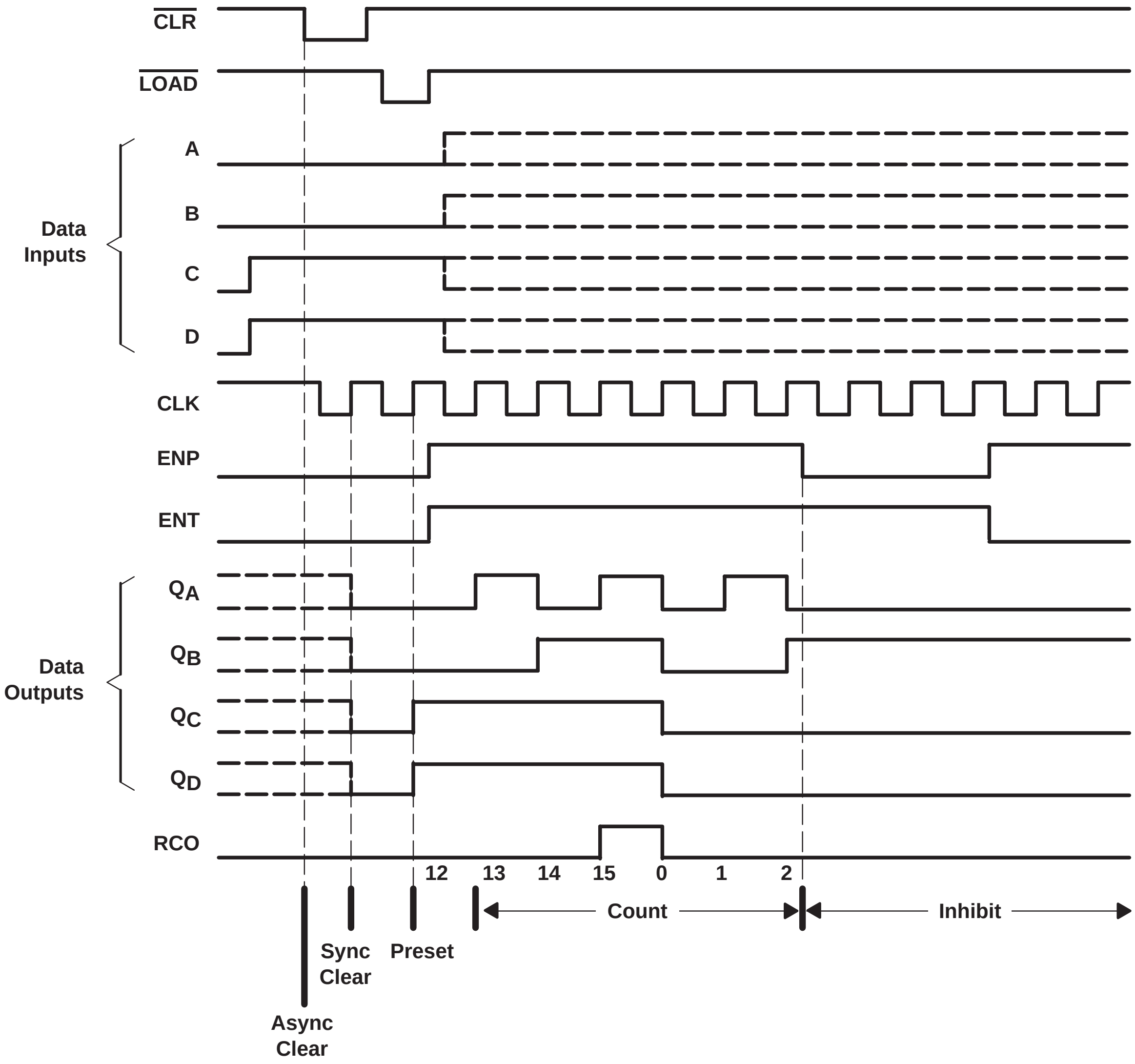
logic diagram, each flip-flop (positive logic)



typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–1.2 V to 7 V
Input current range	–30 mA to 5 mA
Voltage range applied to any output in the high state	–0.5 V to V_{CC}
Current into any output in the low state	40 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			– 1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[‡]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 1 mA	2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = – 1 mA	2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	ENP, CLK, A, B, C, D	V_{CC} = 5.5 V,	V_I = 0.5 V			– 0.6	mA
	ENT, $\overline{\text{LOAD}}$					– 1.2	
	$\overline{\text{CLR}}$					– 0.6	
I_{OS}[§]		V_{CC} = 5.5 V,	V_O = 0	–60		–150	mA
I_{CC}		V_{CC} = 5.5 V			37	55	mA

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

				V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
f_{clock}	Clock frequency			0	100	0	90	MHz
t_w	Pulse duration	CLK high or low (loading)		5		5		ns
		CLK (counting)	High	4		4		
			Low	6		7		
		$\overline{\text{CLR}}$ low		5		5		
t_{su}	Setup time	Data before CLK↑	High or low	5		5		ns
		$\overline{\text{LOAD}}$ before CLK↑	High	11		11.5		
			Low	8.5		9.5		
		ENP and ENT before CLK↑	High	11		11.5		
			Low	5		5		
t_h	Hold time	Data after CLK↑	High or low	2		2		ns
		$\overline{\text{LOAD}}$ after CLK↑	High	2		2		
			Low	0		0		
		ENP and ENT after CLK↑	High or low	0		0		
t_{su}	Inactive-state setup time, $\overline{\text{CLR}}$ high before CLK↑†			6		6		ns

† Inactive-state state setup time is also referred to as recovery time.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX‡		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			100	120		90		MHz
t_{PLH}	CLK ($\overline{\text{LOAD}}$ high)	Any Q	2.7	5.1	7.5	2.7	8.5	ns
t_{PHL}			2.7	7.1	10	2.7	11	
t_{PLH}	CLK ($\overline{\text{LOAD}}$ low)	Any Q	3.2	5.6	8.5	3.2	9.5	ns
t_{PHL}			3.2	5.6	8.5	3.2	9.5	
t_{PLH}	CLK	RCO	4.2	9.6	14	4.2	15	ns
t_{PHL}			4.2	9.6	14	4.2	15	
t_{PLH}	ENT	RCO	1.7	4.1	7.5	1.7	8.5	ns
t_{PHL}			1.7	4.1	7.5	1.7	8.5	
t_{PHL}	$\overline{\text{CLR}}$	Any Q	4.7	8.6	12	4.7	13	ns
		RCO	3.7	7.6	10.5	3.7	11.5	

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and waveforms are shown in Section 1.

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