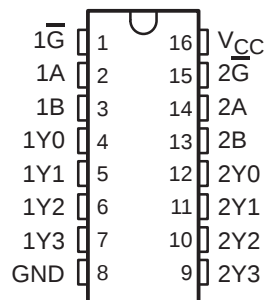


SN54HCT139, SN74HCT139 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SCLS066B – MARCH 1982 – REVISED MAY 1997

- Inputs Are TTL-Voltage Compatible
- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporate Two Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

SN54HCT139 . . . J OR W PACKAGE
SN74HCT139 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



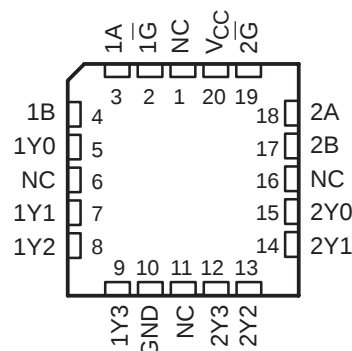
description

The 'HCT139 are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay time of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The 'HCT139 comprise two individual 2-line to 4-line decoders in a single package. The active-low enable ($\overline{G}$) input can be used as a data line in demultiplexing applications. These decoders/demultiplexers feature fully buffered inputs, each of which represents only one normalized load to its driving circuit.

The SN54HCT139 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HCT139 is characterized for operation from -40°C to 85°C .

SN54HCT139 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{G}$	SELECT		Y0	Y1	Y2	Y3
	B	A				
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L



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**TEXAS
INSTRUMENTS**

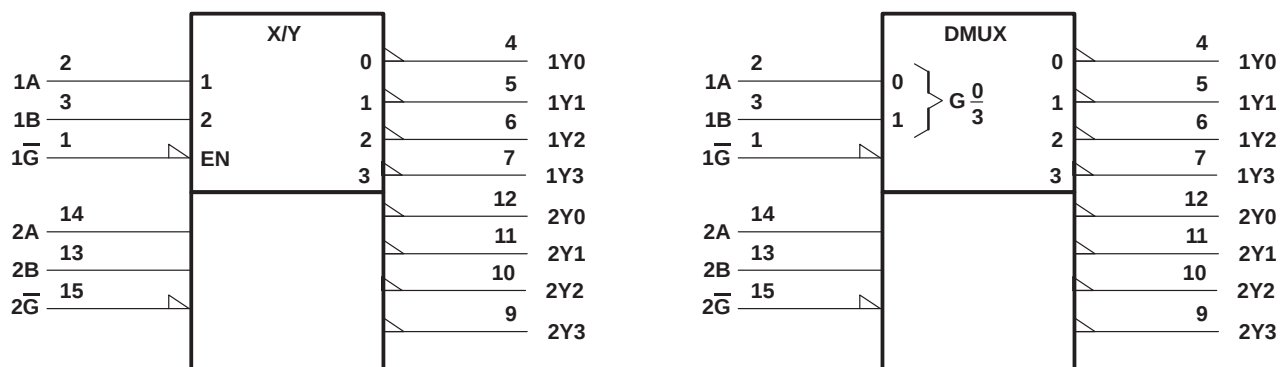
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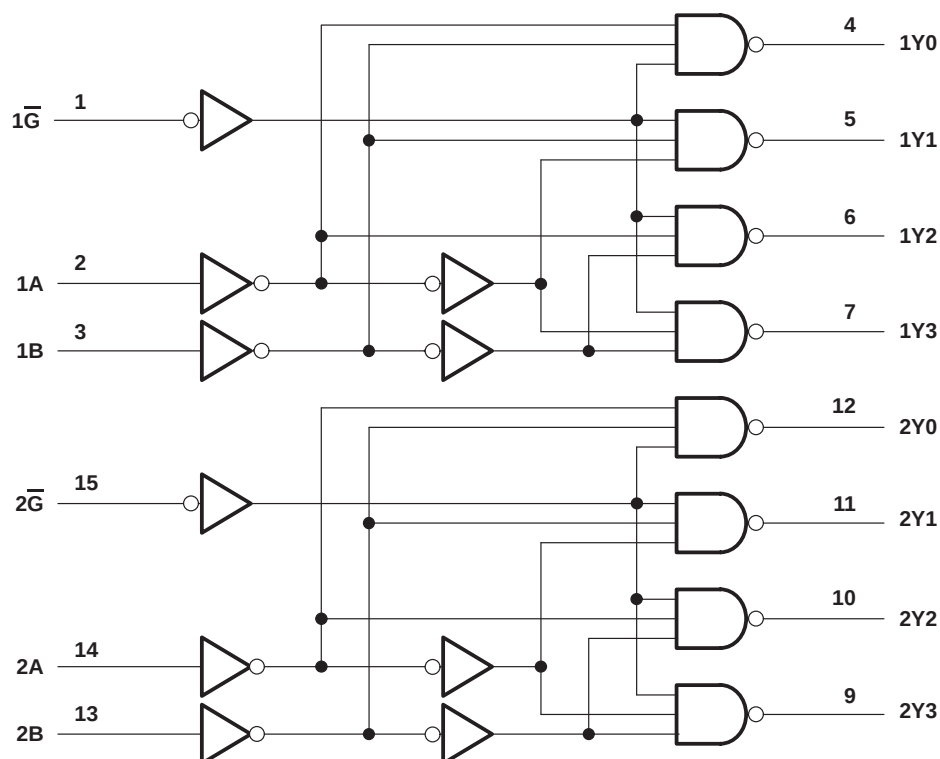
logic symbols (alternatives)[†]



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

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absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	113°C/W
DB package	131°C/W
N package	78°C/W
PW package	149°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		SN54HCT139			SN74HCT139			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$			2			V
V_{IL}	Low-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$			0			V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	0		500	0		500	ns
T_A	Operating free-air temperature	–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT139		SN74HCT139		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20 \mu\text{A}$	4.5 V	4.4	4.499		4.4		4.4		V
		$I_{OH} = -4 \text{ mA}$		3.98	4.3		3.7		3.84		
V_{OL}	$V_I = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \mu\text{A}$	4.5 V		0.001	0.1		0.1		0.1	V
		$I_{OL} = 4 \text{ mA}$			0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC} \text{ or } 0$		5.5 V	±0.1	±100		±1000		±1000		nA
I_{CC}	$V_I = V_{CC} \text{ or } 0, I_O = 0$		5.5 V			8	160		80		μA
$\Delta I_{CC}^\ddagger$	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4	3		2.9		mA
C_i			4.5 V to 5.5 V		3	10	10		10		pF

‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

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DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

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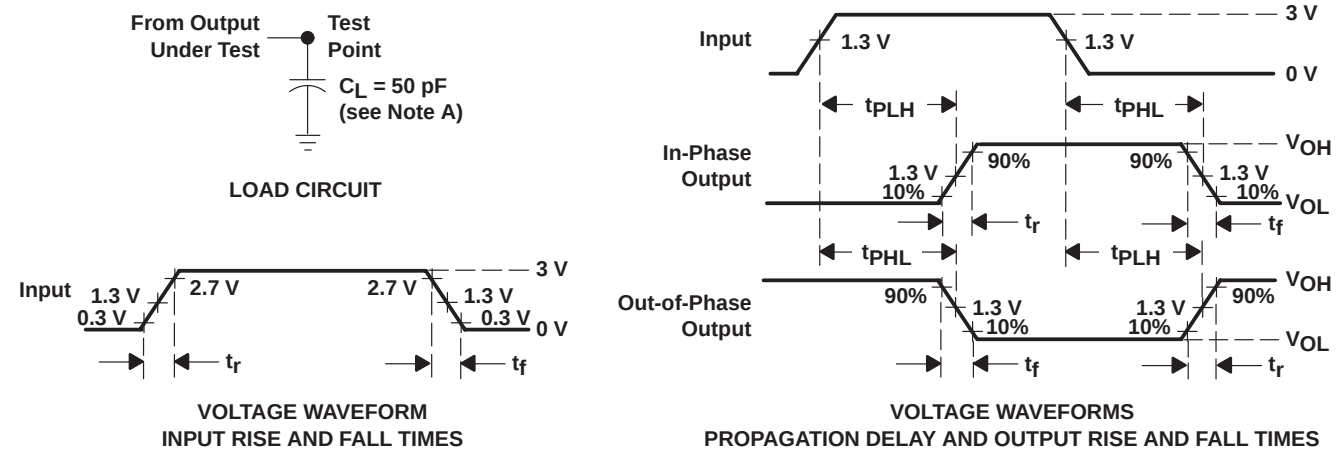
switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT139		SN74HCT139		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	4.5 V		14	34		51		43	ns
			5.5 V		12	30		50		40	
	$\overline{G}$	Y	4.5 V		11	34		51		43	
			5.5 V		10	30		50		40	
t_t		Y	4.5 V		8	15		22		19	ns
			5.5 V		6	14		21		17	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per decoder	No load	25	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r = 6\text{ ns}$, $t_f = 6\text{ ns}$.
 - C. The outputs are measured one at a time with one input transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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