

**TYPE SN54L71**  
**AND-GATED R-S MASTER-SLAVE**  
**FLIP-FLOPS WITH PRESET AND CLEAR**  
 REVISED DECEMBER 1983

- Dependable Texas Instruments Quality and Reliability





**description**

This R-S flip-flop circuit is based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave

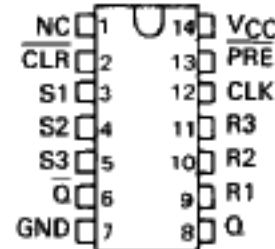
The SN54L71 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

**FUNCTION TABLE**

INPUTS					OUTPUTS	
PRE	CLR	CLK	S	R	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H		L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H		H	L	H	L
H	H		L	H	L	H
H	H		H	H	INDETERMINATE	

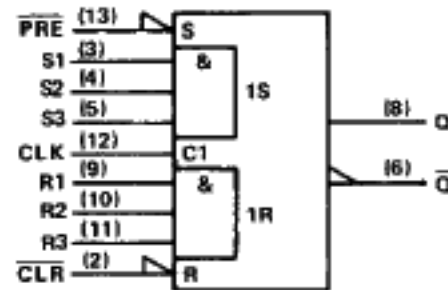
<sup>†</sup> This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

**SN54L71 . . . J PACKAGE**  
**(TOP VIEW)**



NC - No internal connection

**logic symbol**



Pin numbers shown are for J packages.

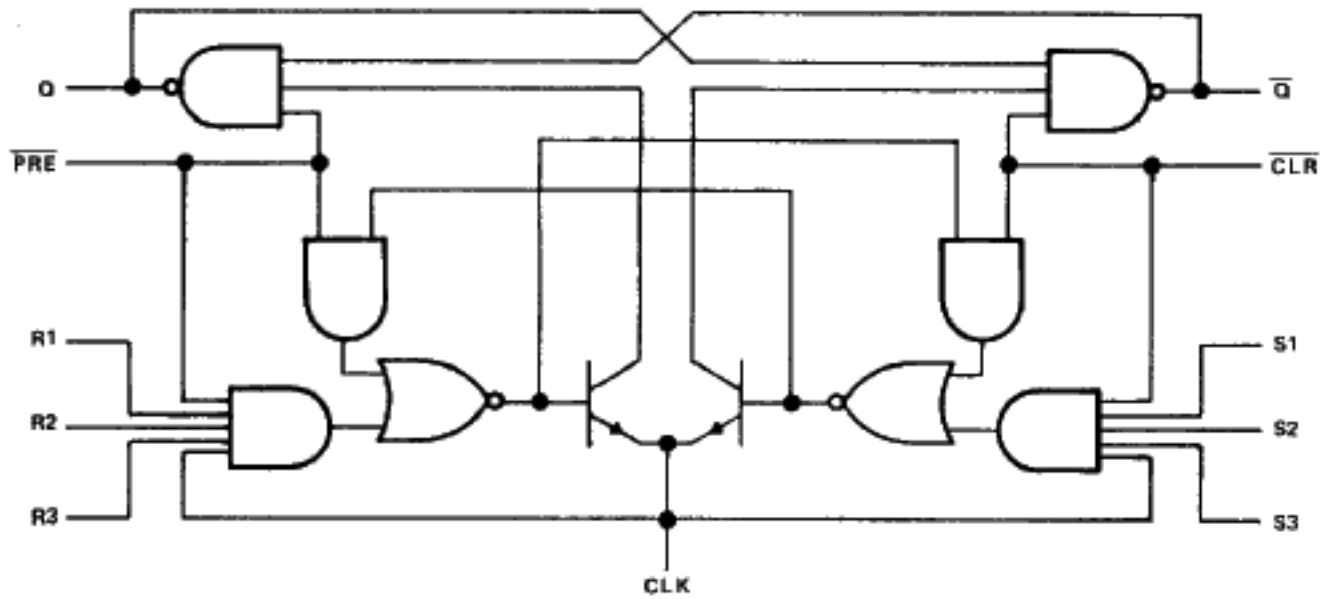
**positive logic**

$$R = R1 \cdot R2 \cdot R3$$

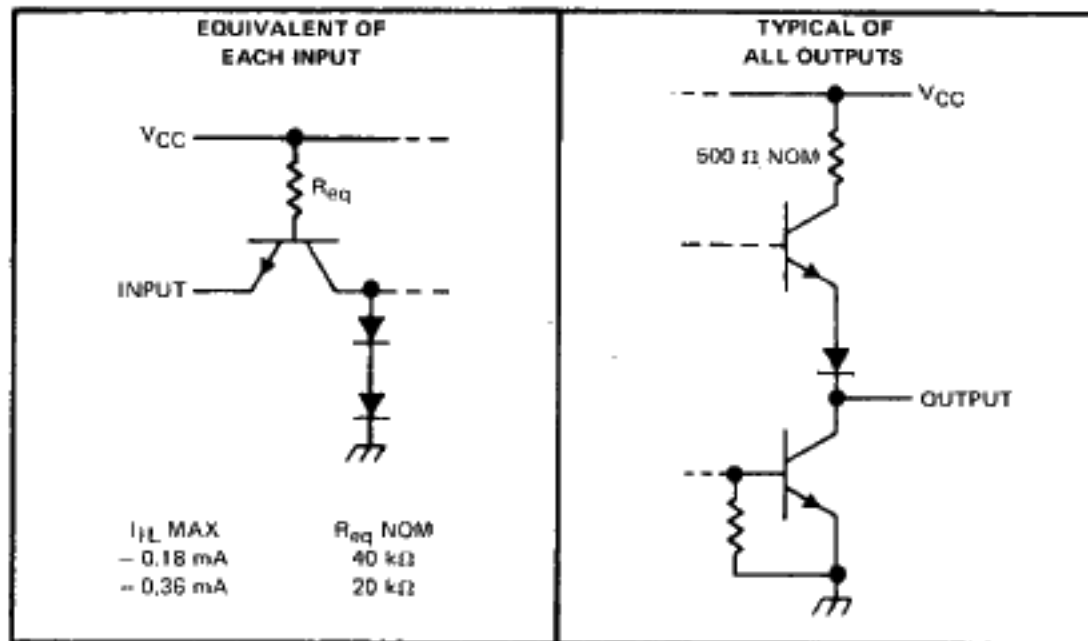
$$S = S1 \cdot S2 \cdot S3$$

**TYPE SN54L71  
AND-GATED R-S MASTER-SLAVE  
FLIP-FLOPS WITH PRESET AND CLEAR**

logic diagram



schematics of input and outputs



3

TTL DEVICES

# TYPE SN54L71 AND-GATED R-S MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage .....	5.5 V
Operating free-air temperature .....	- 55°C to 125°C
Storage temperature range .....	- 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage	Clock input		0.6	V
	All other inputs		0.7	
$I_{OH}$ High-level output current			- 0.1	mA
$I_{OL}$ Low-level output current			2	mA
$t_w$ Pulse duration	CLK high or low		200	ns
	PRE or CLR low		100	
$t_{su}$ Setup time before CLK $\uparrow$	0			ns
$t_h$ Hold time-data after CLK $\downarrow$	0			ns
$T_A$ Operating free-air temperature	- 55		125	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS $\dagger$	MIN	TYP $\ddagger$	MAX	UNIT
$V_{OH}$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = \text{MAX}$ , $I_{OH} = -0.1 \text{ mA}$	2.4	3.3		V
$V_{OL}$	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = \text{MAX}$ , $I_{OL} = 2 \text{ mA}$		0.15	0.3	V
$I_I$	R or S	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$		0.1	mA
	All other			0.2	
$I_{IH}$	R or S	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$		10	$\mu\text{A}$
	PRE or CLR			20	
	CLK			- 0.2	
$I_{IL}$	R or S	$V_{CC} = \text{MAX}$ , $V_I = 0.3 \text{ V}$		- 0.18	mA
	All other			- 0.36	
$I_{OS}$	$V_{CC} = \text{MAX}$	- 3		- 15	mA
$I_{CC}$	$V_{CC} = \text{MAX}$ , See Note 2		0.76	1.44	mA

$\dagger$  For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

$\ddagger$  All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

NOTE 2: With all outputs open,  $I_{CC}$  is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{max}}$				2.5	3		MHz
$t_{PLH}$	PRE or CLR	Q or $\bar{Q}$	$R_L = 4 \text{ k}\Omega$ , $C_L = 50 \text{ pF}$		35	75	ns
$t_{PHL}$	PRE or CLR (CLK high)	$\bar{Q}$ or Q		60	150	ns	
	PRE or CLR (CLK low)				200		
$t_{PLH}$	CLK	Q or $\bar{Q}$		10	35	75	ns
$t_{PHL}$			10	60	150		

NOTE 3: See General Information Section for load circuits and voltage waveforms.

**3**  
TTL DEVICES