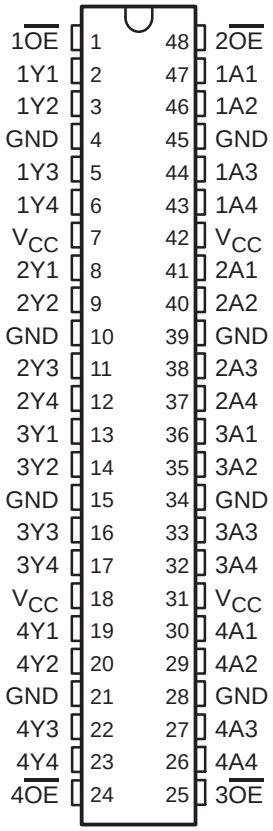
- **Member of the Texas Instruments Widebus™ Family**
- **Operates From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max $t_{pd}$ of 4.1 ns at 3.3 V**
- **Typical $V_{OLP}$ (Output Ground Bounce) <0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) >2 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V $V_{CC}$)**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

**DGG, DGV, OR DL PACKAGE**
**(TOP VIEW)**




## description/ordering information

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

The SN74LVCH16244A is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | SSOP − DL | Tube | SN74LVCH16244ADL | LVCH16244A |
| | | Tape and reel | SN74LVCH16244ADLR | |
| | TSSOP − DGG | Tape and reel | SN74LVCH16244ADGGR | LVCH16244A |
| | TVSOP − DGV | Tape and reel | SN74LVCH16244ADGVR | LDH244A |
| | VFBGA − GQL | Tape and reel | SN74LVCH16244AGQLR | LDH244A |
| | VFBGA − ZQL (Pb-free) | | SN74LVCH16244AZQLR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

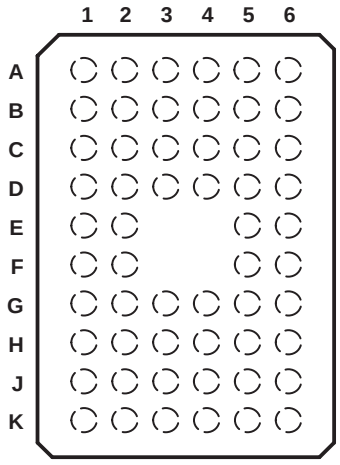
## description/ordering information (continued)

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

**GQL OR ZQL PACKAGE**
**(TOP VIEW)**




### terminal assignments

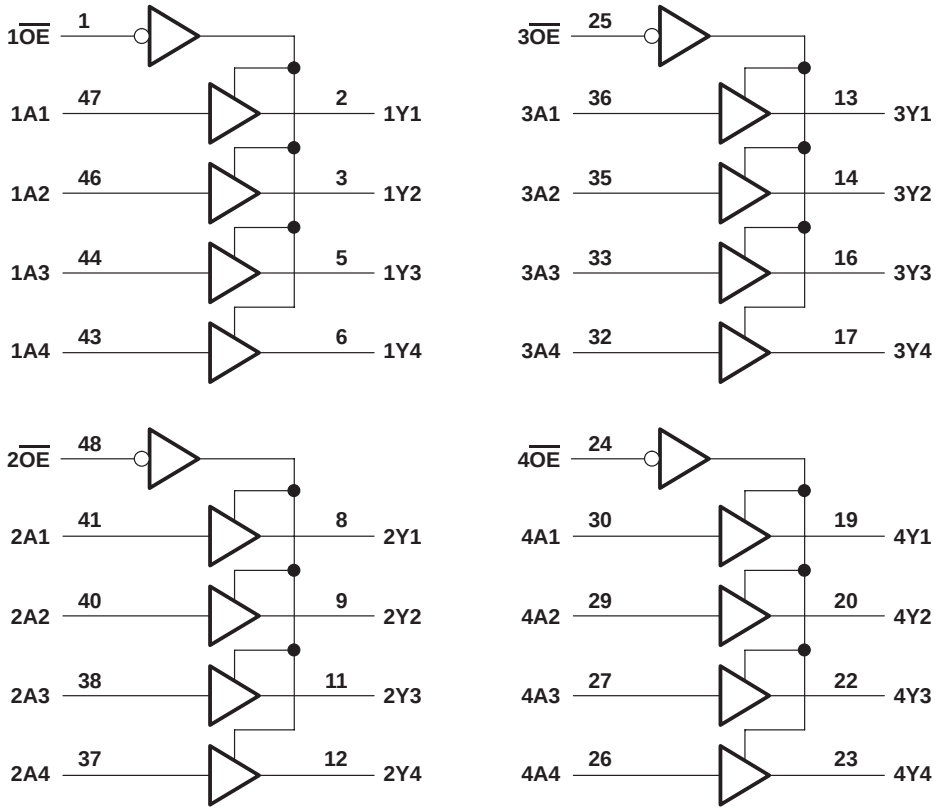
| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| A | $1\overline{OE}$ | NC | NC | NC | NC | $2\overline{OE}$ |
| B | 1Y2 | 1Y1 | GND | GND | 1A1 | 1A2 |
| C | 1Y4 | 1Y3 | $V_{CC}$ | $V_{CC}$ | 1A3 | 1A4 |
| D | 2Y2 | 2Y1 | GND | GND | 2A1 | 2A2 |
| E | 2Y4 | 2Y3 | | | 2A3 | 2A4 |
| F | 3Y1 | 3Y2 | | | 3A2 | 3A1 |
| G | 3Y3 | 3Y4 | GND | GND | 3A4 | 3A3 |
| H | 4Y1 | 4Y2 | $V_{CC}$ | $V_{CC}$ | 4A2 | 4A1 |
| J | 4Y3 | 4Y4 | GND | GND | 4A4 | 4A3 |
| K | $4\overline{OE}$ | NC | NC | NC | NC | $3\overline{OE}$ |

NC − No internal connection

**FUNCTION TABLE**
**(each 4-bit buffer)**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | A | Y |
| L | H | H |
| L | L | L |
| H | X | Z |

## logic diagram (positive logic)




Pin numbers shown are for the DGG, DGV, and DL packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) . . . . . −0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . −50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . −50 mA
Continuous output current, $I_O$ . . . . . ±50 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package . . . . . 70°C/W
DGV package . . . . . 58°C/W
DL package . . . . . 63°C/W
GQL/ZQL package . . . . . 42°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of $V_{CC}$ is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | $0.65 \times V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | $0.35 \times V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | High or low state | 0 | $V_{CC}$ | V |
| | | 3-state | 0 | 5.5 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | −4 | mA |
| | | $V_{CC}$ = 2.3 V | | −8 | |
| | | $V_{CC}$ = 2.7 V | | −12 | |
| | | $V_{CC}$ = 3 V | | −24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 2.7 V | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | −40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | $I_{OH}$ = −100 μA | | 1.65 V to 3.6 V | $V_{CC}$−0.2 | | | V |
| | $I_{OH}$ = −4 mA | | 1.65 V | 1.2 | | | |
| | $I_{OH}$ = −8 mA | | 2.3 V | 1.7 | | | |
| | $I_{OH}$ = −12 mA | | 2.7 V | 2.2 | | | |
| | | | 3 V | 2.4 | | | |
| | $I_{OH}$ = −24 mA | | 3 V | 2.2 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 μA | | 1.65 V to 3.6 V | | | 0.2 | V |
| | $I_{OL}$ = 4 mA | | 1.65 V | | | 0.45 | |
| | $I_{OL}$ = 8 mA | | 2.3 V | | | 0.7 | |
| | $I_{OL}$ = 12 mA | | 2.7 V | | | 0.4 | |
| | $I_{OL}$ = 24 mA | | 3 V | | | 0.55 | |
| $I_I$ | $V_I$ = 0 to 5.5 V | | 3.6 V | | | ±5 | μA |
| $I_{I(hold)}$ | $V_I$ = 0.58 V | | 1.65 V | 15 | | | μA |
| | $V_I$ = 1.07 V | | | −15 | | | |
| | $V_I$ = 0.7 V | | 2.3 V | 45 | | | |
| | $V_I$ = 1.7 V | | | −45 | | | |
| | $V_I$ = 0.8 V | | 3 V | 75 | | | |
| | $V_I$ = 2 V | | | −75 | | | |
| | $V_I$ = 0 to 3.6 V‡ | | 3.6 V | | | ±500 | |
| $I_{off}$ | $V_I$ or $V_O$ = 5.5 V | | 0 | | | ±10 | μA |
| $I_{OZ}$ | $V_O$ = 0 to 5.5 V | | 3.6 V | | | ±10 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND | $I_O$ = 0 | 3.6 V | | | 20 | μA |
| | 3.6 V ≤ $V_I$ ≤ 5.5 V§ | | | | | 20 | |
| $\Delta I_{CC}$ | One input at $V_{CC}$ − 0.6 V, | Other inputs at $V_{CC}$ or GND | 2.7 V to 3.6 V | | | 500 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 5.5 | | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 6 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.
§ This applies in the disabled state only.

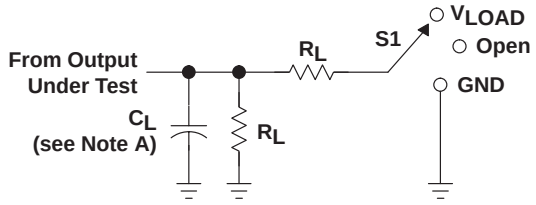
## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 1.5 | 6.6 | 1 | 3.9 | 1 | 4.7 | 1.1 | 4.1 | ns |
| $t_{en}$ | $\overline{OE}$ | Y | 1.5 | 7.5 | 1 | 4.7 | 1 | 5.8 | 1 | 4.6 | ns |
| $t_{dis}$ | $\overline{OE}$ | Y | 1.5 | 10.3 | 1 | 5.3 | 1 | 6.2 | 1.8 | 5.8 | ns |
| $t_{sk(o)}$ | | | | | | | | | | 1 | ns |

## operating characteristics, $T_A = 25°C$

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance per buffer/driver | Outputs enabled | f = 10 MHz | 33 | 32 | 35 | pF |
| | | Outputs disabled | | 2 | 2 | 3 | |

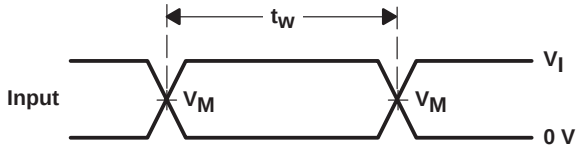
## PARAMETER MEASUREMENT INFORMATION



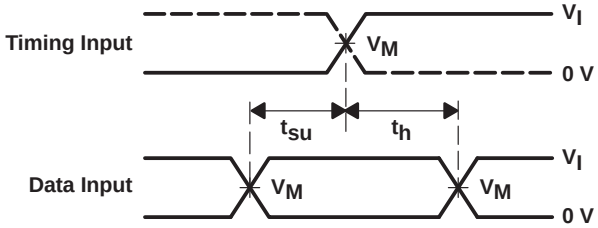

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

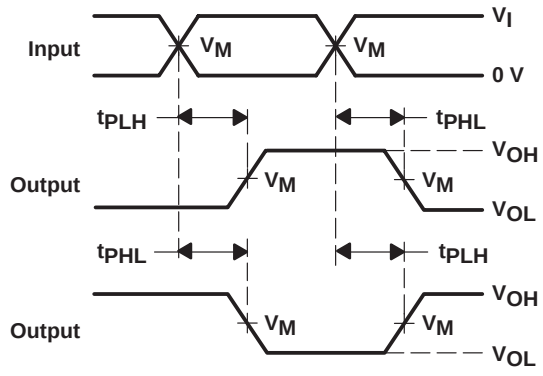
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V ± 0.3 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



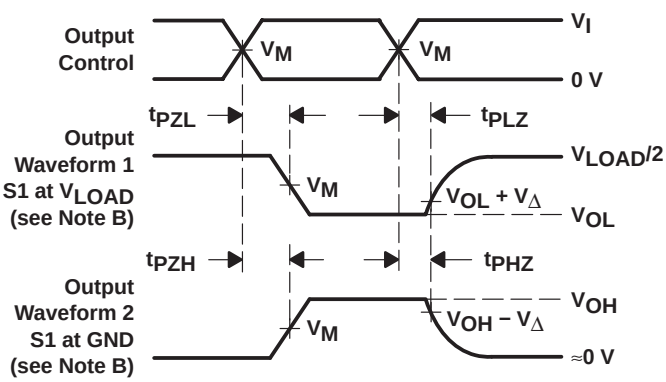

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

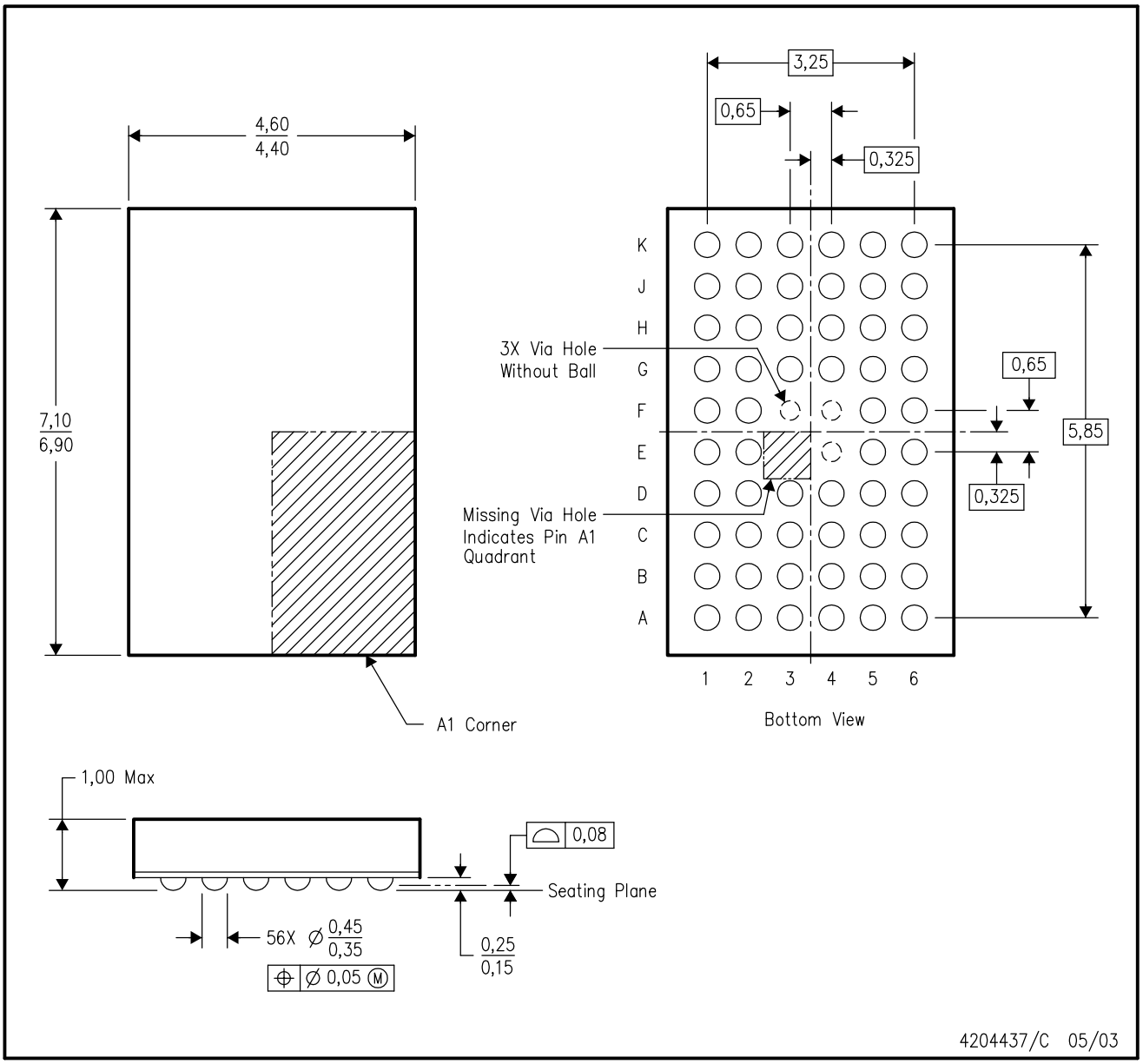



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

ZQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY

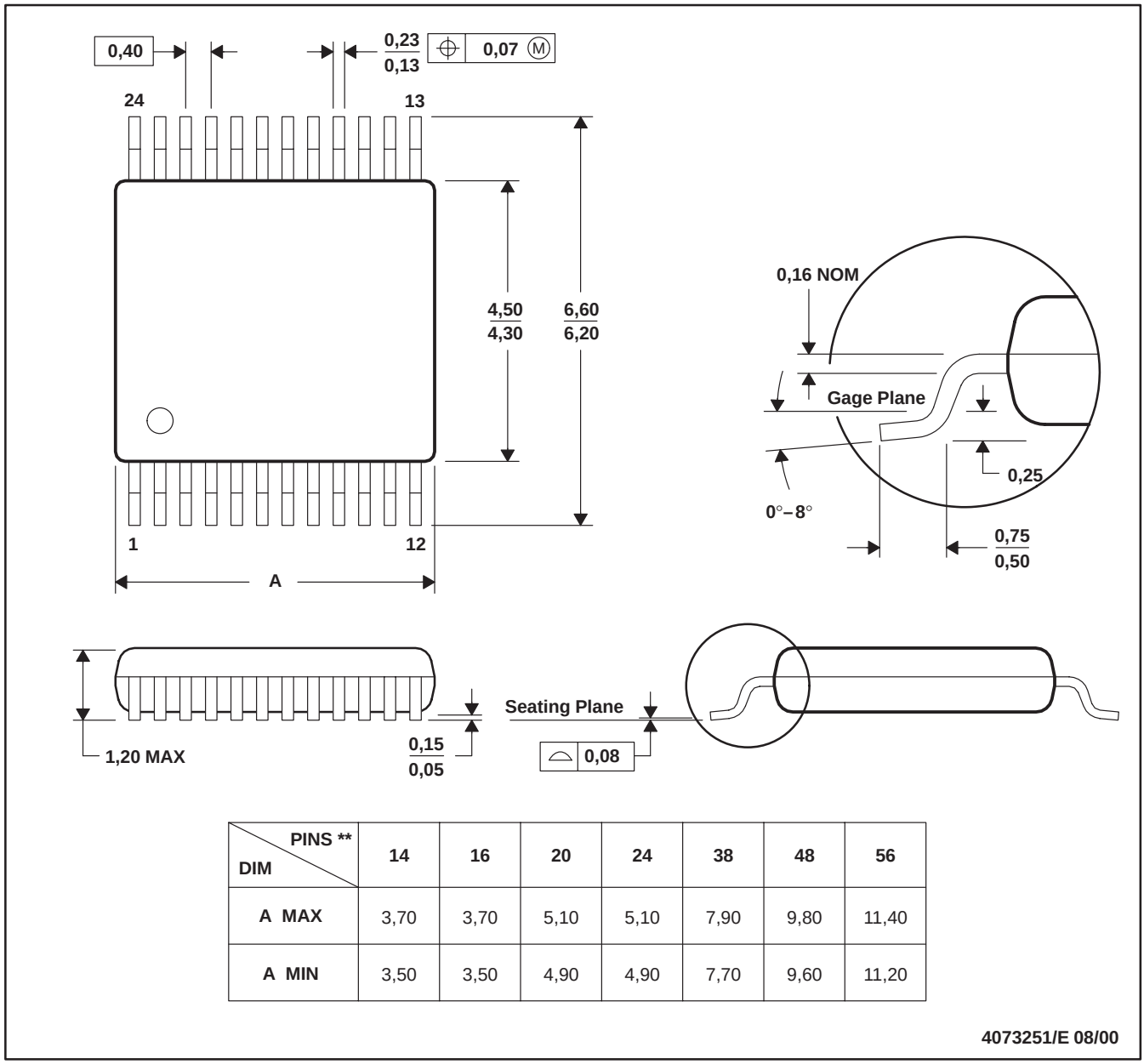



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration.
D. Falls within JEDEC MO–225 variation BA.
E. This package is lead–free. Refer to the 56 GQL package (drawing 4200583) for tin–lead (SnPb).

MicroStar Junior is a trademark of Texas Instruments.

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

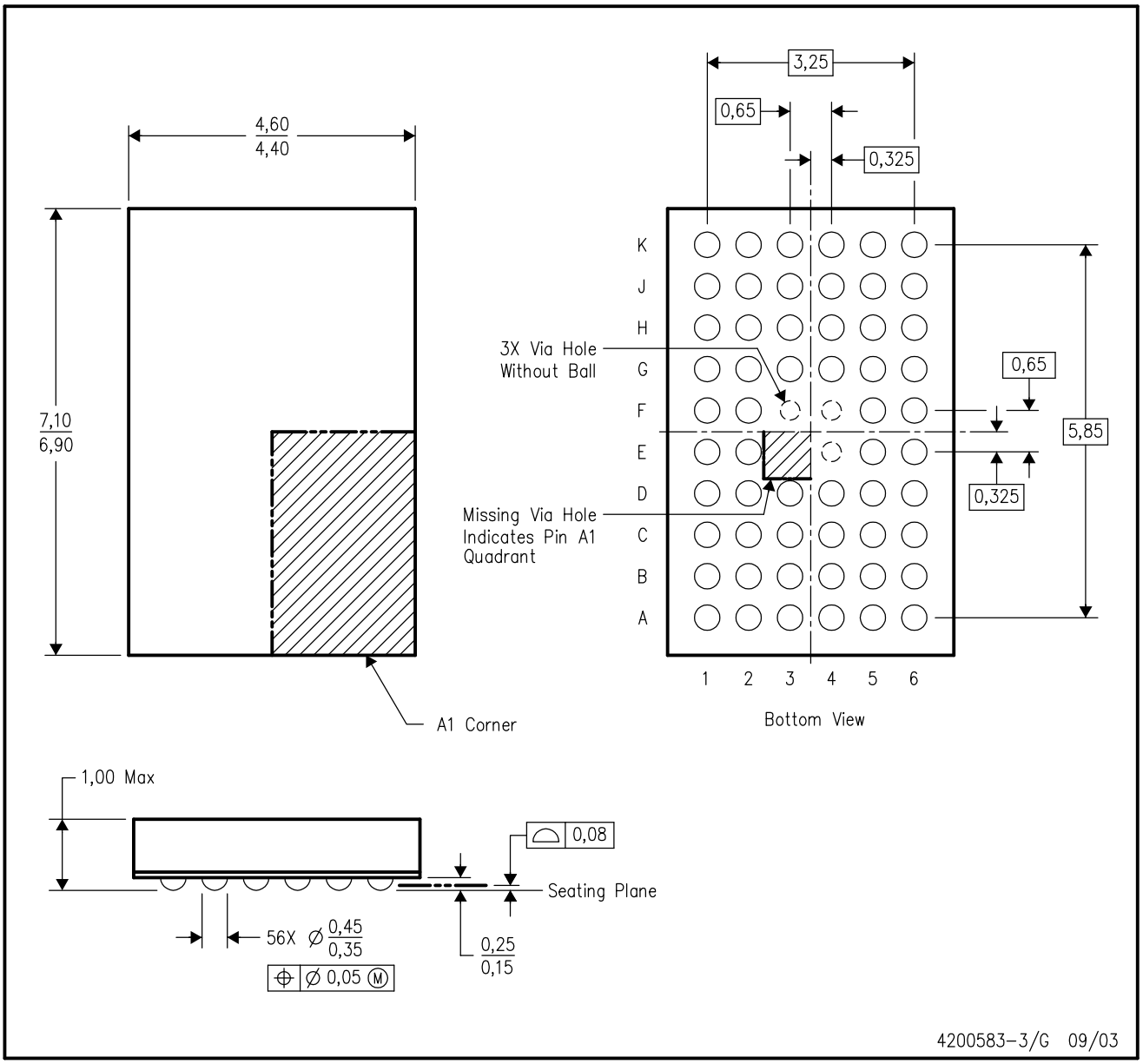



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration.
D. Falls within JEDEC MO–225 variation BA.
E. This package is tin–lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead–free.

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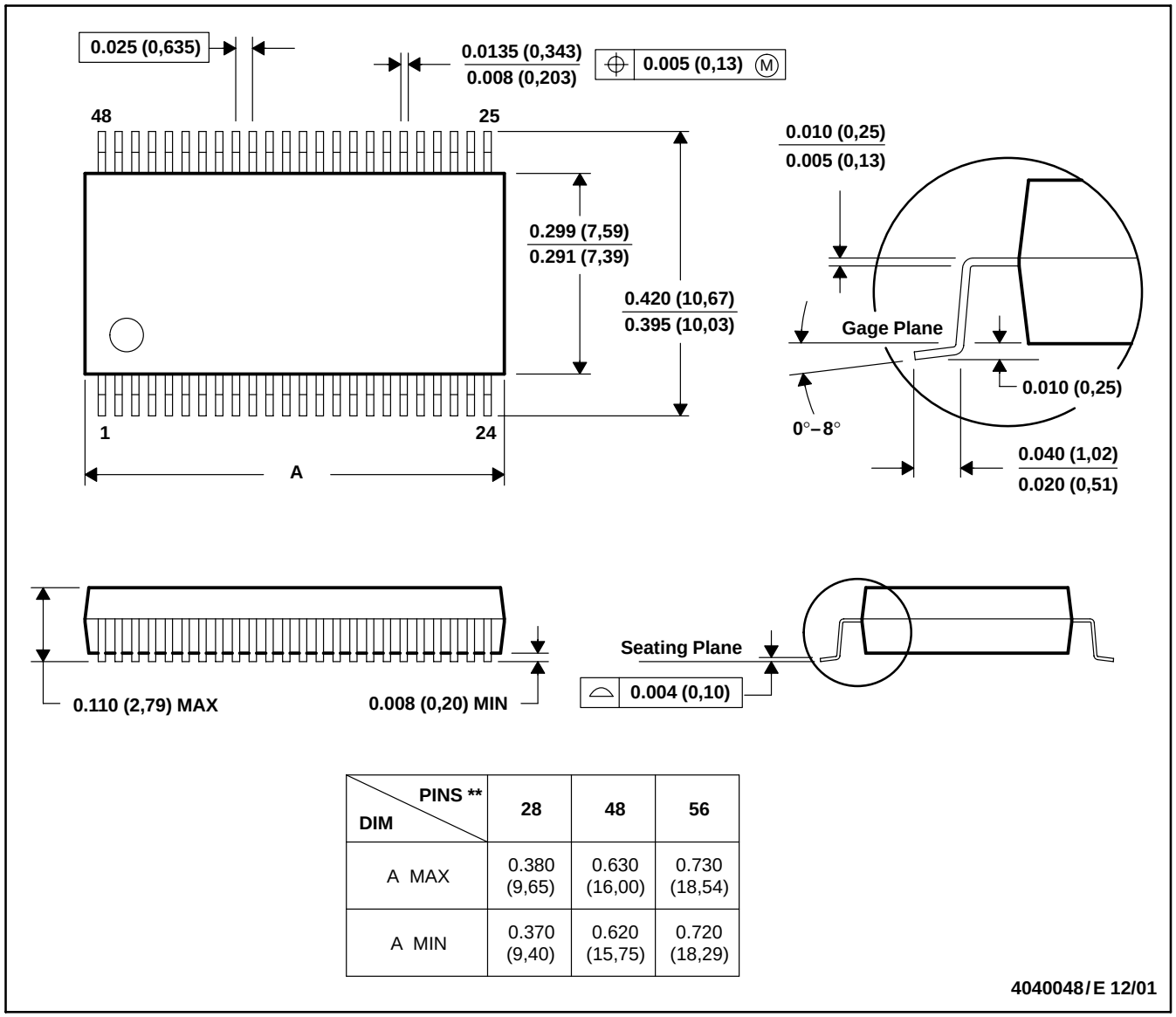
## DL (R-PDSO-G**)

## PLASTIC SMALL-OUTLINE PACKAGE

**48 PINS SHOWN**



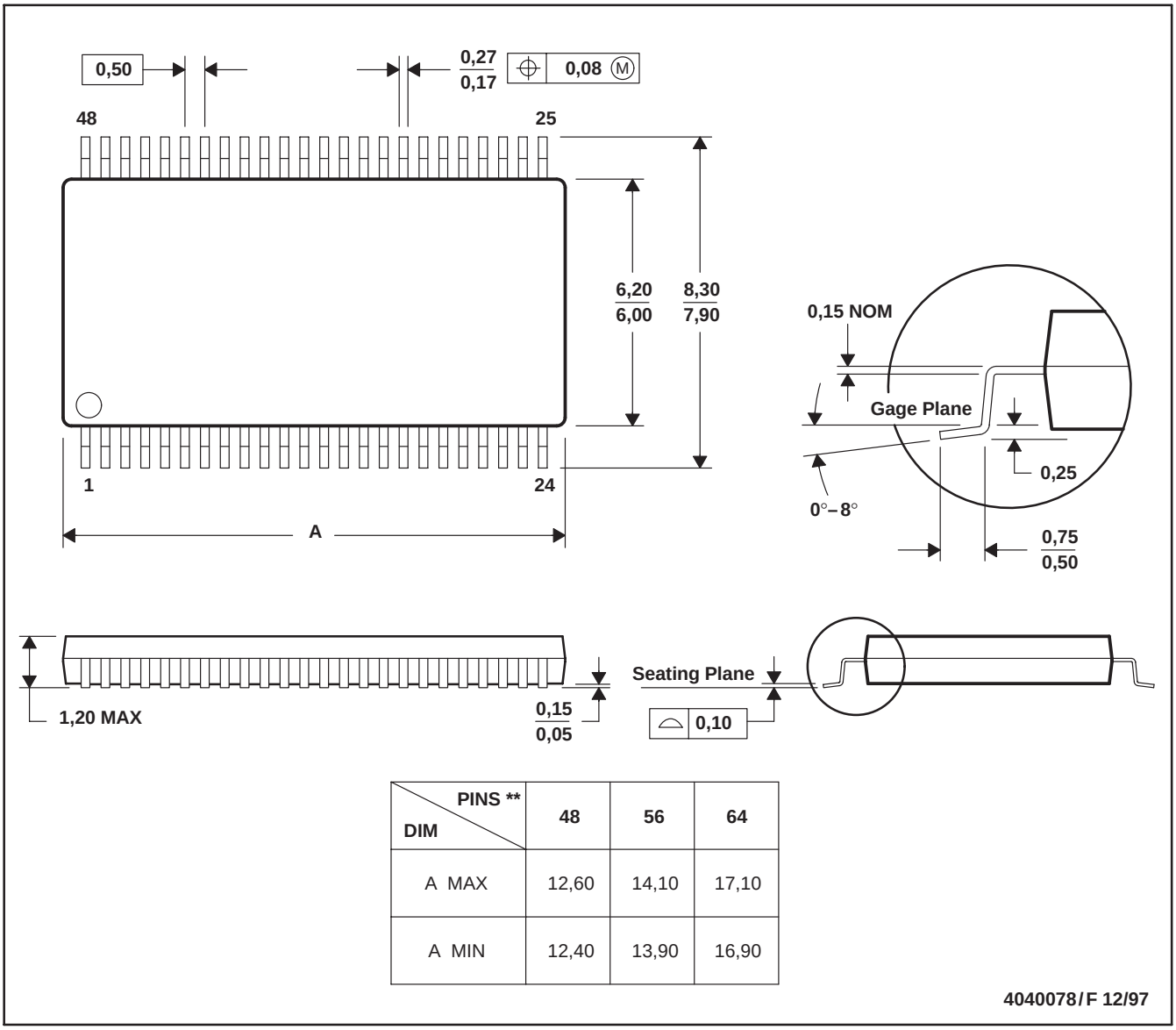

| DIM \ PINS ** | 28 | 48 | 56 |
|---|---|---|---|
| A MAX | 0.380 (9,65) | 0.630 (16,00) | 0.730 (18,54) |
| A MIN | 0.370 (9,40) | 0.620 (15,75) | 0.720 (18,29) |

**4040048/E 12/01**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**




| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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