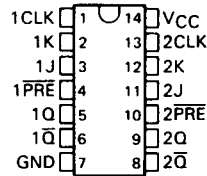


# SN54LS113A, SN54S113, SN74LS113A, SN74S113A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

D2661, APRIL 1982 - REVISED MARCH 1988

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54LS113A, SN54S113 . . . J OR W PACKAGE  
SN74LS113A, SN74S113A . . . D OR N PACKAGE  
(TOP VIEW)



## description

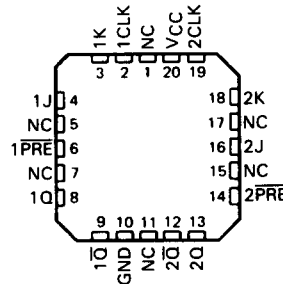
These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset input sets the outputs regardless of the levels of the other inputs. When preset (PRE) is inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54LS113A and SN54S113 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS113A and SN74S113A are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each flip-flop)

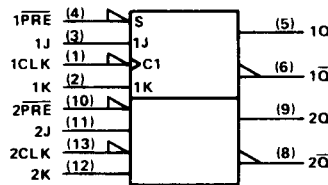
INPUTS				OUTPUTS	
PRE	CLK	J	K	Q	Q-bar
L	X	X	X	H	L
H	↓	L	L	Q <sub>0</sub>	Q <sub>0</sub> -bar
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q <sub>0</sub>	Q <sub>0</sub> -bar

SN54LS113A, SN54S113 . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

## logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

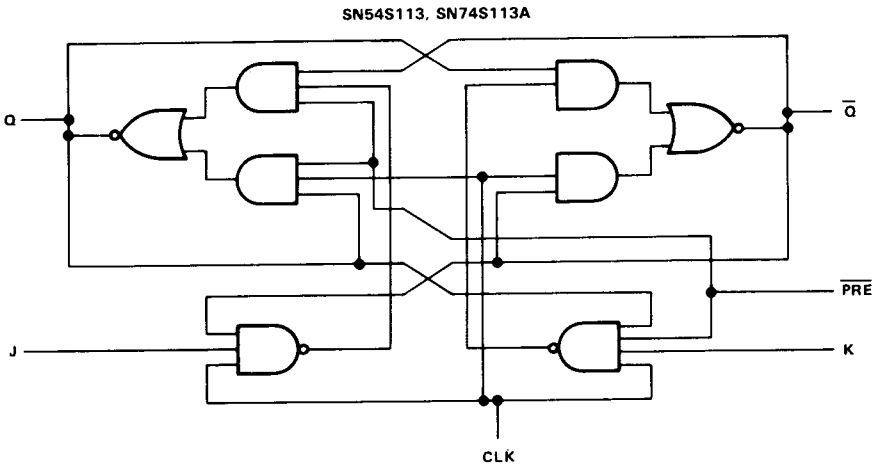
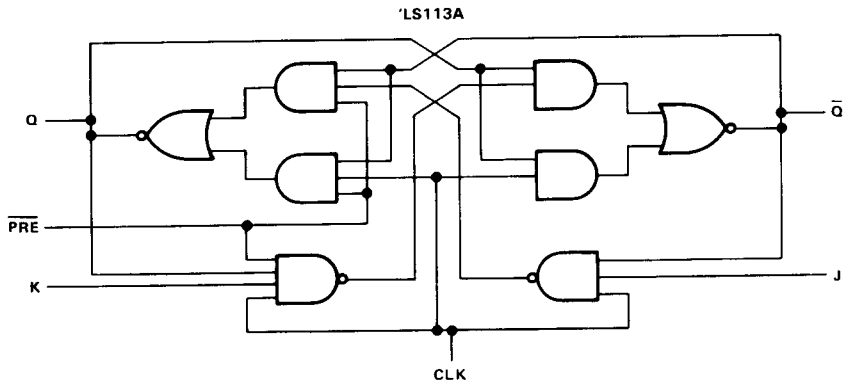
Pin numbers shown are for D, J, N, and W packages.

2

TTL Devices

**SN54LS113A, SN54S113, SN74LS113A, SN74S113A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH PRESET**

logic diagrams (positive logic)



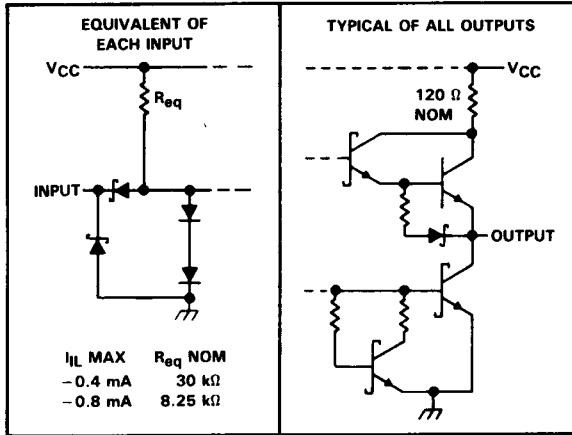
2

TTL Devices

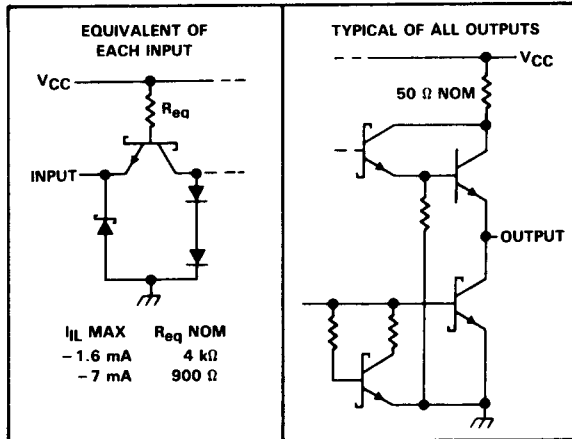
**SN54LS113A, SN74LS113A, SN54S113, SN74S113A  
DUAL J-K NEGATIVE-EDGE-TRIGGERED  
FLIP-FLOPS WITH PRESET**

**schematics of inputs and outputs**

'LS113A



SN54S113, SN74S113A



**2**  
TTL Devices

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, VCC (see Note 1)	7 V
Input voltage: 'LS113A	7 V
SN54S113, SN74S113A	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminals.

**SN54LS113A, SN74LS113A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH PRESET**

**recommended operating conditions**

		SN54LS113A			SN74LS113A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.7			0.8	V
I <sub>OH</sub>	High-level output current			-0.4			-0.4	mA
I <sub>OL</sub>	Low-level output current			4			8	mA
f <sub>clock</sub>	Clock frequency	0		30	0		30	MHz
t <sub>w</sub>	Pulse duration	CLK high		20	20			ns
		PRE or CLR low		25	25			
t <sub>su</sub>	Set up time-before CLK↓	Data high or low		20	20			ns
		PRE inactive		20	20			
t <sub>h</sub>	Hold time-data after CLK↓			0	0			ns
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

**2**

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

**TTL Devices**

PARAMETER		TEST CONDITIONS†	SN54LS113A			SN74LS113A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA	-1.5			-1.5			V
V <sub>OH</sub>		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = -0.4 mA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 4 mA	0.25	0.4		0.25	0.4		V
		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 8 mA				0.35	0.5		
I <sub>I</sub>	J or K	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V	0.1			0.1			mA
	PRE		0.3			0.3			
	CLK		0.4			0.4			
I <sub>IH</sub>	J or K	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V	20			20			μA
	PRE		60			60			
	CLK		80			80			
I <sub>IL</sub>	J or K	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V	-0.4			-0.4			mA
	PRE or CLK		-0.8			-0.8			
I <sub>OS</sub> ‡		V <sub>CC</sub> = MAX, see Note 2	-20	-100		-20	-100		mA
I <sub>CC</sub> (Total)		V <sub>CC</sub> = MAX, see Note 3	4	6		4	6		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTES: 2. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V<sub>O</sub> = 2.25 V and 2.125 V for the '54 family and the '74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

3. With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

**SN54LS113A, SN74LS113A**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED**  
**FLIP-FLOPS WITH PRESET**

switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{max}$			$R_L = 2\text{ k}\Omega$ , $C_L = 15\text{ pF}$	30	45		MHz
$t_{PLH}$	PRE or CLK	Q or $\bar{Q}$			15	20	ns
$t_{PHL}$					15	20	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

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TTL Devices

# SN54S113, SN74S113A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

## recommended operating conditions

		SN54S113			SN74S113A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage				0.8			V
I <sub>OH</sub>	High-level output current				-1			-1 mA
I <sub>OL</sub>	Low-level output current				20			20 mA
t <sub>w</sub>	Pulse duration	CLK high		6	6		ns	
		CLK low		6.5	6.5			
		PRE low		8	8			
t <sub>su</sub>	Set up time-before CLK↓	Data high or low		7	7		ns	
t <sub>h</sub>	Hold time-data after CLK↓	0			0			ns
T <sub>A</sub>	Operating free-air temperature	-55	125		0	70		°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

2  
TTL Devices

PARAMETER		TEST CONDITIONS†		SN54S113			SN74S113A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = MIN,	I <sub>I</sub> = -18 mA	-1.2			-1.2			V
V <sub>OH</sub>		V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -1 mA	2.5	3.4		2.7	3.4		V
V <sub>OL</sub>		V <sub>CC</sub> = MIN,	V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 20 mA	0.5			0.5			V
I <sub>I</sub>		V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5 V	1			1			mA
I <sub>IH</sub>	J or K	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.7 V	50			50			μA
	PRE or CLK			100			100			
I <sub>IL</sub>	J or K	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.5 V	-1.6			-1.6			mA
	PRE‡			-7			-7			
	CLK‡			-4			-4			
I <sub>OS</sub> ‡		V <sub>CC</sub> = MAX		-40	-100		-40	-100		mA
I <sub>CC</sub> ‡		V <sub>CC</sub> = MAX,	see Note 3	15	25		15	25		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Clear is tested with preset high and preset is tested with clear high.

¶ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

# Values are average per flip-flop.

NOTE 3: With all outputs open, I<sub>CC</sub> is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>				80	125		MHz
t <sub>PLH</sub>	PRE	Q or $\bar{Q}$	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 15 pF		4	7	ns
t <sub>PHL</sub>	PRE (CLK high)	$\bar{Q}$ or Q			5	7	ns
	PRE (CLK low)				5	7	ns
t <sub>PLH</sub>	CLK	Q or $\bar{Q}$			4	7	ns
t <sub>PHL</sub>					5	7	ns

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.