- Controls 32 Electrodes
- 80-V (Ramped V_{CC2}) Totem-Pole Outputs
- Low CMOS Stand-By Power Consumption
- Energy Recovery System Compatible
- 15-mA Source and Sink Compatibility
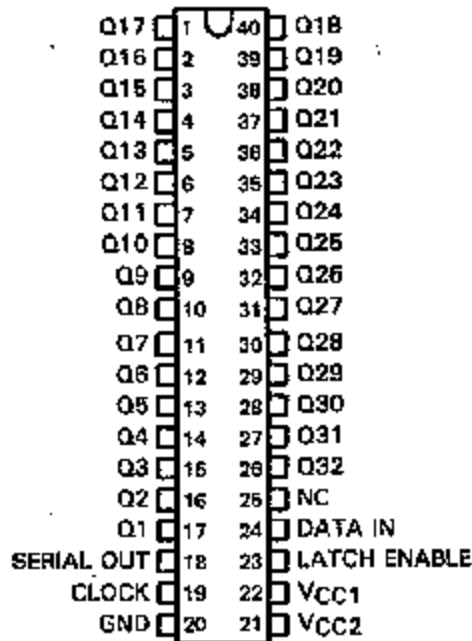- High-Speed Serially-Shifted Data Input

description

The SN65559, SN65560, SN75559, and SN75560 are monolithic BIDFET[†] integrated circuits designed to provide the serial-to-parallel conversion and level translation of data in a matrix-addressable electroluminescent display. The device inputs are diode-clamped CMOS inputs. The SN65560 and SN75560 output sequences are reversed from the SN65559 and SN75559 for ease in printed circuit board layout.

These column drivers consist of a 32-bit static shift register, 32 latches, and 32 high-voltage outputs. Serial data is entered into the shift register on the low-to-high transition of the clock signal. A logic high signal on the Latch Enable input transfers the data from the shift register to the latches while the V_{CC2} bus is low. Once stable in the latch circuits, the V_{CC2} rail is ramped up to allow the data to appear at the high-voltage outputs. By limiting V_{CC2} to a maximum of 60 volts, these devices may be safely operated in a non-ramped V_{CC2} mode. Drivers may be cascaded via the serial data output of the static shift register. This output is not affected by the Latch Enable input.

The SN65559 and SN65560 are characterized for operation from −40°C to 85°C. The SN75559 and SN75560 are characterized for operation from 0°C to 70°C.
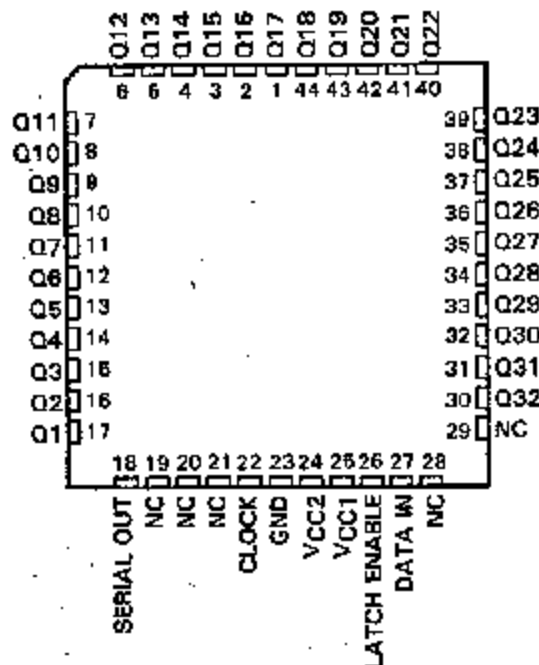
SN65559, SN75559
N DUAL-IN-LINE PACKAGE
(TOP VIEW)

Q17	1	40	Q18
Q16	2	39	Q19
Q15	3	38	Q20
Q14	4	37	Q21
Q13	5	36	Q22
Q12	6	35	Q23
Q11	7	34	Q24
Q10	8	33	Q25
Q9	9	32	Q26
Q8	10	31	Q27
Q7	11	30	Q28
Q6	12	29	Q29
Q5	13	28	Q30
Q4	14	27	Q31
Q3	15	26	Q32
Q2	16	25	NC
Q1	17	24	DATA IN
SERIAL OUT	18	23	LATCH ENABLE
CLOCK	19	22	V_{CC1}
GND	20	21	V_{CC2}

SN65559, SN75559 ... FN PACKAGE
(TOP VIEW)

NC—No internal connection

[†]BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on the same chip—Patented Process

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SN65560, SN75560
N DUAL-IN-LINE PACKAGE
(TOP VIEW)

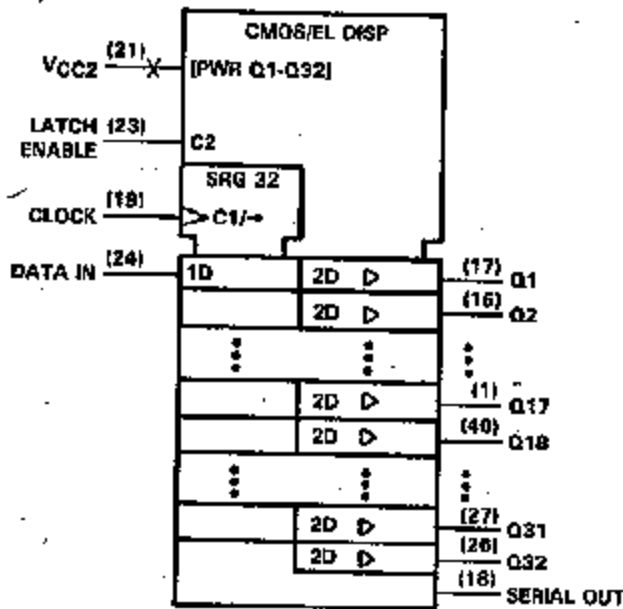|		
Q16	1 ⌴ 40	Q15
Q17	2 39	Q14
Q18	3 38	Q13
Q19	4 37	Q12
Q20	5 36	Q11
Q21	6 35	Q10
Q22	7 34	Q9
Q23	8 33	Q8
Q24	9 32	Q7
Q25	10 31	Q6
Q26	11 30	Q5
Q27	12 29	Q4
Q28	13 28	Q3
Q29	14 27	Q2
Q30	15 26	Q1
Q31	16 25	NC
Q32	17 24	DATA IN
SERIAL OUT	18 23	LATCH ENABLE
CLOCK	19 22	VCC1
GND	20 21	VCC2
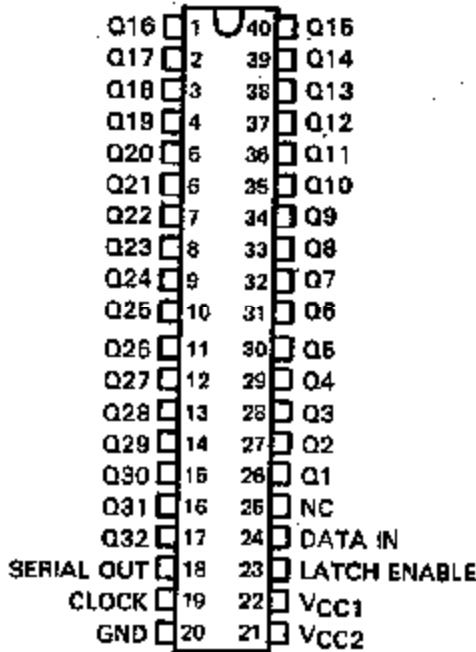
SN65560, SN75560 . . . FN PACKAGE
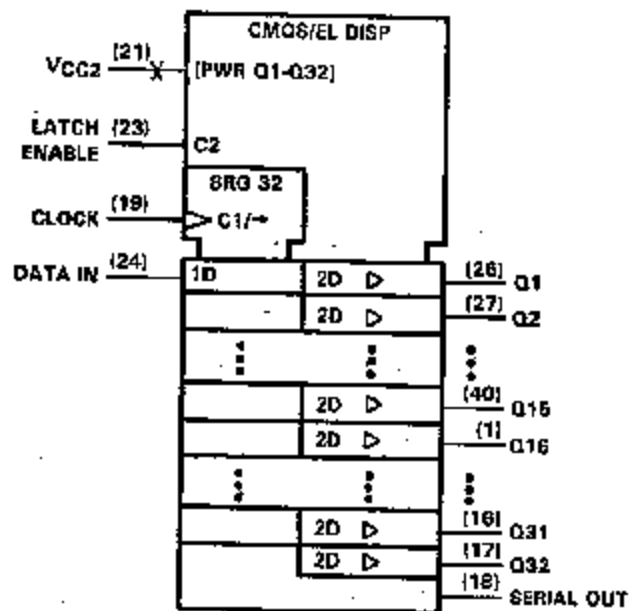### (TOP VIEW)
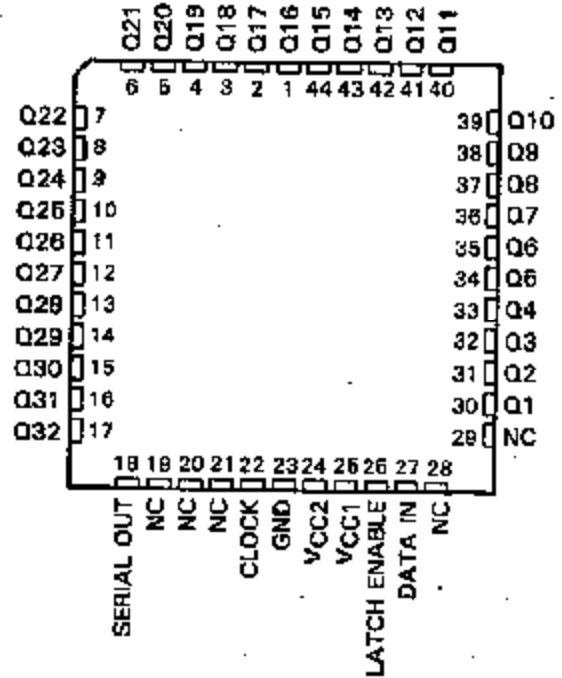
NC—No internal connection

logic symbols†

SN65559, SN75559

SN65560, SN75560

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for N packages.

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FUNCTION TABLE

| FUNCTION | CONTROL INPUTS | | SHIFT REGISTERS R1 THRU R32 | LATCHES LC1 THRU LC32 | OUTPUTS | |
	CLOCK	LATCH ENABLE†			SERIAL	Q1 THRU Q32
LOAD	↑	X	Load and Shift	Determined by Latch Enable	R32‡	LC1 thru LC32 respectively
	Not	X	No change		R32	
LATCH	X	L	As determined above	Stored data	R32	LC1 thru LC32 respectively
	X	H		New data	R32	

H = high level; L = low level; X = irrelevant; ↑ = low-to-high-level transition

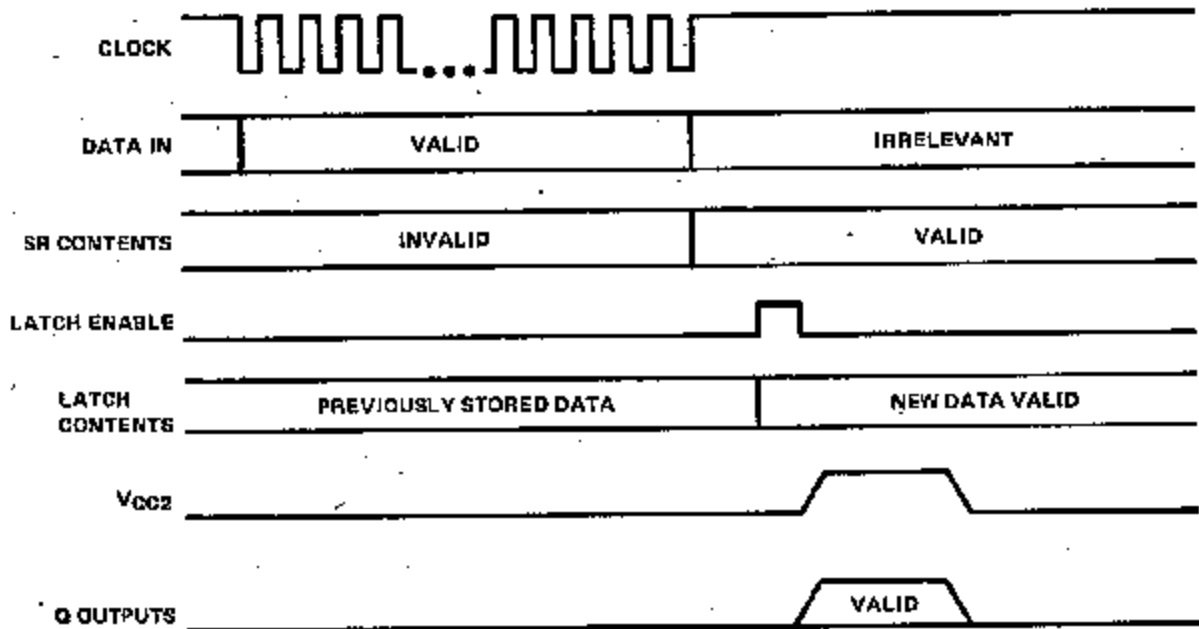† New data enters the latches while Latch Enable is high. These data are stored while Latch Enable is low.

‡ R32 and the serial output take on the state of R31, R31 takes on the state of R30 . . . R2 takes on the state of R1 and R1 takes on the state of the data input.

logic diagram (positive logic)

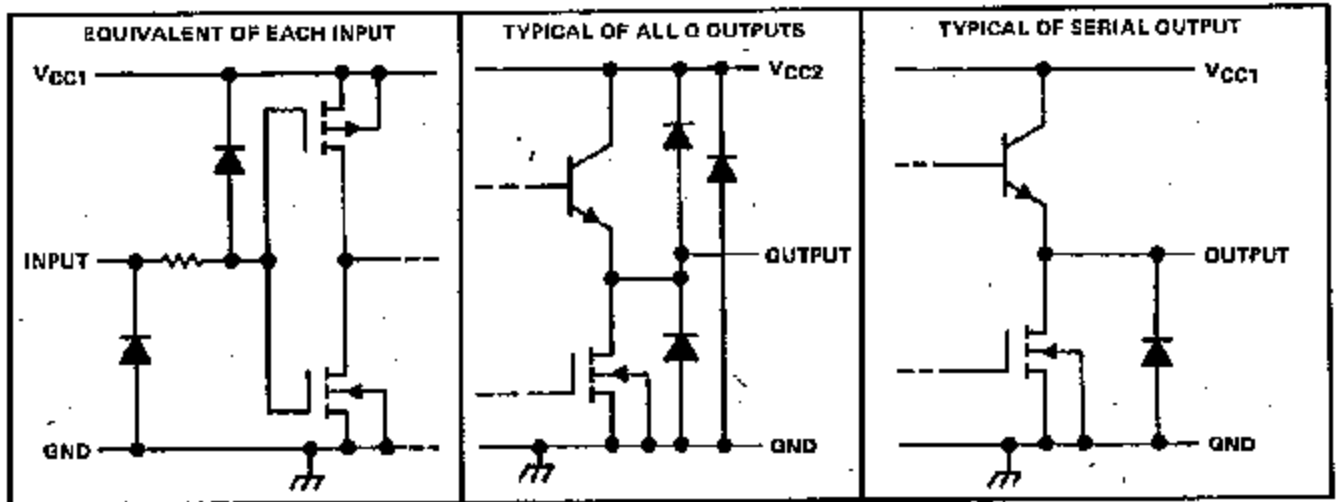Display Drivers 3
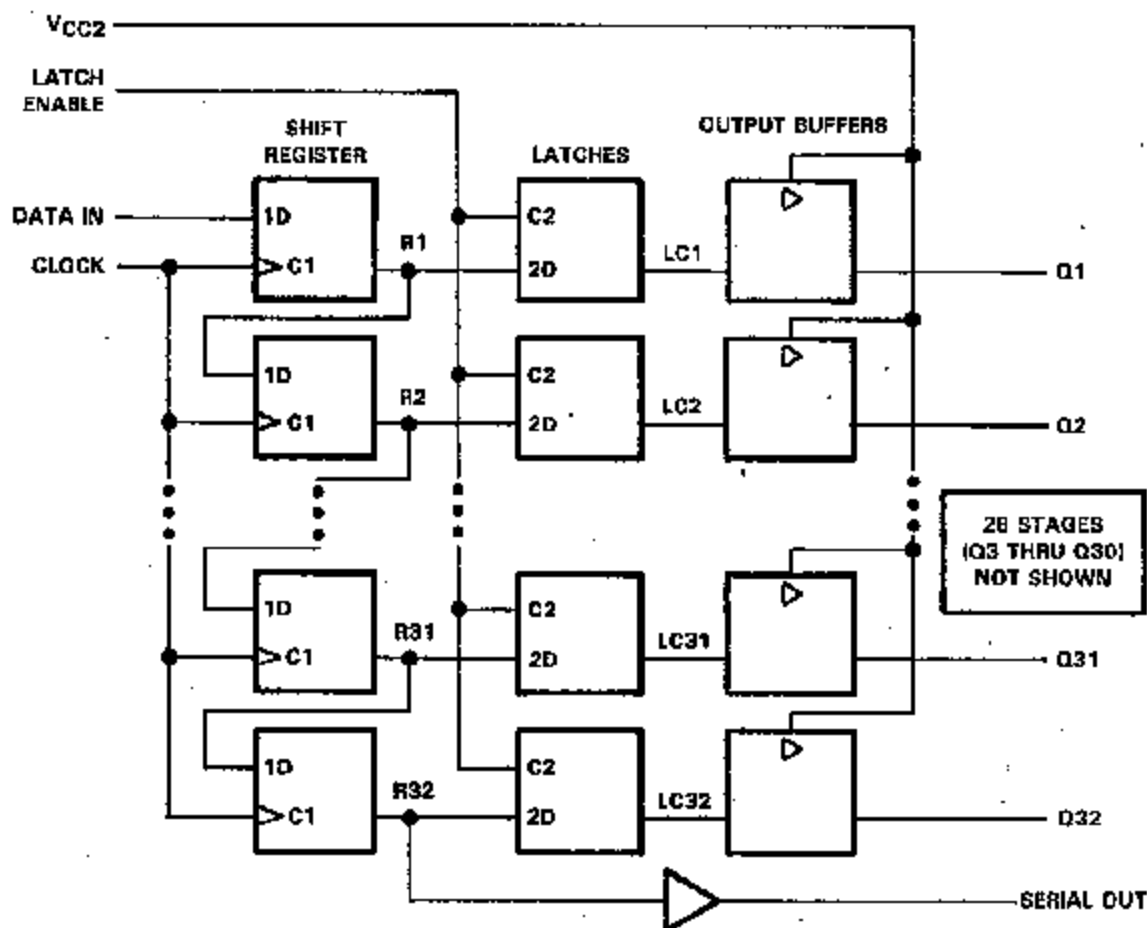
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typical operating sequence

schematic of inputs and outputs

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) .... 18 V

Supply voltage, V_{CC2} .... 90 V

Input voltage, V_I .... $V_{CC1} + 0.3$ V

Continuous total dissipation at (or below) 25 °C free-air temperature (see Note 2):

          N package .... 1250 mW

          FN package .... 1700 mW

Operating free-air temperature range: SN65559, SN65560 .... −40 °C to 85 °C

          SN75559, SN75560 .... 0 °C to 70 °C

Storage temperature range .... −65 °C to 150 °C

Case temperature for 10 seconds: FN package .... 260 °C

Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package .... 260 °C

NOTES: 1. Voltage values are with respect to network ground terminal.
       2. For operation above 25 °C free-air temperature, derate the N package linearly at the rate of 10 mW/°C and the FN package
           at the rate of 13.6 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	15	V
Supply voltage, V_{CC2}		0		80	V
High-level input voltage, V_{IH} (see Figure 1)	$V_{CC1} = 10.8$ V	8.1		11.1	V
	$V_{CC1} = 15$ V	11.25		15.3	
Low-level input voltage, V_{IL} (see Figure 1)	$V_{CC1} = 10.8$ V	−0.3		2.7	V
	$V_{CC1} = 15$ V	−0.3		3.75	
High-level Q output current, I_{OH}		−15			mA
Low-level Q output current, I_{OL}		15			mA
Q output clamp current, I_{OK}				20	mA
Clock frequency, f_{clock}		0		8	MHz
Pulse duration, clock high, $t_{w(CLK)}$		62			ns
Pulse duration, latch enable high, $t_{w(LE)}$		62			ns
Setup time, data before clock 1, t_{su}		20			ns
Hold time, data after clock 1, t_h		50			ns
Rate of rise of V_{CC2}, dv/dt (see Figure 4)				80	V/μs
Operating free-air temperature, T_A	SN65559, SN65560	−40		85	°C
	SN75559, SN75560	0		70	

NOTE 3: V_{CC2} must be ramped only when data within the latches is stable.

electrical characteristics over recommended operating free-air temperature range, $V_{CC1} = 12$ V

	PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	$V_{CC2} = 80$ V,	$I_{OH} = -15$ mA	77		V
		Serial output	$I_{OH} = 100$ μA		10.5		
V_{OL}	Low-level output voltage	Q outputs	$I_{OL} = 15$ mA			8	V
		Serial output	$I_{OL} = 100$ μA			1	
I_{IH}	High-level input current		$V_{IH} = V_{CC1}$			1	μA
I_{IL}	Low-level input current		$V_{IL} = GND$			−1	μA
I_{CC1}	Supply current from V_{CC1}		$V_I = V_{CC1}$			500	μA
I_{CC2}	Supply current from V_{CC2}		$V_{CC2} = 80$ V	Outputs low		3	mA
				Outputs high		0.6	

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switching characteristics, V_{CC1} = 12 V, V_{CC2} = 0, T_A = 25°C

	PARAMETER	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level	Clock	Serial Out	C_L = 20 pF, See Figure 3		140	ns
t_{PLH}	Propagation delay time, low-to-high level	Clock	Serial Out	C_L = 20 pF, See Figure 3		140	ns
t_d	Delay time, V_{CC2} to Q output	V_{CC2}	Q	dv/dt = 80 V/μs, C_L = 100 pF, See Figure 4		100	ns

RECOMMENDED OPERATING CONDITIONS

INPUT VOLTAGE LOGIC-LEVEL LIMITS
vs
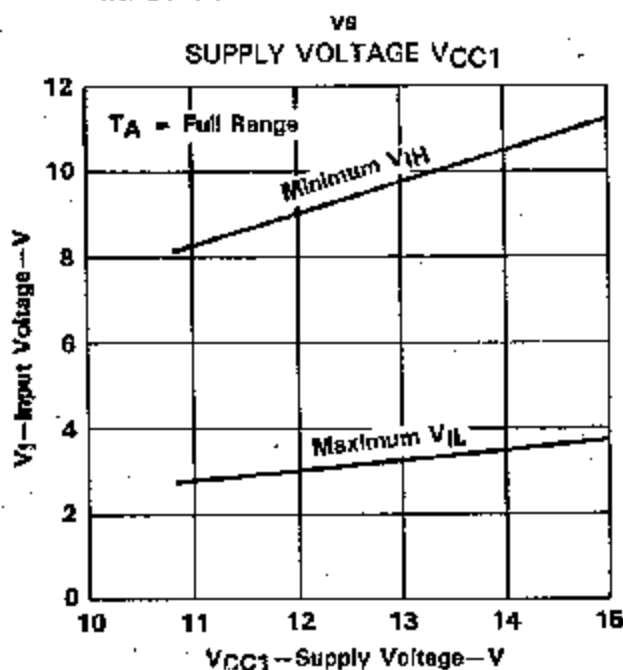### SUPPLY VOLTAGE V_{CC1}

FIGURE 1

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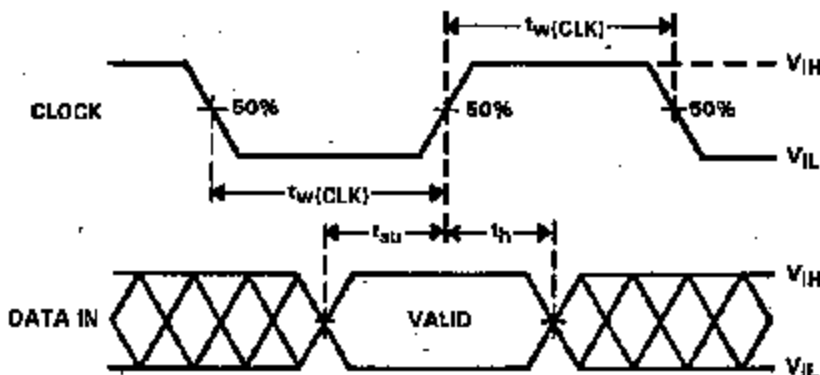## PARAMETER MEASUREMENT INFORMATION
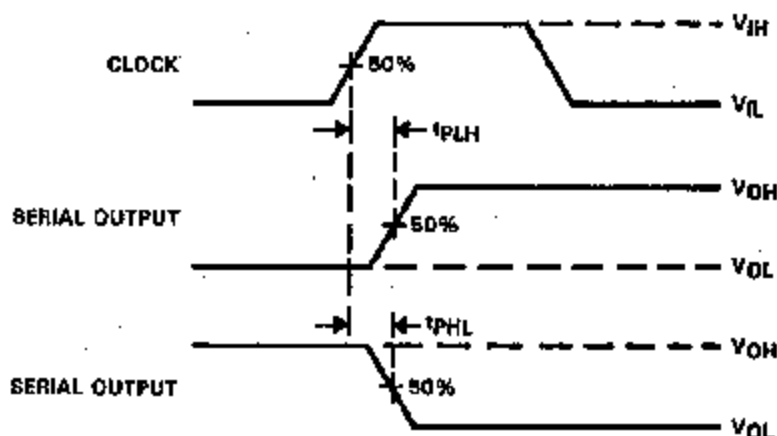

FIGURE 2. INPUT TIMING VOLTAGE WAVEFORMS

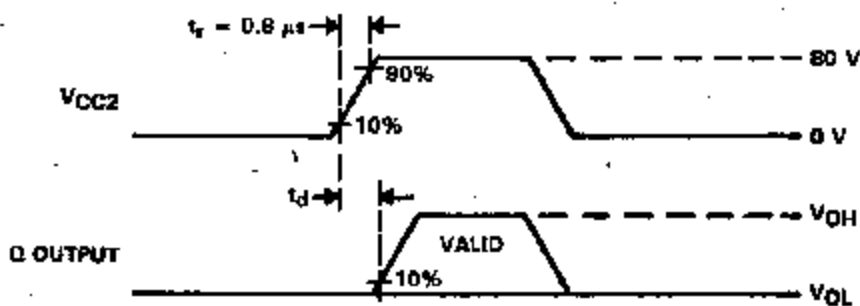FIGURE 3. VOLTAGE WAVEFORMS FOR PROPAGATION DELAY CLOCK TO SERIAL OUTPUT

FIGURE 4. VOLTAGE WAVEFORMS FOR DELAY TIMES, LATCH ENABLE TO Q OUTPUTS

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