

True +3.0V to +5.5V RS-232 Transceivers

- Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
- 250kbps Transmission Rate Under Load
- 1 μ A Low-Power Shutdown with Receivers Active (**SP3222B**)
- Interoperable with RS-232 down to +2.7V power source
- ESD Specifications:
±2kV Human Body Model



DESCRIPTION

The SP3222B/3232B series is an RS-232 transceiver solution intended for portable or handheld applications such as notebook or palmtop computers. The SP3222B/3232B series has a high-efficiency, charge-pump power supply that requires only 0.1 μ F capacitors in 3.3V operation. This charge pump allows the SP3222B/3232B series to deliver true RS-232 performance from a single power supply ranging from +3.0V to +5.5V. The ESD tolerance of the SP3222B/3232B devices are over \pm 15kV for both Human Body Model and IEC1000-4-2 Air discharge test methods. The SP3222B device has a low-power shutdown mode where the devices' driver outputs and charge pumps are disabled. During shutdown, the supply current falls to less than 1 μ A.

SELECTION TABLE

MODEL	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	Shutdown	TTL 3-State	No. of Pins
SP3222B	+3.0V to +5.5V	2	2	4	Yes	Yes	18, 20
SP3232B	+3.0V to +5.5V	2	2	4	No	No	16

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC} -0.3V to +6.0V
 $V+$ (NOTE 1) -0.3V to +7.0V
 $V-$ (NOTE 1) +0.3V to -7.0V
 $V+ + |V-|$ (NOTE 1) +13V

I_{CC} (DC V_{CC} or GND current) ± 100 mA

Input Voltages

$TxIN, \overline{EN}$ -0.3V to +6.0V
 $RxIN$ ± 25 V

Output Voltages

$TxOUT$ ± 13.2 V
 $RxOUT$ -0.3V to ($V_{CC} + 0.3$ V)

Short-Circuit Duration

$TxOUT$ Continuous

Storage Temperature -65°C to +150°C

Power Dissipation Per Package

20-pin SSOP (derate 9.25mW/°C above +70°C) 750mW
 18-pin PDIP (derate 15.2mW/°C above +70°C) 1220mW
 18-pin SOIC (derate 15.7mW/°C above +70°C) 1260mW
 20-pin TSSOP (derate 11.1mW/°C above +70°C) 890mW
 16-pin SSOP (derate 9.69mW/°C above +70°C) 775mW
 16-pin PDIP (derate 14.3mW/°C above +70°C) 1150mW
 16-pin Wide SOIC (derate 11.2mW/°C above +70°C) 900mW
 16-pin TSSOP (derate 10.5mW/°C above +70°C) 850mW
 16-pin nSOIC (derate 13.57mW/°C above +70°C) 1086mW

NOTE 1: $V+$ and $V-$ can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

NOTE 2: Driver Input hysteresis is typically 250mV.

SPECIFICATIONS

Unless otherwise noted, the following specifications apply for $V_{CC} = +3.0$ V to +5.5V with $T_{AMB} = T_{MIN}$ to T_{MAX} , C_1 to $C_4 = 0.1\mu$ F

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current		0.3	1.0	mA	no load, $T_{AMB} = +25^\circ\text{C}$, $V_{CC} = 3.3$ V, $TxIN = V_{CC}$ or GND
Shutdown Supply Current		1.0	10	μ A	$\overline{SHDN} = \text{GND}$, $T_{AMB} = +25^\circ\text{C}$, $V_{CC} = +3.3$ V, $TxIN = V_{CC}$ or GND
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW			0.8	V	$TxIN, \overline{EN}, \overline{SHDN}$, Note 2
Input Logic Threshold HIGH	2.0 2.4			V V	$V_{CC} = 3.3$ V, Note 2 $V_{CC} = 5.0$ V, Note 2
Input Leakage Current		± 0.01	± 1.0	μ A	$TxIN, \overline{EN}, \overline{SHDN}$, $T_{AMB} = +25^\circ\text{C}$, $V_{IN} = 0$ V to V_{CC}
Output Leakage Current		± 0.05	± 10	μ A	receivers disabled, $V_{OUT} = 0$ V to V_{CC}
Output Voltage LOW			0.4	V	$I_{OUT} = 1.6$ mA
Output Voltage HIGH	$V_{CC} - 0.6$	$V_{CC} - 0.1$		V	$I_{OUT} = -1.0$ mA
DRIVER OUTPUTS					
Output Voltage Swing	± 5.0	± 5.4		V	3k Ω load to ground at all driver outputs, $T_{AMB} = +25^\circ\text{C}$
Output Resistance	300			Ω	$V_{CC} = V+ = V- = 0$ V, $T_{OUT} = +2$ V
Output Short-Circuit Current		± 35	± 60	mA	$V_{OUT} = 0$ V
Output Leakage Current			± 25	μ A	$V_{OUT} = \pm 12$ V, $V_{CC} = 0$ V, or 3.0V to 5.5V, drivers disabled

SPECIFICATIONS (continued)

Unless otherwise noted, the following specifications apply for $V_{CC} = +3.0V$ to $+5.5V$ with $T_{AMB} = T_{MIN}$ to T_{MAX} , C_1 to $C_4 = 0.1\mu F$. Typical Values apply at $V_{CC} = +3.3V$ or $+5.5V$ and $T_{AMB} = 25^\circ C$.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RECEIVER INPUTS					
Input Voltage Range	-25		+25	V	
Input Threshold LOW	0.6 0.8	1.2 1.5		V	$V_{CC}=3.3V$ $V_{CC}=5.0V$
Input Threshold HIGH		1.5 1.8	2.4 2.4	V	$V_{CC}=3.3V$ $V_{CC}=5.0V$
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	k Ω	
TIMING CHARACTERISTICS					
Maximum Data Rate	250			kbps	$R_L=3k\Omega$, $C_L=1000pF$, one driver switching
Receiver Propagation Delay		0.15 0.15		μs	t_{PHL} , RxIN to RxOUT, $C_L=150pF$ t_{PLH} , RxIN to RxOUT, $C_L=150pF$
Receiver Output Enable Time		200		ns	
Receiver Output Disable Time		200		ns	
Driver Skew		100		ns	$ t_{PHL} - t_{PLH} $, $T_{AMB} = 25^\circ C$
Receiver Skew		50		ns	$ t_{PHL} - t_{PLH} $
Transition-Region Slew Rate			30	V/ μs	$V_{CC} = 3.3V$, $R_L = 3K\Omega$, $T_{AMB} = 25^\circ C$, measurements taken from $-3.0V$ to $+3.0V$ or $+3.0V$ to $-3.0V$

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for $V_{CC} = +3.3V$, 250kbps data rates, all drivers loaded with $3k\Omega$, $0.1\mu F$ charge pump capacitors, and $T_{AMB} = +25^{\circ}C$.

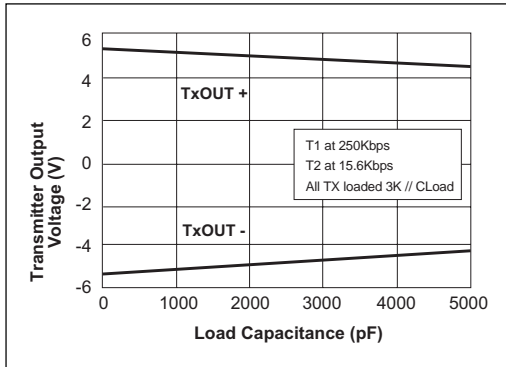


Figure 1. Transmitter Output Voltage vs Load Capacitance.

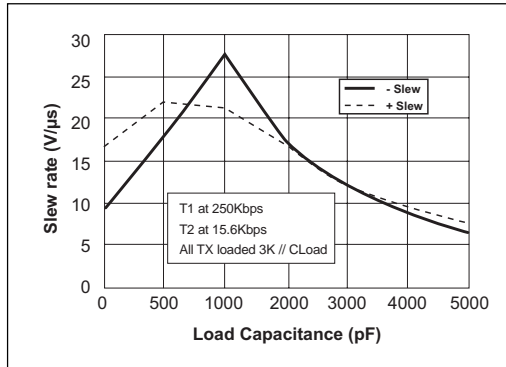


Figure 2. Slew Rate vs Load Capacitance.

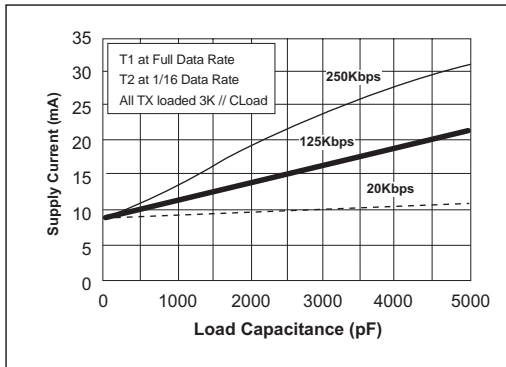


Figure 3. Supply Current vs Load Capacitance when Transmitting Data.

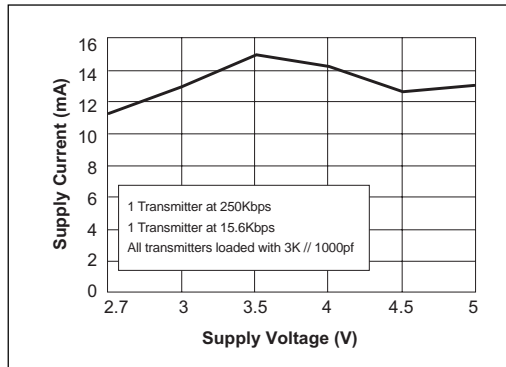


Figure 4. Supply Current vs Supply Voltage.

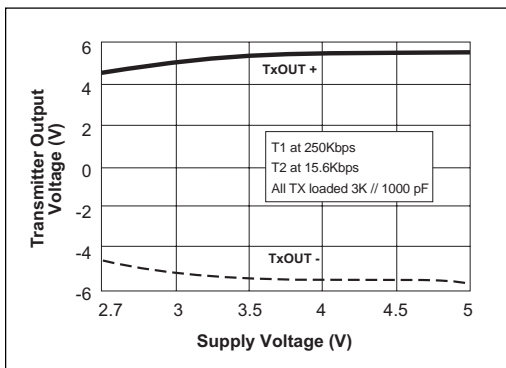


Figure 5. Transmitter Output Voltage vs Supply Voltage.

NAME	FUNCTION	PIN NUMBER		
		SP3222B		SP3232B
		DIP/SO	SSOP TSSOP	
$\overline{\text{EN}}$	Receiver Enable. Apply logic LOW for normal operation. Apply logic HIGH to disable the receiver outputs (high-Z state).	1	1	-
C1+	Positive terminal of the voltage doubler charge-pump capacitor.	2	2	1
V+	+5.5V generated by the charge pump.	3	3	2
C1-	Negative terminal of the voltage doubler charge-pump capacitor.	4	4	3
C2+	Positive terminal of the inverting charge-pump capacitor.	5	5	4
C2-	Negative terminal of the inverting charge-pump capacitor.	6	6	5
V-	-5.5V generated by the charge pump.	7	7	6
T1OUT	RS-232 driver output.	15	17	14
T2OUT	RS-232 driver output.	8	8	7
R1IN	RS-232 receiver input.	14	16	13
R2IN	RS-232 receiver input.	9	9	8
R1OUT	TTL/CMOS receiver output.	13	15	12
R2OUT	TTL/CMOS receiver output.	10	10	9
T1IN	TTL/CMOS driver input.	12	13	11
T2IN	TTL/CMOS driver input.	11	12	10
GND	Ground.	16	18	15
V _{CC}	+3.0V to +5.5V supply voltage	17	19	16
$\overline{\text{SHDN}}$	Shutdown Control Input. Drive HIGH for normal device operation. Drive LOW to shutdown the drivers (high-Z output) and the on-board power supply.	18	20	-
N.C.	No Connect.	-	11, 14	-

Table 1. Device Pin Description

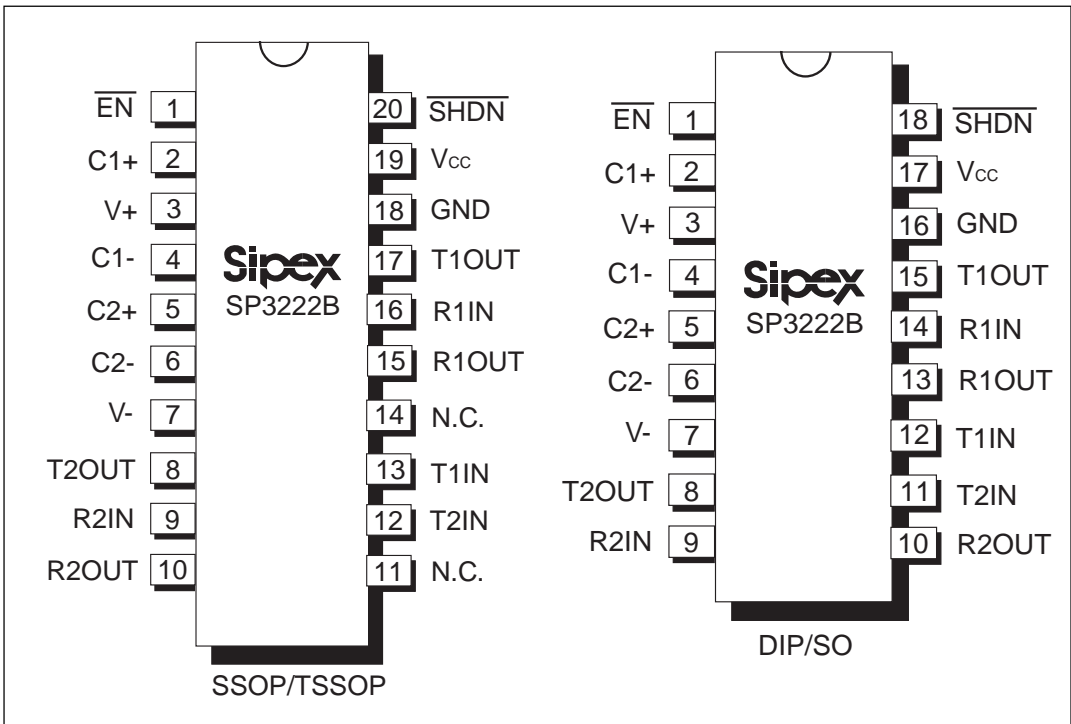


Figure 6. Pinout Configurations for the SP3222B

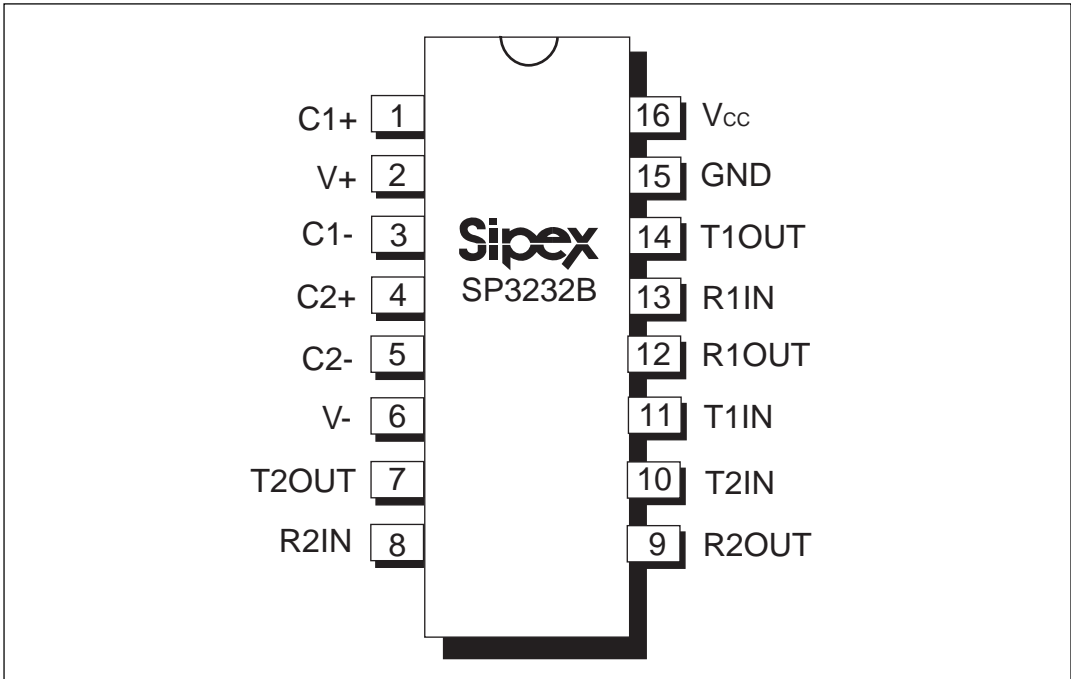


Figure 7. Pinout Configuration for the SP3232B

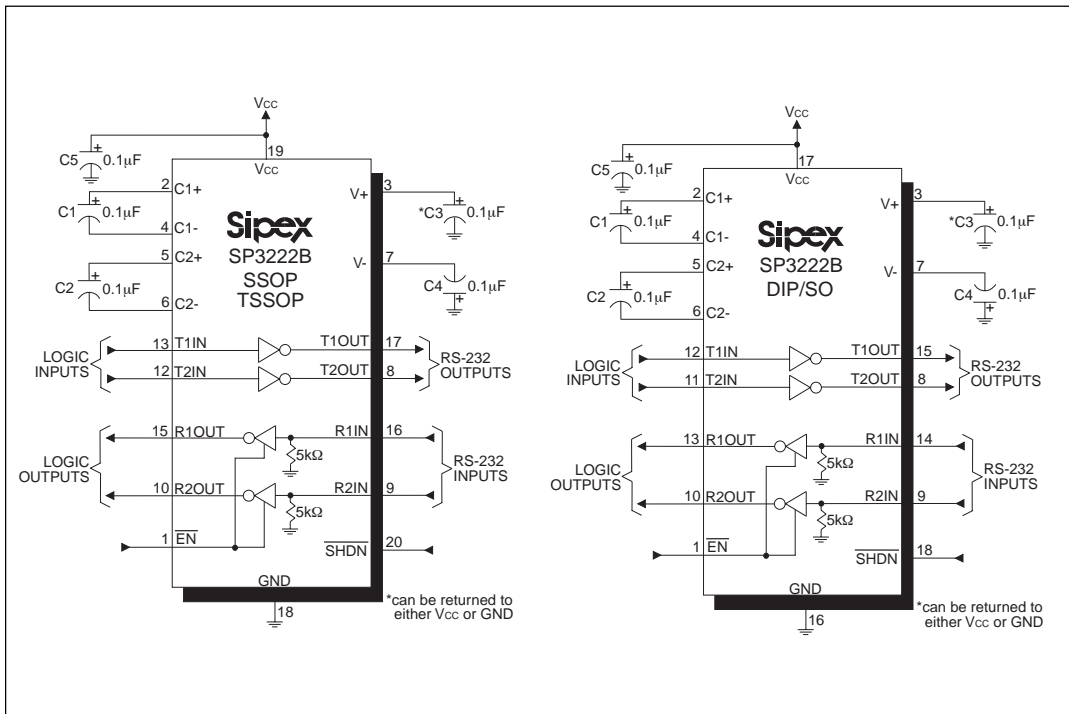


Figure 8. SP3222B Typical Operating Circuits

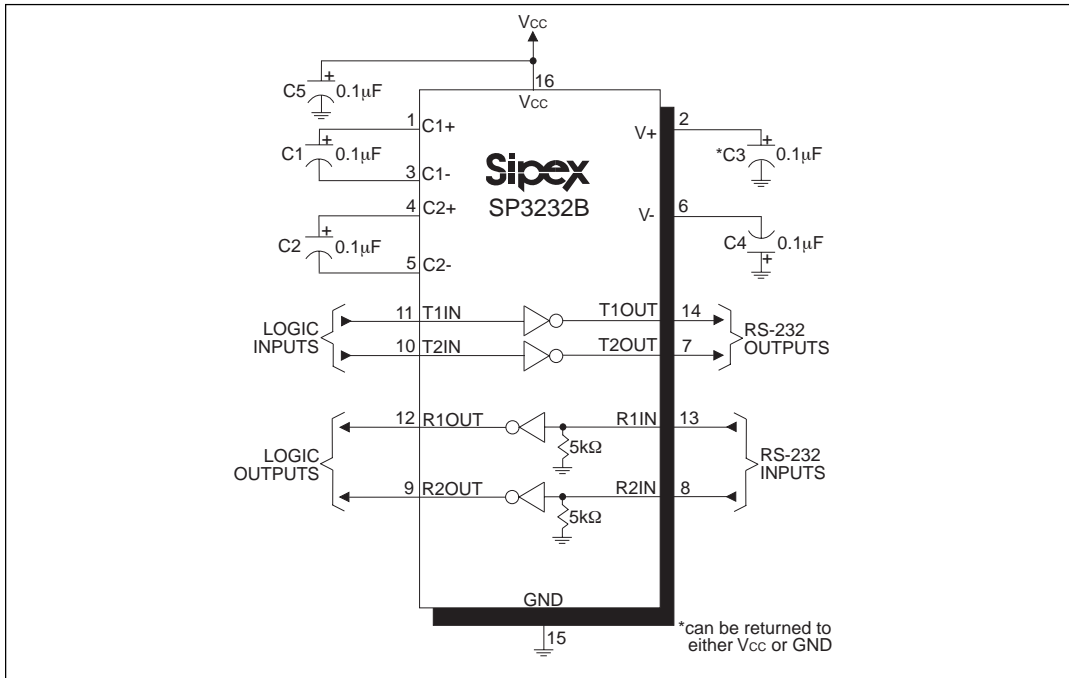


Figure 9. SP3232B Typical Operating Circuit

DESCRIPTION

The **SP3222B/3232B** transceivers meet the EIA/TIA-232 and V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The **SP3222B/3232B** devices all feature Sipex's proprietary on-board charge pump circuitry that generates $2 \times V_{CC}$ for RS-232 voltage levels from a single +3.0V to +5.5V power supply. This series is ideal for +3.3V-only systems, mixed +3.3V to +5.5V systems, or +5.0V-only systems that require true RS-232 performance. The **SP3222B/3232B** series have drivers that operate at a typical data rate of 250kbps fully loaded.

The **SP3222B** and **SP3232B** are 2-driver/2-receiver devices ideal for portable or hand-held applications. The **SP3222B** features a $1\mu\text{A}$ shutdown mode that reduces power consumption and extends battery life in portable systems. Its receivers remain active in shutdown mode, allowing external devices such as modems to be monitored using only $1\mu\text{A}$ supply current.

THEORY OF OPERATION

The **SP3222B/3232B** series are made up of three basic circuit blocks: 1. Drivers, 2. Receivers, and 3. the Sipex proprietary charge pump.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to $\pm 5.0\text{V}$ EIA/TIA-232 levels inverted relative to the input logic levels. Typically, the RS-232 output voltage swing is $\pm 5.5\text{V}$ with no load and at least $\pm 5\text{V}$ minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. Driver outputs will meet EIA/TIA-562 levels of $\pm 3.7\text{V}$ with supply voltages as low as 2.7V .

The drivers can guarantee a data rate of 250kbps fully loaded with $3\text{K}\Omega$ in parallel with 1000pF , ensuring compatibility with PC-to-PC communication software.

The slew rate of the driver output is internally limited to a maximum of $30\text{V}/\mu\text{s}$ in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

Figure 10 shows a loopback test circuit used to the RS-232 drivers. *Figure 11* shows the test results of the loopback circuit with all drivers active at 120kbps with RS-232 loads in parallel with 1000pF capacitors. *Figure 12* shows the test results where one driver was active at 250kbps and all drivers loaded with an RS-232 receiver in parallel with a 1000pF capacitor. A solid RS-232 data transmission rate of 250kbps provides compatibility with many designs in personal computer peripherals and LAN applications.

The **SP3222B** driver's output stages are turned off (tri-state) when the device is in shutdown mode. When the power is off, the **SP3222B** device permits the outputs to be driven up to $\pm 12\text{V}$. The driver's inputs do not have pull-up resistors. Designers should connect unused inputs to V_{CC} or GND.

In the shutdown mode, the supply current falls to less than $1\mu\text{A}$, where $\overline{\text{SHDN}} = \text{LOW}$. When the **SP3222B** device is shut down, the device's driver outputs are disabled (tri-stated) and the charge pumps are turned off with V_+ pulled down to V_{CC} and V_- pulled to GND. The time required to exit shutdown is typically $100\mu\text{s}$. Connect $\overline{\text{SHDN}}$ to V_{CC} if the shutdown mode is not used.

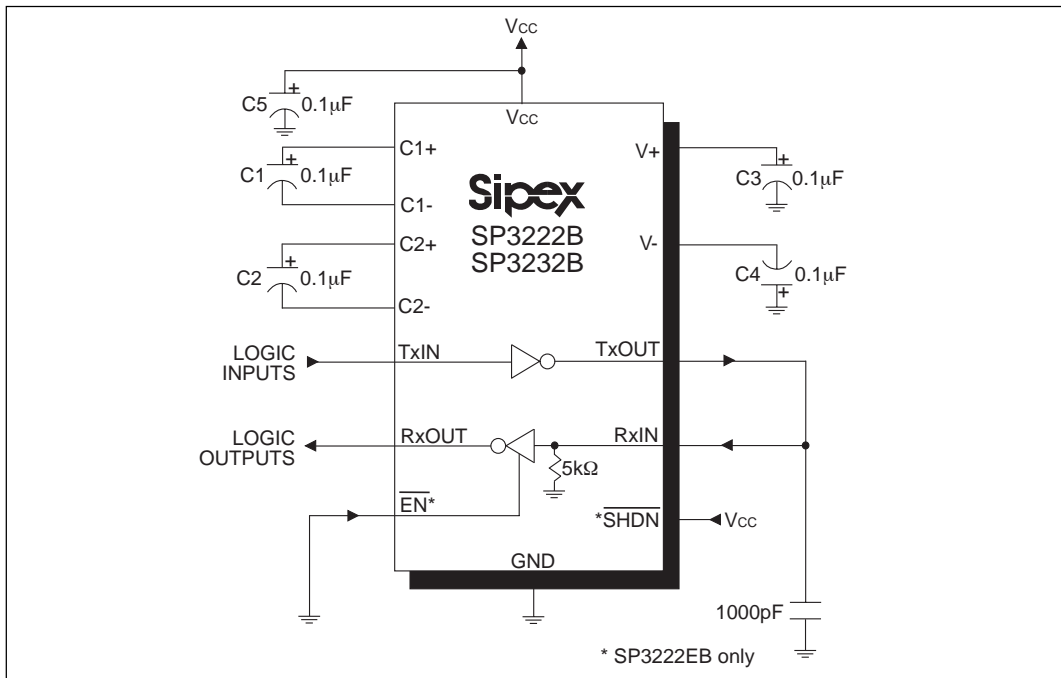


Figure 10. SP3222B/3232B Driver Loopback Test Circuit

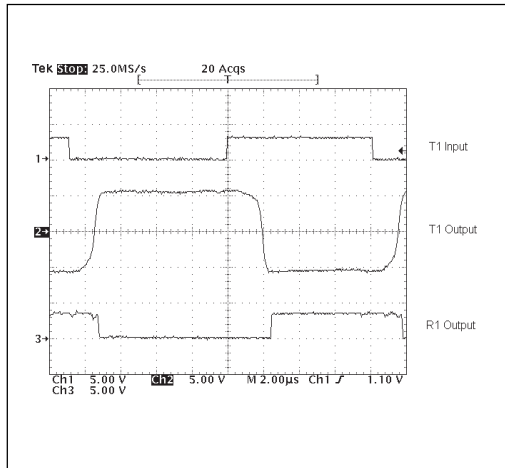


Figure 11. Driver Loopback Test Results at 120kbps

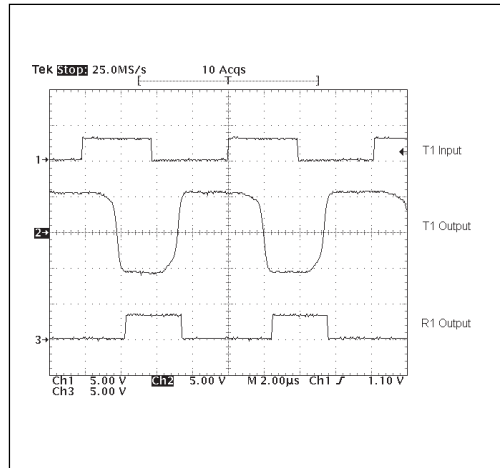


Figure 12. Driver Loopback Test Results at 250kbps

Receivers

The receivers convert EIA/TIA-232 levels to TTL or CMOS logic output levels. The SP3222B receivers have an inverting tri-state output. These receiver outputs (RxOUT) are tri-stated when the enable control $\overline{\text{EN}} = \text{HIGH}$. In the shutdown mode, the receivers can be active or inactive. $\overline{\text{EN}}$ has no effect on TxOUT. The truth table logic of the **SP3222B** driver and receiver outputs can be found in *Table 2*.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, a 5k Ω pull-down resistor to ground will commit the output of the receiver to a HIGH state.

Charge Pump

The charge pump is a **Sipex**-patented design (5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage (V_{CC}) over the +3.0V to +5.5V range.

In most circumstances, decoupling the power supply can be achieved adequately using a 0.1 μF bypass capacitor at C5 (refer to *Figures 8 and 9*).

$\overline{\text{SHDN}}$	$\overline{\text{EN}}$	TxOUT	RxOUT
0	0	Tri-state	Active
0	1	Tri-state	Tri-state
1	0	Active	Active
1	1	Active	Tri-state

Table 2. SP3222B Truth Table Logic for Shutdown and Enable Control

In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor of the same value as charge-pump capacitor C1. Physically connect bypass capacitors as close to the IC as possible.

The charge pumps operate in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pumps are enabled. If the output voltage exceed a magnitude of 5.5V, the charge pumps are disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC} . C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^- . Since C_2^+ is connected to V_{CC} , the voltage potential across capacitor C_2 is now 2 times V_{CC} .

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3 . This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3 , the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{\text{CC}}$ in the negative terminal of C_1 , which is applied to the negative side of capacitor C_2 . Since C_2^+ is at V_{CC} , the voltage potential across C_2 is 2 times V_{CC} .

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4 , the V_{DD} storage capacitor.

This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4 , the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC} ; in a no-load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 250kHz. The external capacitors can be as low as 0.1 μ F with a 16V breakdown voltage rating.

ESD Tolerance

The **SP3222B/3232B** series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electrostatic discharges and associated transients.

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electrostatic energy and discharge it to an integrated circuit.

The simulation is performed by using a test model as shown in *Figure 18*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

For the Human Body Model, the current limiting resistor (R_s) and the source capacitor (C_s) are 1.5k Ω and 100pF, respectively.

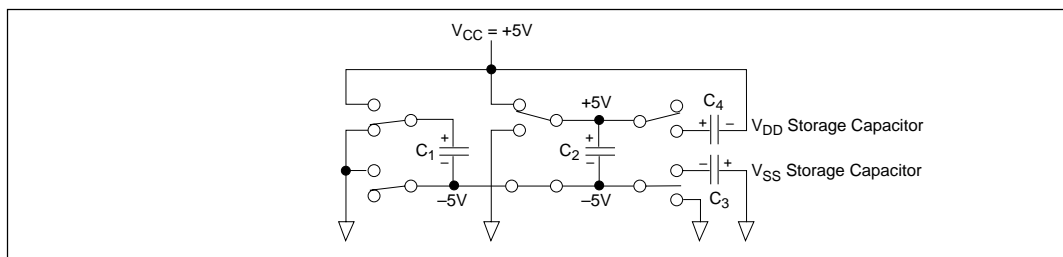


Figure 13. Charge Pump — Phase 1

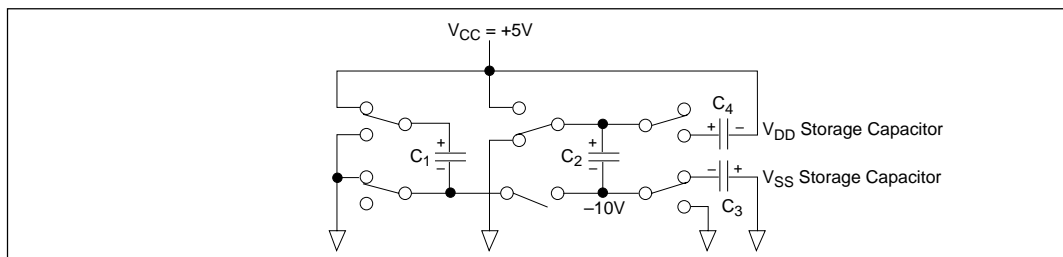


Figure 14. Charge Pump — Phase 2

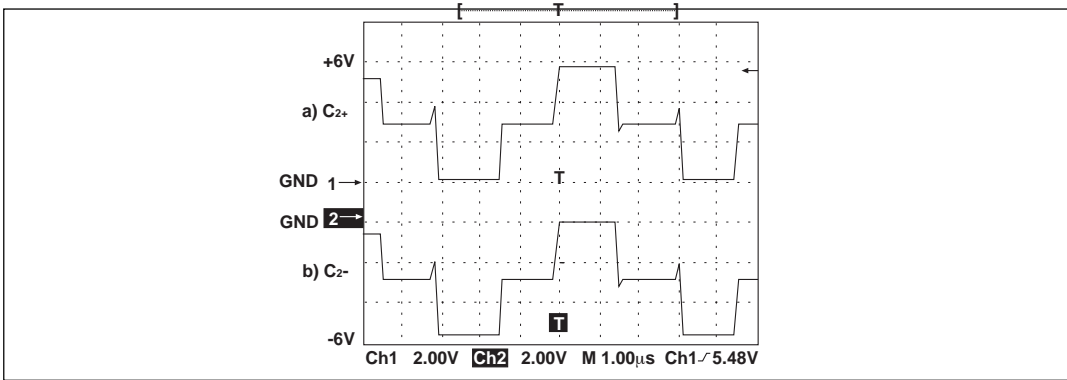


Figure 15. Charge Pump Waveforms

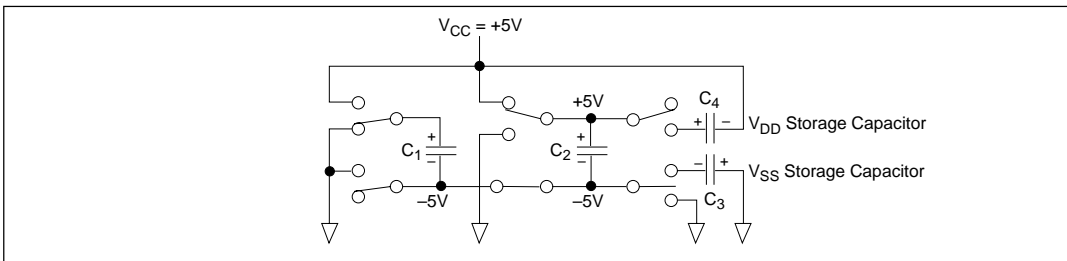


Figure 16. Charge Pump — Phase 3

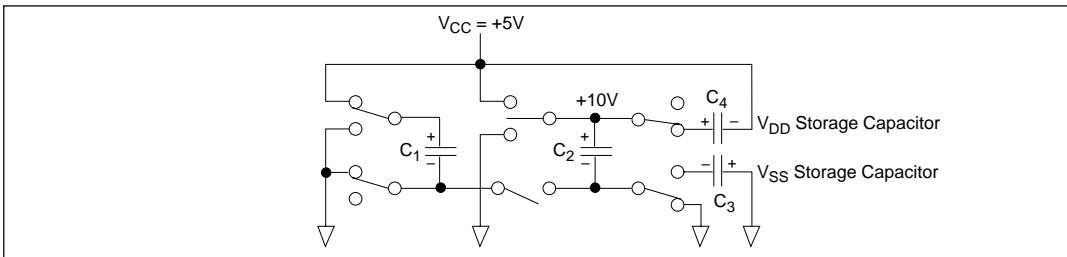


Figure 17. Charge Pump — Phase 4

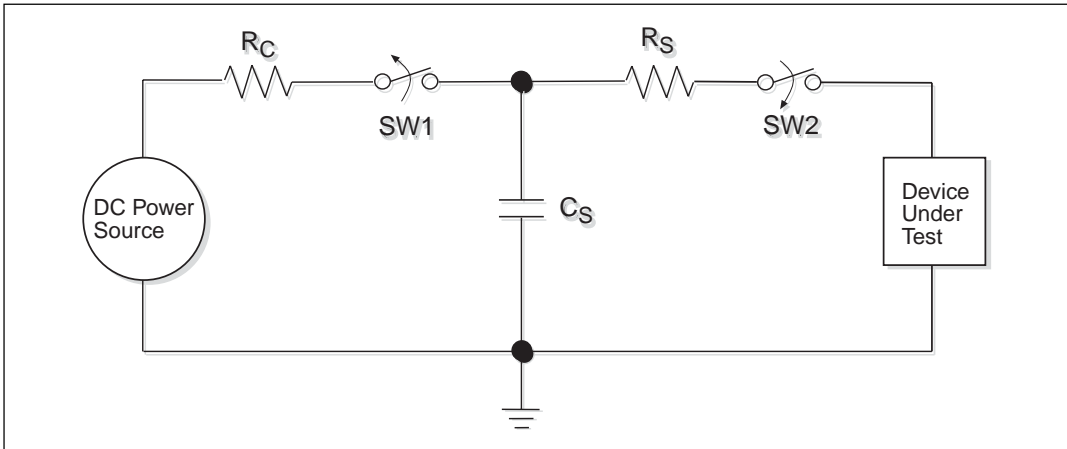
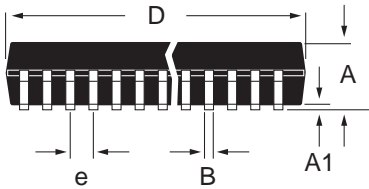
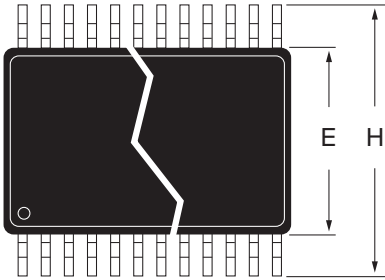


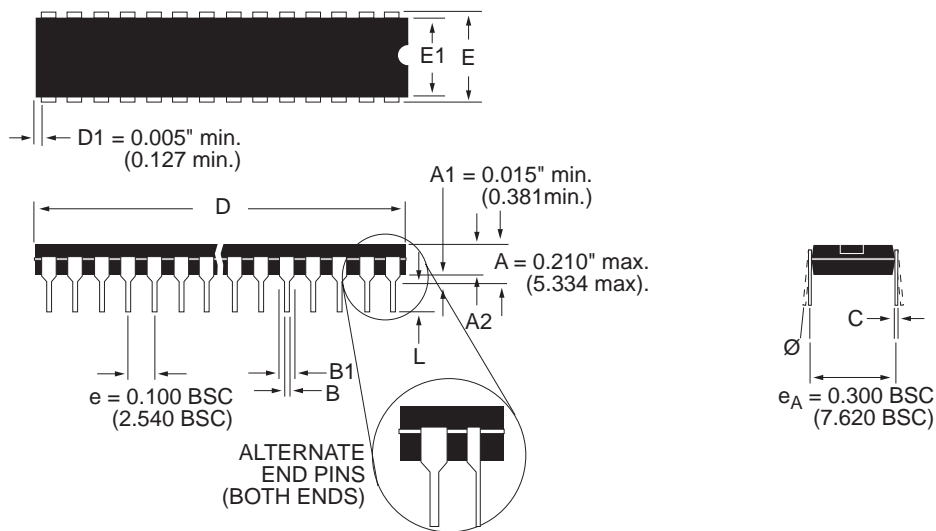
Figure 18. ESD Test Circuit for Human Body Model

PACKAGE: PLASTIC SHRINK SMALL OUTLINE (SSOP)



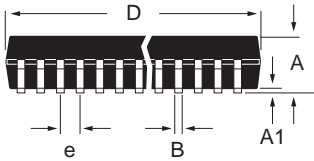
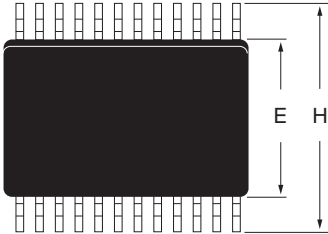
DIMENSIONS (Inches) Minimum/Maximum (mm)	16-PIN	20-PIN
A	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)
A1	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)
B	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)
D	0.239/0.249 (6.07/6.33)	0.278/0.289 (7.07/7.33)
E	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)
e	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)
H	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)
L	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)

PACKAGE: PLASTIC DUAL-IN-LINE (NARROW)



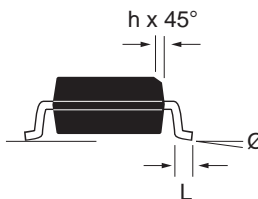
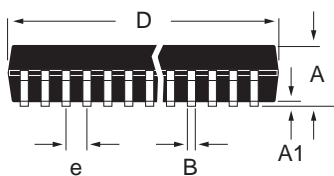
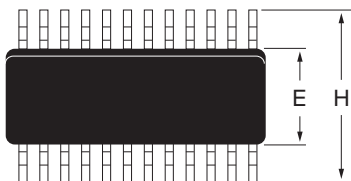
DIMENSIONS (Inches) Minimum/Maximum (mm)	16-PIN	18-PIN
A2	0.115/0.195 (2.921/4.953)	0.115/0.195 (2.921/4.953)
B	0.014/0.022 (0.356/0.559)	0.014/0.022 (0.356/0.559)
B1	0.045/0.070 (1.143/1.778)	0.045/0.070 (1.143/1.778)
C	0.008/0.014 (0.203/0.356)	0.008/0.014 (0.203/0.356)
D	0.780/0.800 (19.812/20.320)	0.880/0.920 (22.352/23.368)
E	0.300/0.325 (7.620/8.255)	0.300/0.325 (7.620/8.255)
E1	0.240/0.280 (6.096/7.112)	0.240/0.280 (6.096/7.112)
L	0.115/0.150 (2.921/3.810)	0.115/0.150 (2.921/3.810)
\emptyset	0°/ 15° (0°/15°)	0°/ 15° (0°/15°)

**PACKAGE: PLASTIC
SMALL OUTLINE (SOIC)
(WIDE)**



DIMENSIONS (Inches) Minimum/Maximum (mm)	16-PIN	18-PIN
A	0.090/0.104 (2.29/2.649)	0.090/0.104 (2.29/2.649)
A1	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)
D	0.398/0.413 (10.10/10.49)	0.447/0.463 (11.35/11.74)
E	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)

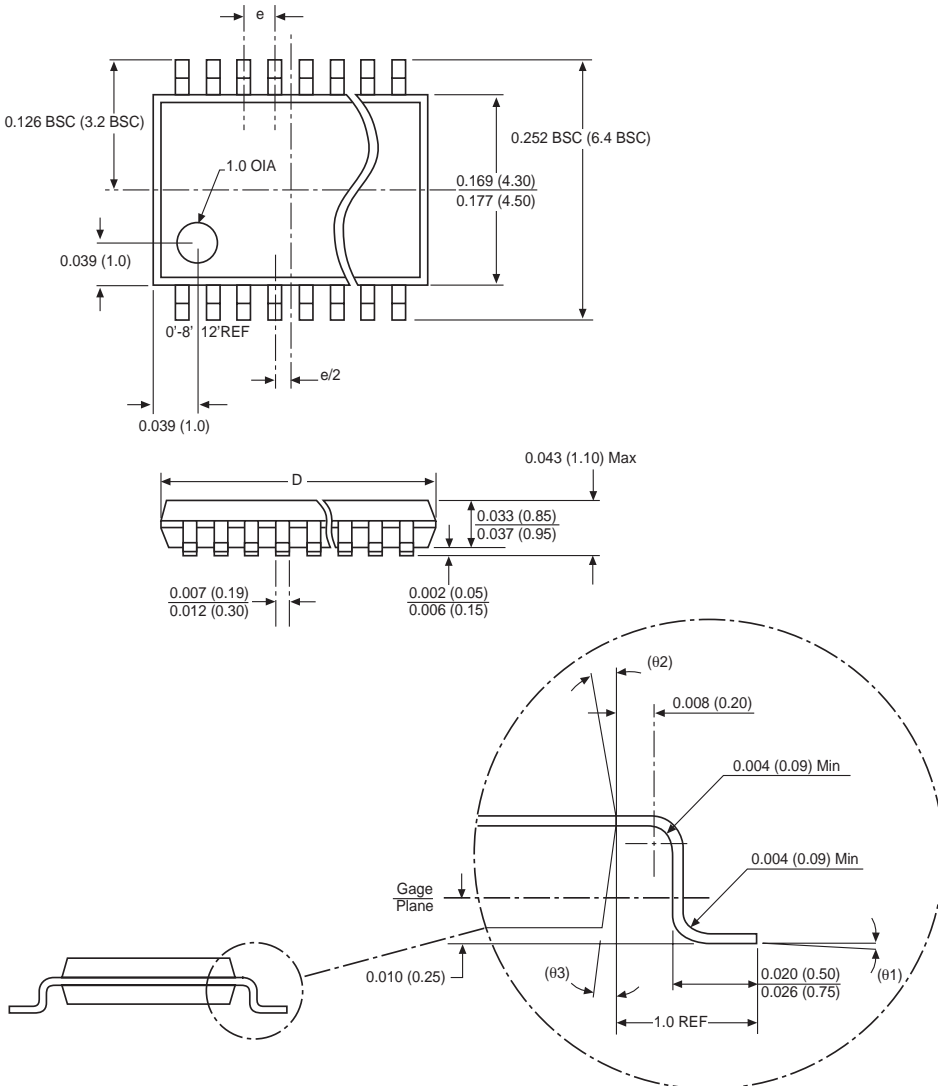
**PACKAGE: PLASTIC
SMALL OUTLINE (SOIC)
(NARROW)**



DIMENSIONS (Inches) Minimum/Maximum (mm)	16-PIN
A	0.053/0.069 (1.346/1.748)
A1	0.004/0.010 (0.102/0.249)
B	0.013/0.020 (0.330/0.508)
D	0.386/0.394 (9.802/10.000)
E	0.150/0.157 (3.802/3.988)
e	0.050 BSC (1.270 BSC)
H	0.228/0.244 (5.801/6.198)
h	0.010/0.020 (0.254/0.498)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

PACKAGE: PLASTIC THIN SMALL OUTLINE (TSSOP)

DIMENSIONS						
in inches (mm) Minimum/Maximum						
Symbol	14 Lead	16 Lead	20 Lead	24 Lead	28 Lead	38 Lead
D	0.193/0.201 (4.90/5.10)	0.193/0.201 (4.90/5.10)	0.252/0.260 (6.40/6.60)	0.303/0.311 (7.70/7.90)	0.378/0.386 (9.60/9.80)	0.378/0.386 (9.60/9.80)
e	0.026 BSC (0.65 BSC)	0.026 BSC (0.65 BSC)	0.026 BSC (0.65 BSC)	0.026 BSC (0.65 BSC)	0.026 BSC (0.65 BSC)	0.020 BSC (0.50 BSC)



ORDERING INFORMATION

Model	Temperature Range	Package Type
SP3222BCA	0°C to +70°C	20-Pin SSOP
SP3222BCP	0°C to +70°C	18-Pin PDIP
SP3222BCT	0°C to +70°C	18-Pin WSOIC
SP3222BCY	0°C to +70°C	20-Pin TSSOP
SP3222BEA	-40°C to +85°C	20-Pin SSOP
SP3222BEP	-40°C to +85°C	18-Pin PDIP
SP3222BET	-40°C to +85°C	18-Pin WSOIC
SP3222BEY	-40°C to +85°C	20-Pin TSSOP
SP3232BCA	0°C to +70°C	16-Pin SSOP
SP3232BCP	0°C to +70°C	16-Pin PDIP
SP3232BCT	0°C to +70°C	16-Pin WSOIC
SP3232BCN	0°C to +70°C	16-Pin nSOIC
SP3232BCY	0°C to +70°C	16-Pin TSSOP
SP3232BEA	-40°C to +85°C	16-Pin SSOP
SP3232BEP	-40°C to +85°C	16-Pin PDIP
SP3232BET	-40°C to +85°C	16-Pin WSOIC
SP3232BEN	-40°C to +85°C	16-Pin nSOIC
SP3232BEY	-40°C to +85°C	16-Pin TSSOP

Please consult the factory for pricing and availability on a Tape-On-Reel option.



ANALOG EXCELLENCE

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