DATA SHEET

凌陽科技
SUNPLUS

SPMC802B

32-pin General Purpose Microcontroller (OTP)

AUG. 07, 2002

Version 1.0

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32-PIN GENERAL PURPOSE MICROCONTROLLER (OTP)

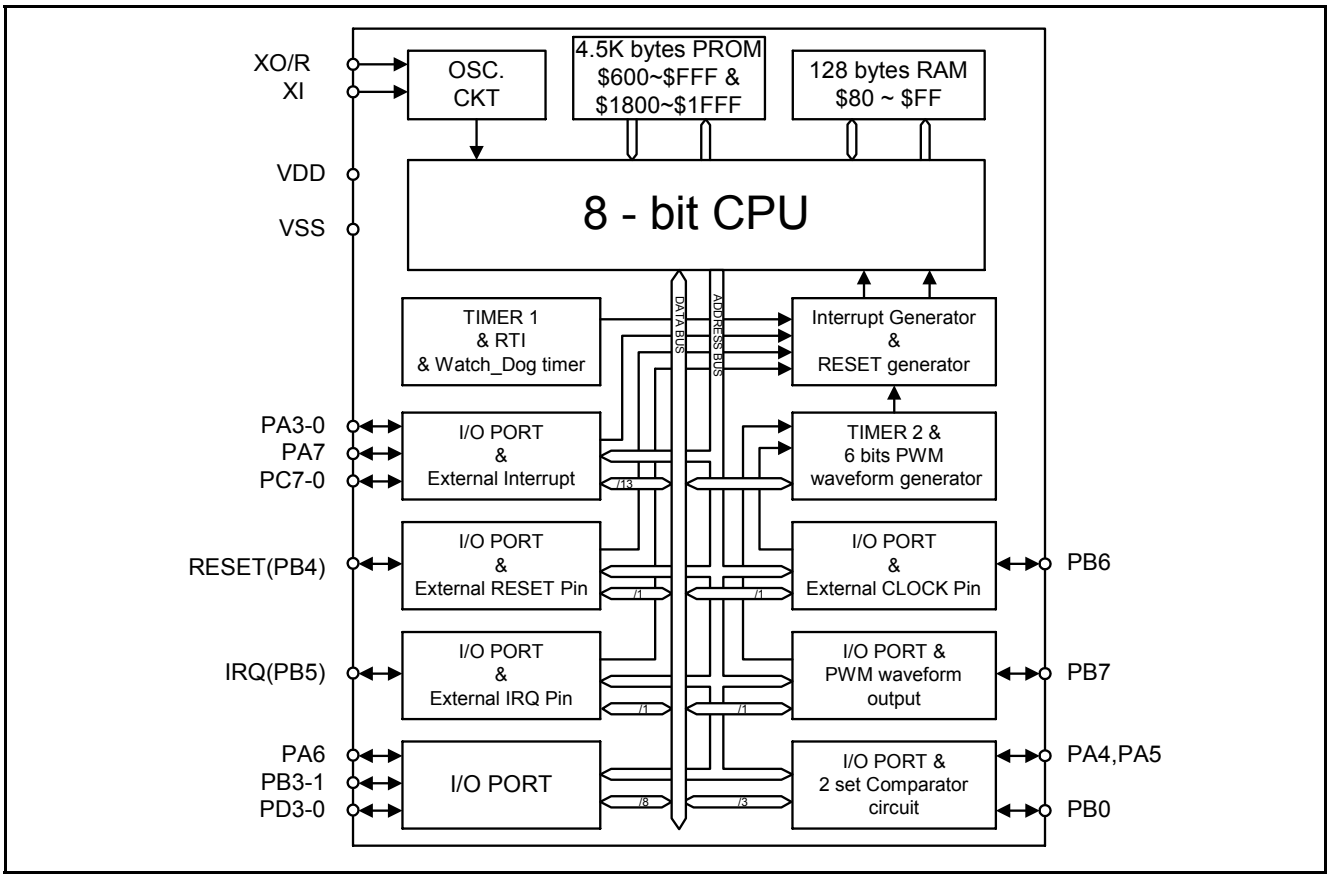
1. GENERAL DESCRIPTION

The SPMC802B is an OTP version of SPMC02A with reliability enhancement. It equips with an 8-bit Sunplus CPU core, 4.5K bytes of program ROM, and 128 bytes of RAM. SPMC802B also combines with four I/O ports, two timers with one PWM output, two Comparator inputs, and a Watchdog Timer. Three groups of interrupt are implemented for different kinds of applications. Major application fields are small home appliances or computer peripheral applications. The details are described below.

2. FEATURES

- Built-in 8-bit Sunplus CPU core with two index registers and up to 6MHz clock operation.
- 28 general-purpose I/O channels that are belong to four I/O ports. Some of them are combined with the options to select Pull-Up/Down Resistors.
- Three external interrupt groups, one is come from individual I/O Channel PB5 and group input PA3:0, one is come from individual I/O Channel, PA7, and one is a group input, PC port.
- External Reset input option on PB4.
- An 8-bit Timer with Real Time Interrupt control.
- An 8-bit Re-loadable Timer with 8 stages prescalar.
- One 6-bit PWM waveform output.
- Two voltage Comparator inputs with selectable internal or external voltage reference. An interrupt event control for the compare result.
- A watchdog timer for program control.
- 4.5K bytes of ROM with 128 bytes of RAM.
- R-Oscillation or Crystal input options for system clock.
- Stop or Wait Control setting for Power-Saving Mode.
- Slow Transition Output Pins.

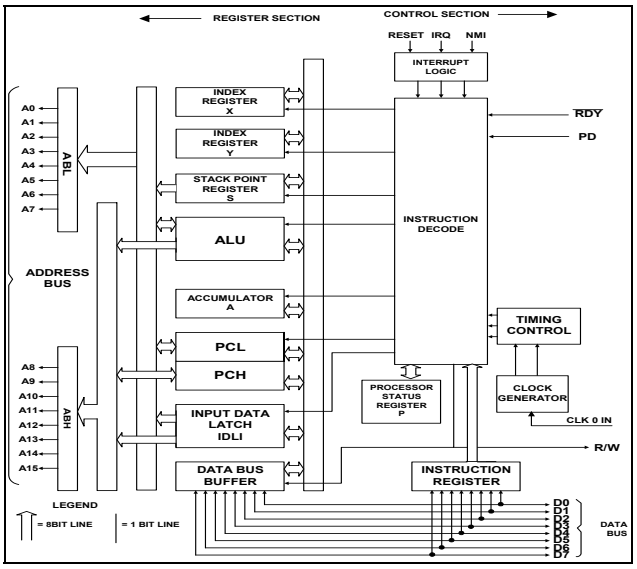
3. BLOCK DIAGRAM



3.1. CPU

The microprocessor of SPMC802B is a SUNPLUS high performance processor equipped with Accumulator, Program Counter, X Register, Y Register, Stack Pointer and Processor Status Register (The same as 6502 instruction's structure). SPMC802B is a fully static CMOS design. The oscillation frequency could be varied up to 6.0MHz depends on the application needs.

3.1.1. Block diagram of Sunplus CPU



3.2. Memory

3.2.1. Memory map

SPMC802B Supports 4.5K bytes of EPROM with 512 bytes test ROM. It also has the configurable options can be programmed by writer for different applications. The addresses for EPROM, test ROM, and options are located in $0400h ~ $0FFFh and $1800h ~ $1FFFh. The RAM area is located in $0080h ~ $00FFh. The functional control registers and I/O control registers are located in $0000h ~ $0013h. A set of system control registers can be configured through indexed access addresses $003Eh and $003Fh. The buffers for stack pointer are started from $01FFh with downward direction. This area is mirrored to the RAM area $00FFh ~ $0080h. A system control register named Stack Limit Register (SLR) is used to limit the Stack area to prevent the override of the normal operating contents in the RAM. Once the Stack is over the limiter, CPU reset will be generated.

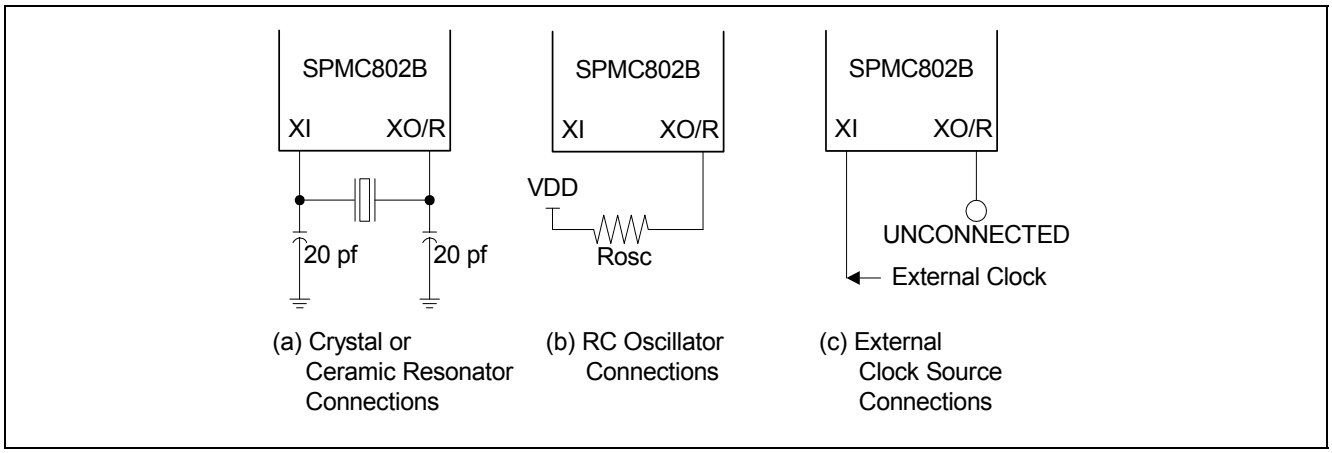
To prevent the illegal accesses on undefined addresses, there is a qualification block to limit the accesses. The illegal accesses will generate the CPU reset to restart the program.

3.2.2. NMI, Reset, IRQ vectors

The address of NMI (not provided in this chip), RESET and IRQ are located from $1FFA to $1FFF. The interrupt vectors should be specified in the program to have proper operation.

3.3. Oscillator

The SPMC802B supports AT-cut parallel resonant oscillated Crystal /Resonator, or RC oscillator, or external clock sources by configurable option (select one from those three types). The design of application circuit should follow the vendors' specifications or recommendations. The diagram listed below represents typical X'TAL/ROSC circuits for most applications:



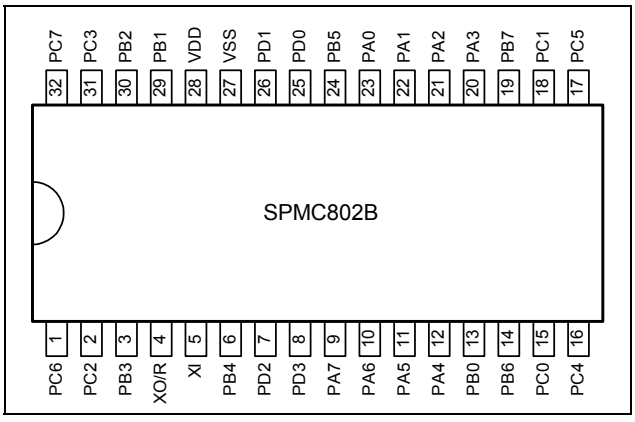
4. SIGNAL DESCRIPTIONS

4.1. PIN Descriptions (32 PIN)

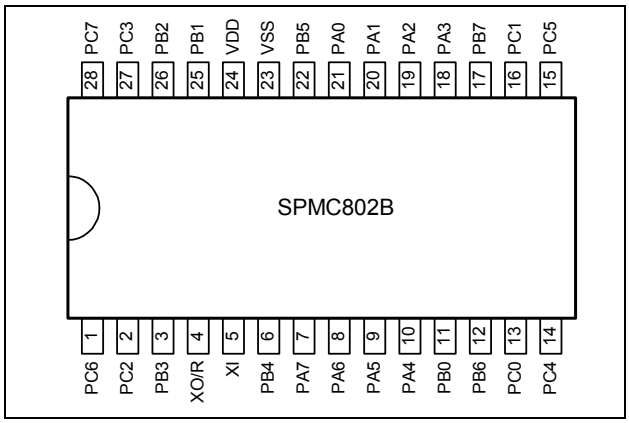
Mnemonic	PIN No.	Functional Description
VDD	28	*System Power Supply.*
VSS	27	*System Ground*.
XO/R	4	*Crystal In or Resistor In Input*. An external resistive pull-up is used to connect with internal OSC circuitry for generating the internal clock and the related time base in R-Oscillation mode. It will be connected with external crystal for a crystal oscillation circuitry in crystal mode.
XI	5	*Crystal Output or External Clock Input*. External clock input is used to connect with internal clock circuitry to generate the internal clock and the related time base in External clock mode. It will be connected with external crystal for a crystal oscillation circuitry in crystal mode.
PA7:0	9, 10, 11, 12 20, 21, 22, 23	*GPIO Port A7:0*. General-purpose inputs/outputs. Using the internal setting can configure it. In addition, PA7 can be used as the external interrupt input. PA5:4 can be the compare inputs of Comparator. PA3:0 can be the group input of external interrupt.
PB5 (V_{pp})	24	*GPIO Port B5*. General-purpose input/output. Using the internal setting can configure it. In addition, PB5 can be used as the external Main IRQ input. It is used as Programming Voltage input in Programming mode.
PB1 (SCK)	29	*GPIO Port B1*. General-purpose input/output. Using the internal setting can configure it. In addition, it is used as Serial Clock input in Programming mode.
PB0 (SDA)	13	*GPIO Port B0*. General-purpose input/output or the voltage reference input for the Comparator. Using the internal setting can configure it. In addition, it is used as Serial Data input/output in Programming mode.
PB7:6,4:2	19, 14, 6, 3, 30	*GPIO Port B7:6,4:2*. General-purpose inputs/output. Using the internal setting can configure it. In addition, PB7 can be the PWM waveform output. PB6 can be set as external event/clock input for Timer 2. PB4 can be used as the Main nRESET input.
PC7:0	32, 1, 17, 16 31, 2, 18, 15	*GPIO Port C7:0*. General-purpose inputs/outputs. Using the internal setting can configure it. In addition, these pins can be used as the external interrupt inputs.
PD3:0	8, 7, 26, 25	*GPIO Port D3:0*. General-purpose inputs/outputs. Using the internal setting can configure it.

4.2. PIN Assignment

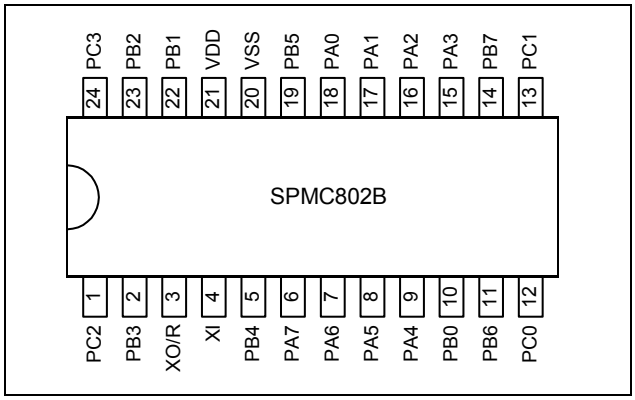
4.2.1. 32 PIN package



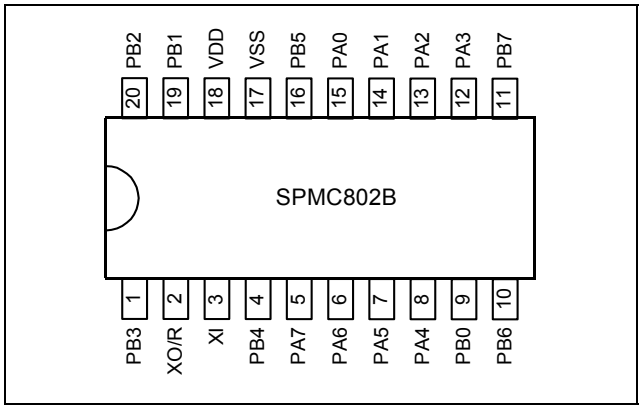
4.2.2. 28 PIN package



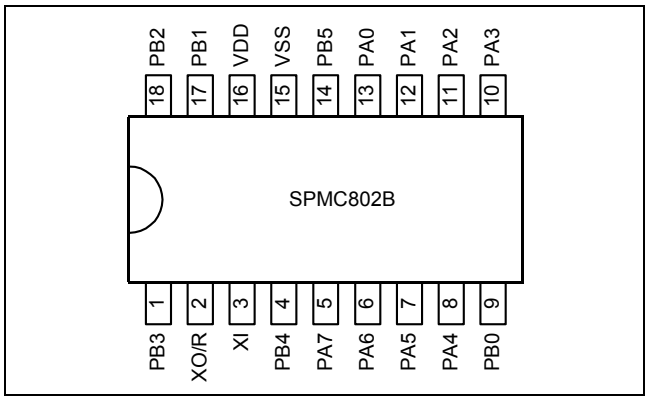
4.2.3. 24 PIN package



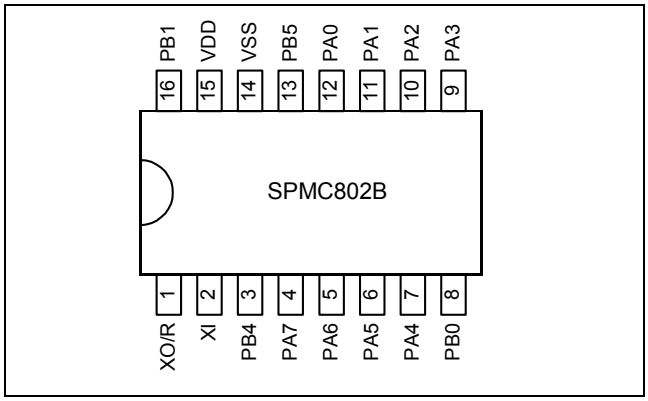
4.2.4. 20 PIN package



4.2.5. 18 PIN package



4.2.6. 16 PIN package



5. FUNCTIONAL DESCRPITIONS

SPMC802B is an OTP for SPMC02A emulating. The functional blocks have two kinds of control input. The first one is configurable option. The other is programmable register. Configurable options are used as permanent assignment. They are configured with the program code in the same time. Once the configurable options are written to SPMC802B, they are unchangeable as the program code. The configurable options are described in detail later. Programmable registers are used to control the functional blocks by the program. The program can access the registers to achieve the desire functions.

There are two kinds of registers with different access methods. The first kind of registers uses direct access as normal. The second kind of registers uses indexed write access for specific function. They are summarized as following. All of the function registers will be set to 0 (except *rt1* and *rt0* in ***TCS1***), when a reset signal occurred. The bits *rt1* and *rt0* will be set to 1 when a reset signal occurred.

5.1. Port A Group

The I/O port A has 8 programmable I/Os that are controlled by data register PA, direction control register DPA, and pull-up/down resistance control register RPA. DPA is used to control the pad I/O attribute. Setting the bit(s) to '1' will enforce the corresponding pad(s) to output mode. It is a write-only register. PA is used to store the data contents for output. Reading PA will get the stored data when corresponding bit of DPA is set as output mode, or will get the pad status if it is in input mode.

There is a built-in Pull-Up/Down resistor on each pad. PA7:6 have pull-up resistors that is permanent in SPMC802B. PA5:4 can be configured with pull-up or pull-down resistors. These configurable pull-up/down resistors should be selected or enabled by configurable option first, and then can be controlled by users' program through RPA.

The output mode on PA7:6 can be programmed as slow transition outputs. Programming the bit **slowe** in RPA to '1' will enforce the output high to low transition time to 250ns ± 20% with 500pf pad loading at 2.0MHz CPU frequency.

PA7 and PA3:0 are used as external interrupt inputs. The more details are described in section Interrupt. PA5:4 are used as voltage compare inputs for Comparator function. They are analog inputs to provide source voltage inputs. The more details are described in section Comparator.

The corresponding pads are assigned for SPMC802B as following: (VDD = 5.0V)

PIN	Rp	IN	OUT	Special Function
PA7	5K Up Always	Schmitt-Trigger	-/8mA	IRQ1 interrupt input
PA6	5K Up Always	Schmitt-Trigger	-/8mA	
PA5	100K Up/Down@rpa5		8/8mA	CMP1 compare input
PA4	100K Up/Down@rpa4		8/8mA	CMP0 compare input
PA3	100K Up/Down@rpa3		8/8mA	IRQ0 interrupt input
PA2	100K Up/Down@rpa2		8/8mA	IRQ0 interrupt input
PA1	100K Up/Down@rpa1		8/8mA	IRQ0 interrupt input
PA0	100K Up/Down@rpa0		8/8mA	IRQ0 interrupt input

5.2. Port B Group

The I/O port B has 8 programmable I/Os that are controlled by data register PB, direction control register DPB, and pull-up/down resistance control register RPB. DPB is used to control the pad I/O attribute. Setting the bit(s) to '1' will enforce the corresponding pad(s) to output mode. It is a write-only register. PB is used to store the data contents for output. Reading PB will get the stored data when corresponding bit of DPB is set as output mode, or will get the pad status if it is in input mode.

There is a built-in Pull-Up/Down resistor on each pad except PB5. PB7, PB6, PB3, and PB0 can be configured with pull-up or pull-down resistors. These configurable pull-up/down resistors should be selected by configurable option first, and then can be controlled by users' program through RPB. PB5 does not have the internal resistor. For interrupt input on PB5, an external pull-up resistor is needed to maintain the interrupt function. PB4, PB2, and PB1 have pull-up resistors. They can be controlled by users' program through RPB.

In SPMC802B, the output mode on PB2 and PB1 can be an open-drain pin with slow transition by program. To achieve the slow transition function, programming the bit **slowe** in RPA to '1' will enforce the output high to low transition time to 250ns ± 20% with 50pf pad loading at 2.0MHz CPU frequency.

PB7 can be a PWM waveform output. PB6 can be an external clock or event input for Timer2. PB5 is used as external interrupt input with falling-edge trigger. PB4 can be used as external active-low reset input by enabling the configurable option. PB0 can be reference voltage input for Comparator function. In case of using PB0 as external reference voltage input, the resistive pull-up/down should be disabled. The more details are described in related sections.

The corresponding pads are assigned for SPMC802B as following: (VDD = 5.0V)

PIN	Rp	IN	OUT	Special Function
PB7	100K Up/Down@rpb7		8/8mA	PWM waveform output
PB6	100K Up/Down@rpb6		8/8mA	External clock/event input
PB5	No Pull-Up/Down	Schmitt-Trigger	-/8mA	IRQ0 interrupt input
PB4	100K Up@rpb4	Schmitt-Trigger	8/8mA	External nRESET input
PB3	100K Up/Down@rpb3		8/8mA	
PB2	100K Up@rpb2		-/20mA	
PB1	100K Up@rpb1		-/20mA	
PB0	100K Up/Down@rpb0		8/8mA	Comparator Vref input

5.3. Port C Group

The I/O port C has 8 programmable I/Os that are controlled by data register PC, direction control register DPC, and pull-up/down resistance control register RPC. DPC is used to control the pad I/O attribute. Setting the bit(s) to '1' will enforce the corresponding pad(s) to output mode. It is a write-only register. PC is used to store the data contents for output. Reading PC will get the stored data when corresponding bit of DPC is set as output mode, or will get the pad status if it is in input mode.

There is a built-in Pull-Up/Down resistor on each pad. These pull-up/down resistors should be selected either pull-up or pull-down by configurable option first, and then can be controlled by users' program through RPC.

PC7:0 are used as external interrupt inputs. The more details are described in section Interrupt.

The corresponding pads are assigned for SPMC802B as following: (VDD = 5.0V)

PIN	Rp	IN	OUT	Special Function
PC7	100K Up/Down@rpc7		8/8mA	IRQ2 interrupt input
PC6	100K Up/Down@rpc6		8/8mA	IRQ2 interrupt input
PC5	100K Up/Down@rpc5		8/8mA	IRQ2 interrupt input
PC4	100K Up/Down@rpc4		8/8mA	IRQ2 interrupt input
PC3	100K Up/Down@rpc3		8/8mA	IRQ2 interrupt input
PC2	100K Up/Down@rpc2		8/8mA	IRQ2 interrupt input
PC1	100K Up/Down@rpc1		8/8mA	IRQ2 interrupt input
PC0	100K Up/Down@rpc0		8/8mA	IRQ2 interrupt input

5.4. Port D Group

The I/O port D has 4 programmable I/Os that are controlled by data register PD, direction control register DPD, and pull-up/down resistance control register RPD. DPD is used to control the pad I/O attribute. Setting the bit(s) to '1' will enforce the corresponding pad(s) to output mode. It is a write-only register. PD is used to store the data contents for output. Reading PD will get the stored data when corresponding bit of DPD is set as output mode, or will get the pad status if it is in input mode.

There is a built-in Pull-Up resistor on each pad. These pull-up resistors can be controlled by users' program through RPD.

The corresponding pads are assigned for SPMC802B as following: (VDD = 5.0V)

PIN	Rp	IN	OUT	Special Function
PD3	100K Up@rpd3		8/8mA	
PD2	100K Up@rpd2		8/8mA	
PD1	100K Up@rpd1		8/8mA	
PD0	100K Up@rpd0		8/8mA	

5.5. Interrupt

There are four kinds of interrupt, Software Interrupt, External Interrupt, Timer Interrupt, and Comparator interrupt. Each of the last three interrupts has individual status (occurred or not) and control (enable or not) registers, whereas Software Interrupt does not. In general, once an interrupt event occurs, the corresponding flag bit will be set. If the related interrupt control bit is set to enable interrupt, an interrupt request signal will be generated and will be dealt with by CPU for service. The interrupt flag bits must be cleared in the interrupt service routine to prevent program from deadlock in interrupt service routine.

Software interrupt is generated by the instruction BRK. The BRK is an executable instruction interrupt; it is executed regardless of the state of the I-bit in the Processor Status Register Flag (inside CPU). It jumps to interrupt routine when BRK occurred. As with any instruction, interrupts pending during the previous instruction is served.

External interrupts are coming from IRQ0, IRQ1, or IRQ2. These IRQ signals are combined with the configurable options and status/control registers to generate the interrupt events to CPU. For all IRQ channels, each channel has individual interrupt control or status bits. Once an external interrupt is occurred, the flag will be set and stays at set unless user software clears the flag. The interrupt request signal will be generated in case of the interrupt is enabled. Channel IRQ0 has a configurable option used to set the trigger mode of the interrupt event. The trigger mode can be selected as either edge trigger mode or level trigger mode. When the interrupt channel is enabled with edge trigger mode, an active transition edge on the external interrupt inputs will generate the interrupt. If the channel is enabled with level trigger mode, the active level of the external interrupt inputs will set the interrupt event until the active level condition is removed. IRQ1 and IRQ2 support edge trigger mode only.

The external interrupt IRQ0 supports interrupt-flag-bit auto-clearing function. It is activated only when interrupt channels of IRQ1 is disabled. When the auto-clearing function is activated, the flag of IRQ0 will be cleared automatically as soon as the interrupt vector is accessed. The user software in interrupt service routine does no need to check the flag because that flag bit has been cleared by hardware. It is used to simplify the interrupt service routine only when the IRQ0 is the unique interrupt source of the system. If the Timer interrupts or Comparator interrupts are enabled with only IRQ0 being enabled as external interrupt source, the external interrupt event due to IRQ0 might be lost in case two interrupt events occur in the same time. To avoid the problem of IRQ0 loss, using IRQ1 or IRQ2 for external interrupt channel, instead of using IRQ0, can solve it. However, no matter the auto-clearing function of interrupt flag is functional, user software must clear the interrupt occurrence in the interrupt service routine.

There is a new configurable option, named irqac, to be added for future supporting. This option can disable the auto-clearing function of IRQ0 interrupt flag. The program tool to maintain the body consistency will control it.

In SPMC802B, IRQ0 is come from either PB5 with falling-edge trigger or group input PA3:0 with rising-edge trigger. A configurable option is used to activate the group interrupt input on PA3:0. IRQ1 is come from PA7. IRQ2 is come from external interrupt group input, PC7:0.

The Timer 1 interrupt and the Comparator interrupt will be described in detail in section Timer1 & Real Time Interrupt and section Comparator.

5.6. Timer1 & Real Time Interrupt

The clock input (XI/XO/R pins), f_{OSC}, is internally divided by two to generate CPU clock, f_{CPU}, for whole system. Timer 1 clock, f_{TM1}, is come from CPU clock with the divisor either 1 or 4 setting by configurable option. The timer clock is fed into an 8-bit free-run timer built as Timer 1 function. Timer 1 Count Register (TCR1) is used to read out the current counting value of Timer 1. Once TCR1 is overflow, it will set the corresponding flag and will generate interrupt for service if the interrupt input is enabled.

The additional counting stages perform the Power On Reset (POR) cycle for clock settling down during power up, the Real Time Interrupt (RTI) function for timing applications, and watchdog Timer for function recovery. The POR and WDT functions are described in detail in section WDT & Reset.

For Real Time Interrupt, there is a pre-scalar to perform the periodic timing events. The pre-scalar is defined below. The timing events will set the flag and will generate interrupt for service if the interrupt is enabled.

rt1:0	RTI Rate			WDT Reset time (=RTI/8)		
	Divisor	$f_{TM1}=f_{CPU}/1$*	$f_{TM1}=f_{CPU}/4$*	Divisor	$f_{TM1}=f_{CPU}/1$*	$f_{TM1}=f_{CPU}/4$*
00	2048	2.048ms	8.192ms	16384	16.384ms	66ms
01	4096	4.096ms	16.384ms	32768	32.768ms	131ms
10	8192	8.192ms	32.768ms	65536	66ms	262ms
11	16384	16.384ms	65.536ms	131072	131ms	524ms

Note1: In this example, the CPU clock is f_{CPU} = 1.0MHz (f_{OSC} = 2.0MHz).
Note2: *The f_{TM1} is selected by configurable option ***fsel***.

5.7. Timer2 & PWM

Timer 2 is a re-loadable 8-bit timer. It consists with an 8-bit prescale counter, a pre-load register, an 8-bit count-up counter, and a control block. The base clock input for Timer 2 f_{TIN2} can be either from CPU clock f_{CPU}, or from external clock through PB6. It is fed into an 8-bit prescale counter to generate the Timer 2 clock, f_{TM2}. The prescalar for Timer 2 clock is set as 2 to the power of the value. An 8-bit counter with a Pre-load Register consist the main counter of Timer 2. Timer 2 Count Register (TCR2) is used to set up the pre-load value in write mode and to read out the current counting value in read mode. Once the Timer 2 clock is enabled, main counter will count up. When Timer 2 rolls over from $FF to pre-load data, it generates overflow signal and reloads the pre-load data into the counting stage and counts up again. The overflow signal will also generate interrupt for service if the interrupt function is enabled.

The PWM waveform generator consists with a 3-duty cycle PWM generator, a 64-duty cycle PWM generator, and a control block for PWM waveform output to PB7. The general I/O function on PB7 will be disabled while the PWM output is enabled. There are two kinds of waveform output can be selected, fixed 3-duty cycle waveform output and programmable 64-duty cycle waveform output. The overflow signal of Timer 2, is the base clock of PWM generator. It will feed into the 3-duty cycle waveform generator and the 64-duty cycle waveform generator.

5.8. Comparator

SPMC802B is built with two channels of voltage Comparator. It can compare the external voltage input coming from PA4 or PA5 with the external voltage reference set up on PB0, or with the internal voltage reference (1.24V). These two channels Comparator can be enabled with the setup of comparison criterion and the reference source, and selectable interrupt input for event service. The input operating range of the Comparator is 0.2V to (VDD-0.2)V.

5.9. WAIT & STOP Mode

There are two kinds of clock control mode supported by SPMC802B as WAIT mode and STOP mode.

The WAIT mode function will disable CPU clock but leave the timer clock active, if the bit **wait** is set as '1'. Once the system being entered the WAIT mode, the activated interrupt events will recover the normal operation immediately from the next address of WAIT mode interrupt point. To confirm the interrupt events can wake up the CPU, the corresponding interrupt enable bits must be set before entering the WAIT mode.

The STOP mode function will disable whole system clock, if the bit **stop** is set as '1'. Once the system being entered the STOP mode, only the activated external interrupt events (from I/Os) can

recover the normal operation from the next address of STOP mode interrupt point with 1024 f_{TM1} clock cycle recovery time for stable oscillation. To confirm the external interrupt events can wake up the system, the corresponding interrupt enable bits must be set before entering the STOP mode.

There are two write paths. One is come from direct write mode through address $0008, another is come from indexed write mode through indexed address $08. The purpose for the dual write paths is for backward compatibility. The option incap is used to inhibit the STOP function coming from the direct write cycle of SNW to improve the system reliability. The indexed write for this register will be described in detail later.

5.10. Reset

There are five kinds of reset resource for the system, Power On Reset (POR), External Reset (PB4), Low Voltage Reset (LVR), Watchdog Timer Reset (WDT), and Illegal Address Reset (IAR). These reset sources can be concluded as external events and internal events. The external events are come from the power line, or external trigger event. The internal events are come from the program exceptions or internal software reset event.

5.11. Reset Management Registers

There are four registers implemented for reset event management, Stack Limit Register (SLR), System Guard Register (SGR), System Control Register (SCR), and System Stop & Wait Register (SNW). The read of these registers uses direct access. Reading the registers through page 0 addresses can get the contents directly. A specific write cycle, named indexed write cycle, is implemented to have higher reliability of content updates. The indexed addresses for these registers are same as the direct addresses used in read cycle.

5.11.1. Indexed write cycle

The procedure of indexed write cycle is formed with two consecutive write cycle of page 0. Only a write with address $003E, called write-index cycle, followed with a write with address $003F, called write-data cycle, can program the reset management registers. The intersections in between these two write cycles are allowed only for the code pre-fetches, means ROM area read cycles. If a ROM-write cycle or an access cycle neither a ROM-read cycle nor a write-data cycle is executed after the write-index cycle, the indexed write cycle will be abnormal terminated without any data updates on these registers.

To prevent abnormal termination of the indexed write cycle, programmers should handle the cycle much carefully. The interrupts should be disabled to prevent unpredicted intersections.

6. ELECTRICAL CHARACTERISTICS

6.1. Item Definition

Symbol	Definition	Symbol	Definition
V_{IH}	Input High Voltage	I_{OH}	Output High Current (Source)
V_{IL}	Input Low Voltage	I_{OL}	Output Low Current (Sink)
V_{TH}	Input Threshold Voltage	I_Z	Output Leakage Current (Source)
SF_V	Frequency Stability	R_P	Pull-Up/Down Resistance
DF_V	Frequency Deviation		

6.2. Absolute Maximum Rating

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Condition
Storage Temperature	T_{STR}	-40	-	125	ºC	
Operating Ambient Temperature	T_{OPR}	0	-	70	ºC	
Voltage Rating on Input	V_{IN}	-0.3	-	VDD +0.3	V	
Voltage Rating on VDD		-0.3	-	7.0	V	
Output Voltage	V_{OUT}	0	-	VDD	V	

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.3. Recommended Operating Conditions

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Supply Voltage	VDD	3.0	-	5.5	V	
CPU Clock (Internal CPU clock)	f_{CPU}	200K	-	6.0M	Hz	VDD = 5.0V
Power Consumption	I_{DD}	-	5.0	-	mA	f_{CPU} = 6.0MHz @ VDD = 5.0V
Power Down Current*	I_{PD}	-	-	10	μA	VDD = 5.0V
Power Up Initial Voltage	V_{INIT}	-	-	0.5	V	
Power On Reset Time	t_{POR}	50	-	-	ms	VDD starts from V_{INIT}
LVR Trigger Voltage	V_{LVR}	-	2.2	-	V	

Note: The power-down current is measured in SLEEP mode with all I/O pins in hi-impedance state and tied to VDD or VSS.

6.4. PIN Attribute Description (VDD = 5.0V, T_A = 0ºC~70ºC)

Mnemonic	Description	Symbol	Min.	Typ.	Max.	Unit	Condition
XI, XO	Special Input Cell Pair for RC oscillation	SF_V	-	-	±5.0	%	$(f_{5.5V}-f_{4.5V})/f_{5.0V}$ *
		DF_V	-	-	±10	%	VDD = 5.0V
		R_P	-	27	-	KΩ	$f_{CPU\_5.0V}$ = 6.0MHz
PA7:6	Input with Schmitt Trigger with Fixed Pull-Up R 8mA Open-Drain Output	V_{IH}	2.0	-	-	V	
		V_{IL}	-	-	0.8	V	
		I_{OL}	8.0	-	-	mA	V_{OL} = 0.5V
		I_P	-	1.0	-	mA	V_{IN} = VSS
PA5:0 PB7:6, 3, 0 PC7:0	Input with Pull-Up/Down option 8mA Output	V_{IH}	3.5	-	-	V	
		V_{IL}	-	-	1.4	V	
		I_{OH}	8.0	-	-	mA	V_{OH} = 2.4V
		I_{OL}	8.0	-	-	mA	V_{OL} = 0.5V
		I_P	-	50	-	μA	V_{IN} = VDD or VSS
PB5	Input with Schmitt Trigger	V_{IH}	2.4	-	-	V	

Mnemonic	Description	Symbol	Min.	Typ.	Max.	Unit	Condition
	8mA Open-Drain Output	V_{IL}	-	-	0.8	V	
		I_{OL}	8.0	-	-	mA	V_{OL} = 0.5V
PB4	Input with Schmitt Trigger with Pull-Up R 8mA Output	V_{IH}	2.0	-	-	V	
		V_{IL}	-	-	0.8	V	
		I_{OH}	8.0	-	-	mA	V_{OH} = 2.4V
		I_{OL}	8.0	-	-	mA	V_{OL} = 0.5V
		R_P	70	100	130	KΩ	V_{IN} = VSS = 0V
PB2:1	Input with Pull-Up R 20mA Open-Drain Output	V_{IH}	3.5	-	-	V	
		V_{IL}	-	-	1.4	V	
		I_{OL}	20	-	-	mA	V_{OL} = 0.5V
		I_P	-	50	-	μA	V_{IN} = VSS = 0V
PD3:0	Input with Pull-Up R 8mA Output	V_{IH}	3.5	-	-	V	
		V_{IL}	-	-	1.4	V	
		I_{OH}	8.0	-	-	mA	V_{OH} = 2.4V
		I_{OL}	8.0	-	-	mA	V_{OL} = 0.5V
		I_P	-	50	-	μA	V_{IN} = VSS = 0V
All	I/O Port Hi-Z Leakage	I_Z	-	-	10	μA	R_P inactive
LVR	Threshold Voltage	V_{LVR}	2.1	2.2	2.3	V	Enable option
	Operating Current	I_{LVR}	-	20	-	μA	
Compare	Input Hysteresis Voltage	V_{HYS}	-	30	-	mV	
	Input Common Mode Voltage	V_{ICM}	0.2	-	VDD -0.2	V	
	CMRR	C_{MRR}	50	-	-	dB	
	Response Time**	t_{CV}	-	-	400	ns	
	Compare Mode Change to Output Valid***	t_{CON}	-	-	10	μs	
	Operating Current	I_{CMP}	-	-	10	μA	per Channel

Note1: *The frequency defined in this item is based on the CPU frequency. It is one-half of the oscillation frequency.

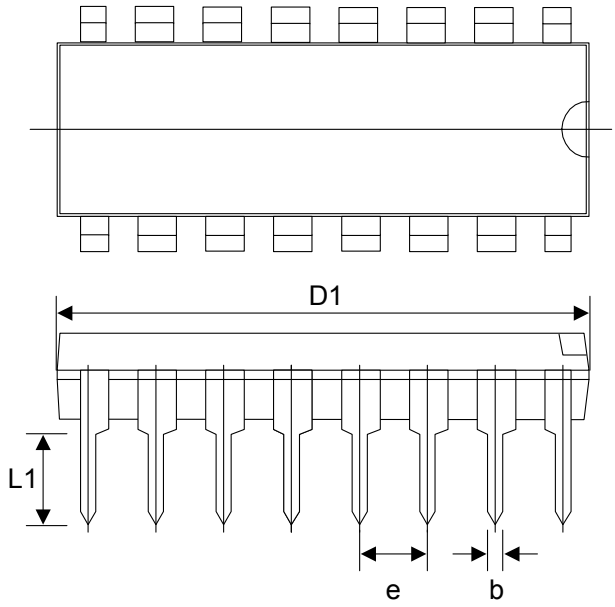
Note2: ** Response time measured with one comparator input at VDD/2, while the other input transitions from VSS to VDD.

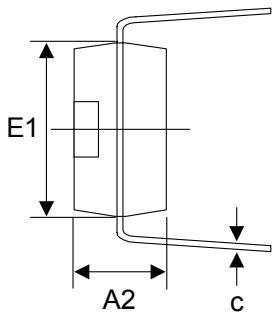
Note3: *** t_{CON} measured with Compare mode enable to output valid, while the internal reference voltage is selected from disable to enable and same setup of comparator inputs as the item t_{CV}.

7. PACKAGE/PAD LOCATIONS

7.1. Package Information

7.1.1. PDIP 16





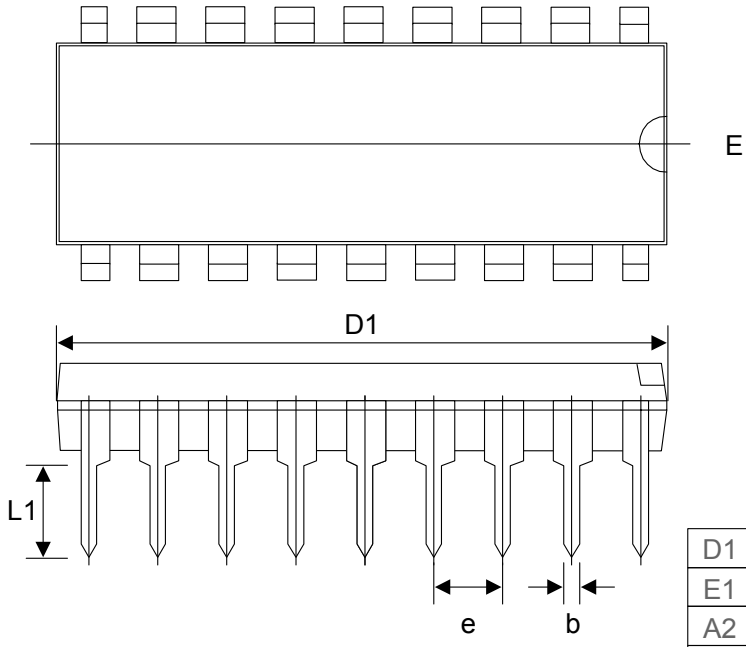
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
750	250	130	115	18	10	100

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-16-300

7.1.2. PDIP 18



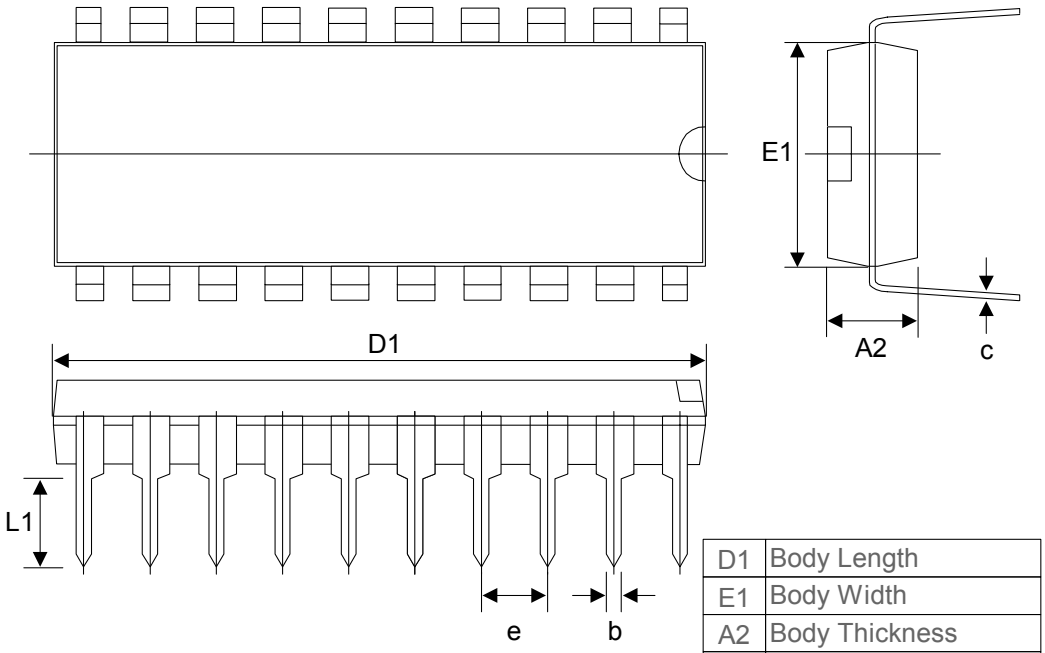
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
900	250	130	115	18	10	100

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-18-300

7.1.3. PDIP 20



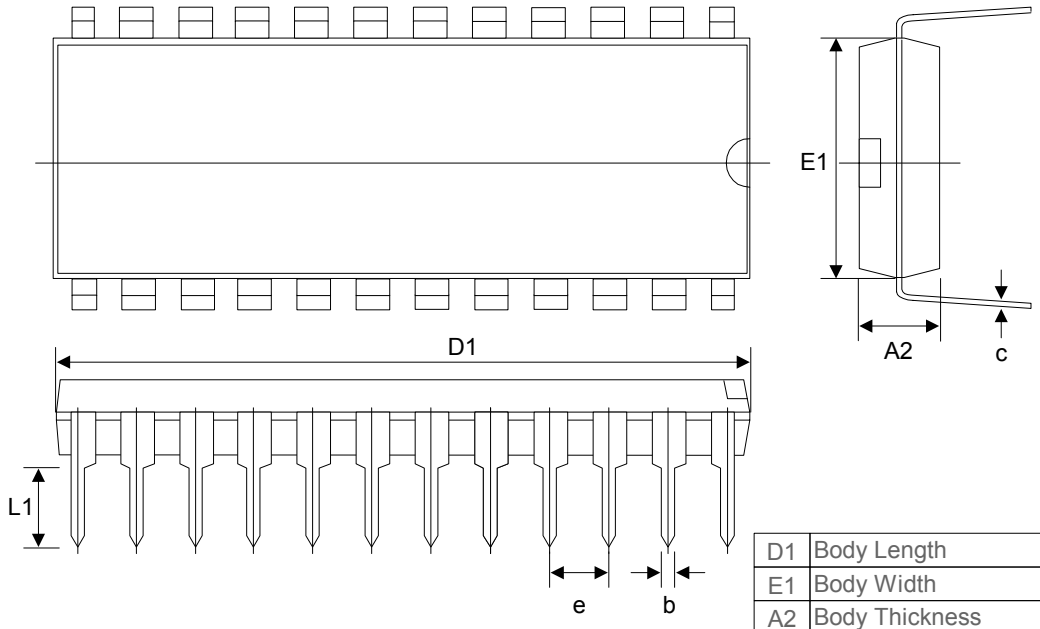
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
1020	250	130	115	18	10	100

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-20-300

7.1.4. PDIP 24



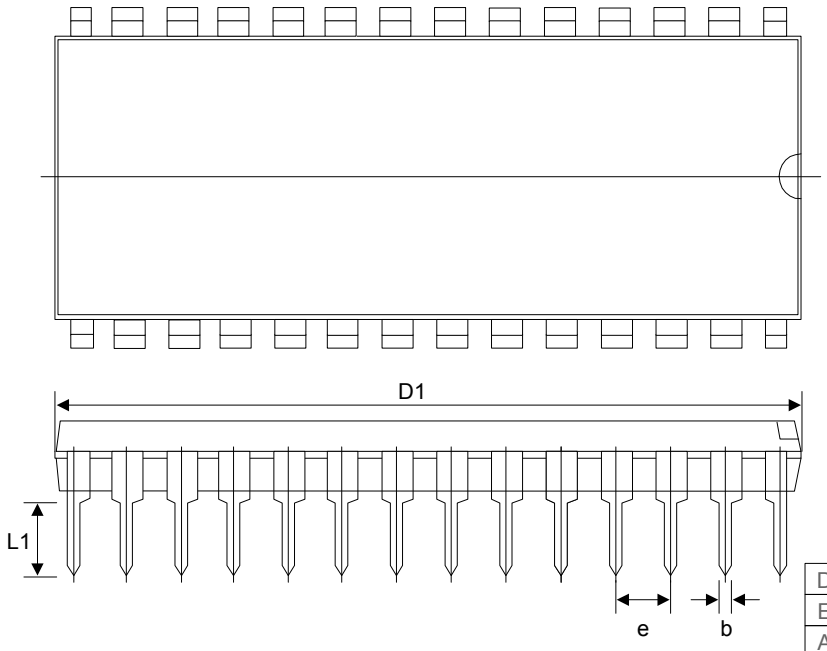
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
1245	250	130	115	18	10	100

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-24-300

7.1.5. PDIP 28 (300mil)



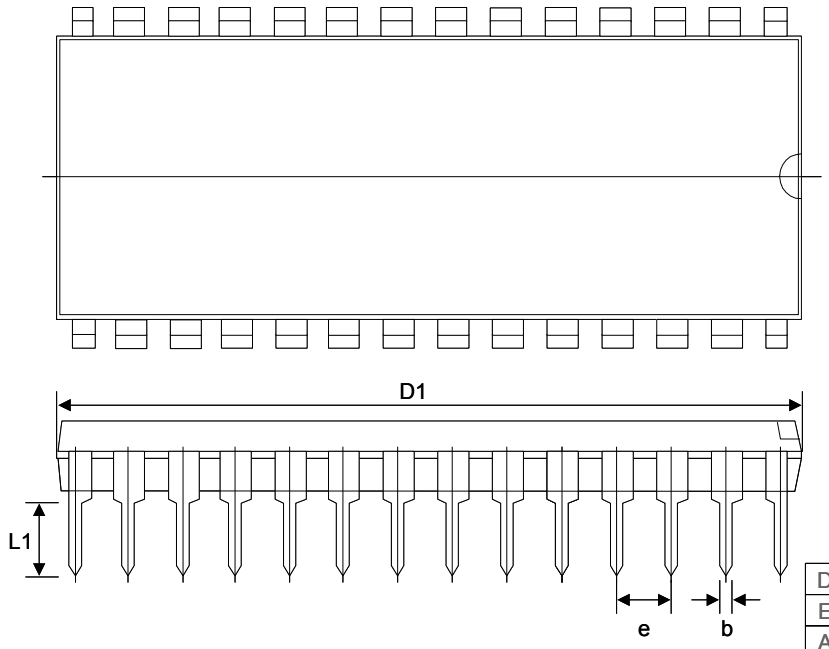
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
1388	290	130	115	18	10	100

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-28-300

7.1.6. PDIP 28 (600mil)



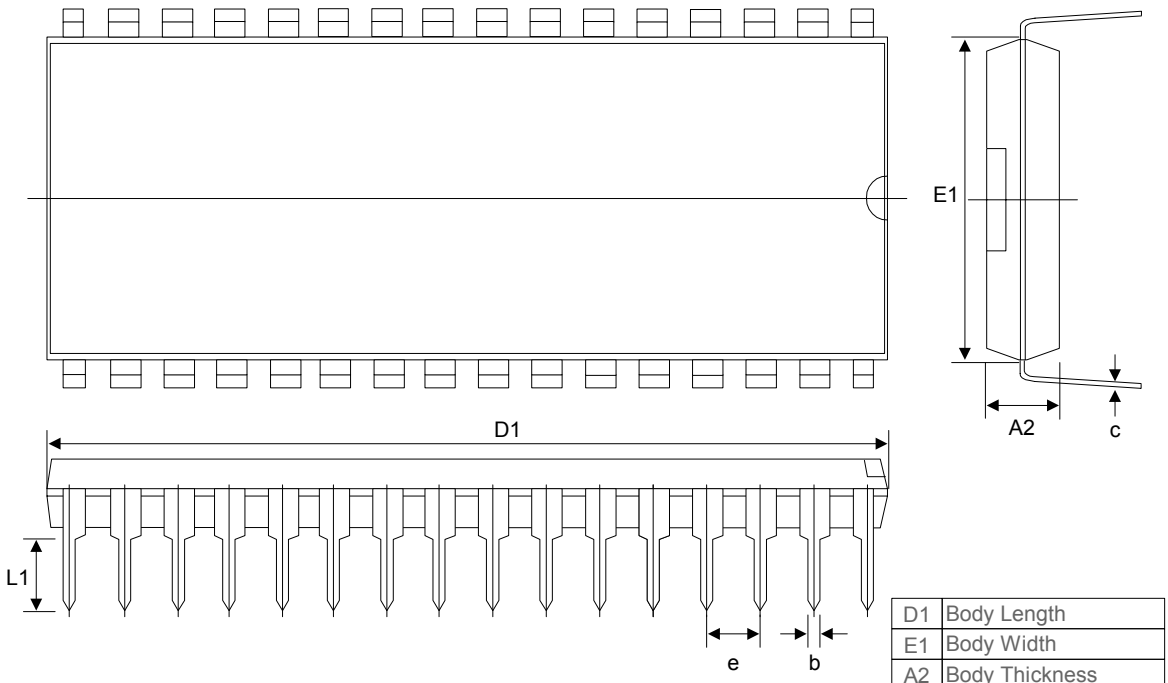
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
1450	550	150	100	18	10	100

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-28-600

7.1.7. PDIP 32 (600mil)



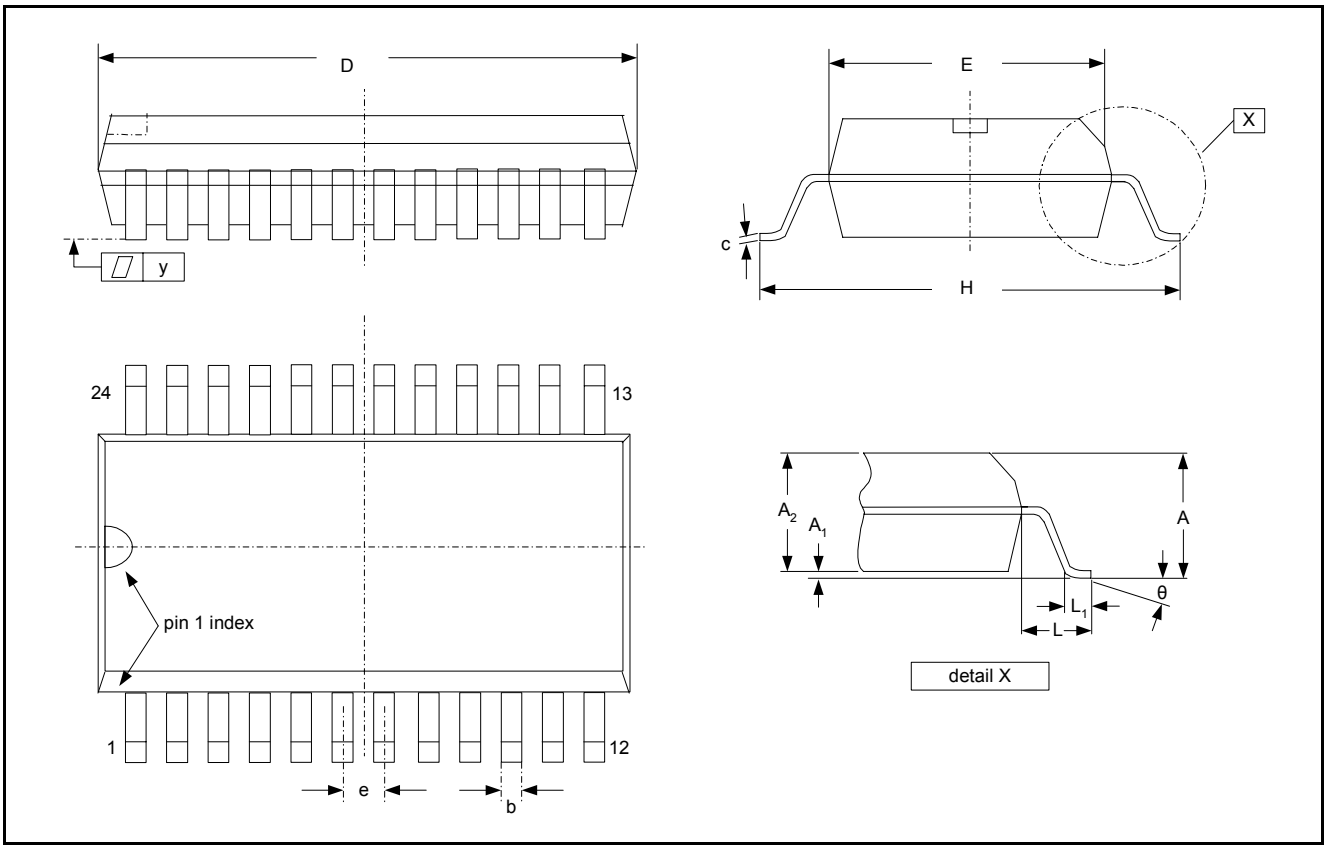
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
1650	550	150	100	18	10	100

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

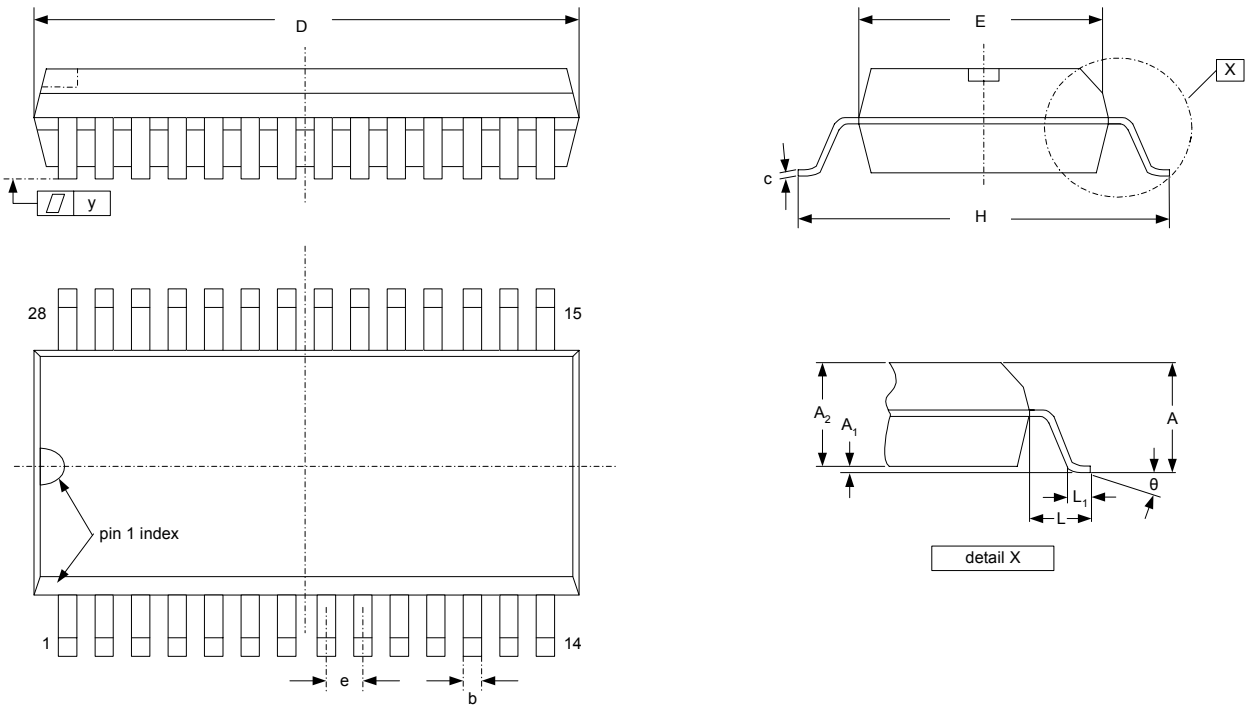
PDIP-32-600

7.1.8. SOP 24 (300mil)



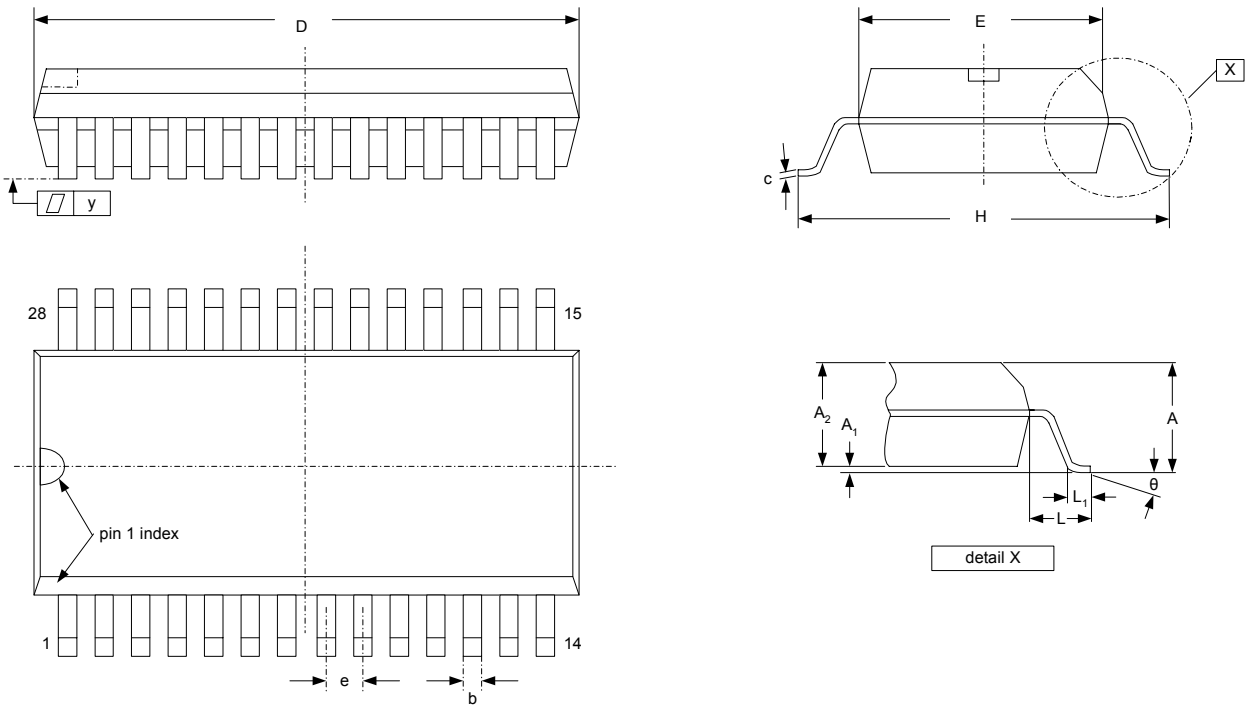
Symbol	Dimension in mm			Dimension in inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.362	2.515	2.642	0.093	0.099	0.104
A_1	0.102	-	0.305	0.004	-	0.012
A_2						
b	-	0.406	-	-	0.016	-
c	-	0.254	-	-	0.010	-
D	15.215	15.240	15.596	0.599	0.600	0.614
E	7.391	7.493	7.595	0.291	0.295	0.299
e	-	1.270	-	-	0.050	-
H	10.008	10.312	10.643	0.394	0.406	0.419
L						
L_1	0.406	0.889	1.270	0.016	0.035	0.050
y	-	-	0.102	-	-	0.004
θ	0^0	-	8^0	0^0	-	8^0

7.1.9. SOP 28 (300mil)



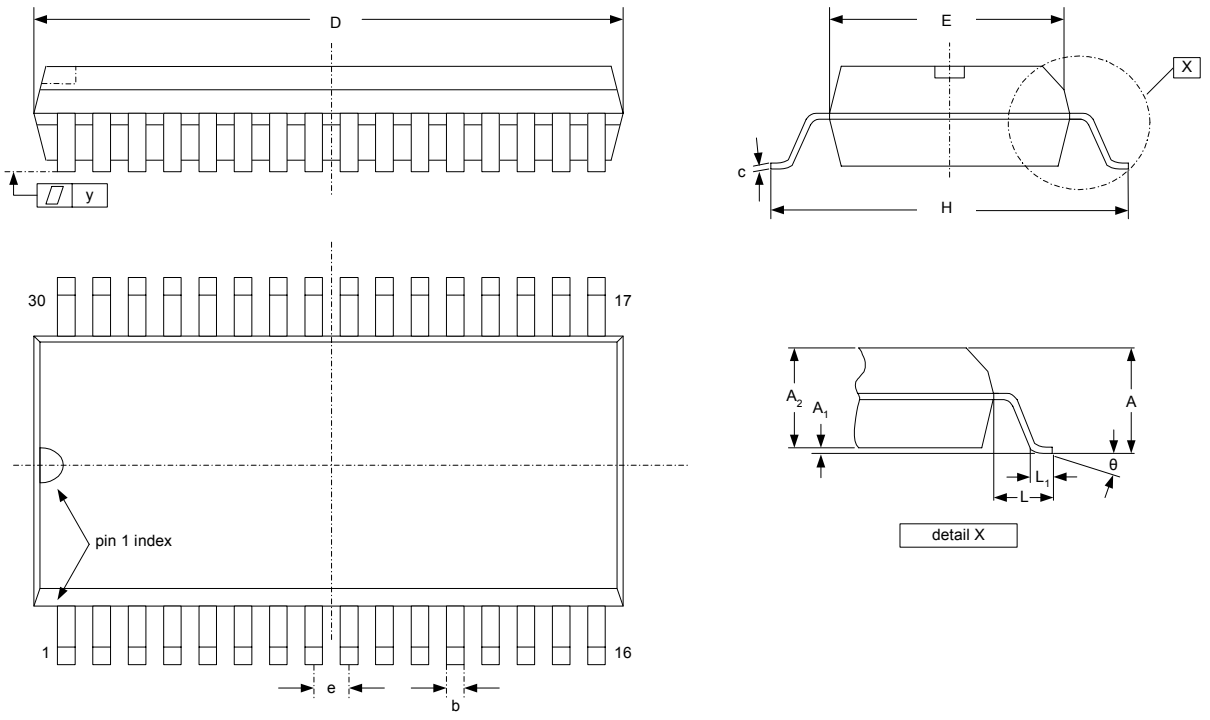
Symbol	Dimension in mm			Dimension in inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.362	-	2.642	0.093	-	0.104
A_1	0.102	-	0.305	0.004	-	0.012
A_2						
b	-	0.406	-	-	0.016	-
c	-	0.254	-	-	0.010	-
D	17.704	-	18.110	0.697	-	0.713
E	7.391	-	7.595	0.291	-	0.299
e	-	1.270	-	-	0.050	-
H	10.008	-	10.643	0.394	-	0.419
L						
L_1	0.406	-	1.270	0.016	-	0.050
y	-	-	0.102	-	-	0.004
θ	0^0		8^0	0^0		8^0

7.1.10. SOP 28 (330mil)



Symbol	Dimension in mm			Dimension in inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	2.845	-	-	0.112
A_1	0.102	-	-	0.004	-	-
A_2	2.362	2.489	2.616	0.093	0.098	0.103
b	0.355	0.406	0.508	0.014	0.016	0.020
c	0.203	0.254	0.356	0.008	0.010	0.014
D	-	18.110	18.618	-	0.713	0.733
E	8.280	8.407	8.534	0.326	0.331	0.336
e	1.118	1.270	1.422	0.044	0.050	0.056
H	11.506	11.811	12.116	0.453	0.465	0.477
L	1.499	0.914	1.905	0.028	0.036	0.044
L_1	0.711	1.702	1.117	0.059	0.067	0.075
y	-	-	0.102	-	-	0.004
θ	0^0	-	10^0	0^0	-	10^0

7.1.11. SOP 32 (445mil)



Symbol	Dimension in mm			Dimension in inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	2.997	-	-	0.116
A_1	0.102	-	-	0.004	-	-
A_2	2.565	2.692	2.819	0.101	0.106	0.111
b	0.356	0.406	0.508	0.014	0.016	0.020
c	0.152	0.203	0.305	0.006	0.008	0.012
D	20.142	20.447	20.752	0.793	0.805	0.817
E	11.176	11.303	11.430	0.440	0.445	0.450
e	1.118	1.270	1.422	0.044	0.050	0.056
H	13.868	14.122	14.376	0.546	0.556	0.566
L	0.584	0.787	0.991	0.023	0.031	0.039
L_1	1.194	1.397	1.600	0.047	0.055	0.063
y	-	-	0.102	-	-	0.004
θ	0^0	-	10^0	0^0	-	10^0

7.2. Ordering Information

Product Number	Package Type
SPMC802B-C	Chip form
SPMC802B-PD03	Package form - PDIP 16
SPMC802B-PD04	Package form - PDIP 18
SPMC802B-PD05	Package form - PDIP 20
SPMC802B-PD06	Package form - PDIP 24
SPMC802B-PD08	Package form - PDIP 28 (300mil)
SPMC802B-PD09	Package form - PDIP 28 (600mil)
SPMC802B-PD11	Package form - PDIP 32 (600mil)
SPMC802B-PS04	Package form - SOP 24 (300mil)
SPMC802B-PS05	Package form - SOP 28 (300mil)
SPMC802B-PS06	Package form - SOP 28 (330mil)
SPMC802B-PS08	Package form - SOP 32 (445mil)

8. DISCLAIMER

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9. REVISION HISTORY

Date	Revision #	Description	Page
AUG. 07, 2002	1.0	Original	27