SQ930C High-Speed USB 2.0

Video Camera Controller

Brief Specification

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REVISION HISTORY

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1.1	Sep 17th , 2004	Revise 1.2 Features due to a software enhancement of JPEG decoding capability: 20 fps ➔ 30fps at VGA format	P. 4
1.2	Nov 17th , 2004	Revise Table 2-10 8032 CPU Interface Pins (LQFP 128): description of port CPU_P3.0	P. 16
1.3	April 22nd , 2005	1. Update 1.1 General Description 2. Correct Figure 4-1 LFBGA 64-pin Package: bottom view – dimension 7.2 ➔ 5.6 (mm) 3. Correct Figure 4-2 LQFP 80-pin Package Diagram	P. 4 P. 18 P. 19

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1. INTRODUCTION

1.1 General Description

The SQ930C High-Speed USB 2.0 Video Camera Controller is a highly integrated and cost-effective solution designed for USB 2.0 PC Camera based applications. It can interface to major brands of CMOS sensors with VGA / 1.3M pixels.

The SQ930C is designed for USB 2.0, the mainstream specification of personal computers. Without the restrictions of USB 1.1 PC camera on USB band width, the SQ930C controller fully expresses the advantage of USB 2.0 on band width (about 40X times faster than USB 1.1). It is also fully compliant with USB 1.1 specification. The SQ930C utilizes lossless compression to achieve the best image quality. With an embedded high-efficient JPEG encoder engine; the transmission rate can achieve 30 frames per second at VGA raw data mode. Based on SQ years of experiences in image processing technology, the SQ930C will be the best solution for PC camera manufacturers.

1.2 Features

Hardware

- Fully compliant with high-speed USB 2.0 specification and 1.1 specification
- Supports varieties of CMOS sensor
- Movie mode (@ 60MHz)
  - JPEG 30fps @ VGA (USB1.1/2.0)
  - Raw data 30fps @ VGA (USB 2.0)
- Built-in JPEG encoder
- Embedded SRAM for image buffer to save overall system cost
- Supports global/color gain control
- Supports Operation Bias(OB)
- 8032 CPU
  - Compatible with industry standard 803x/805x
  - Standard 8051 instruction set
  - Control signals for standard 803x/805x I/O ports
  - 4 clocks/instruction cycle
- Embedded 256 bytes SRAM for CPU
- Embedded 32K bytes ROM for CPU
- One button shot (still image capture)
- Supports external EEPROM for PID/VID
- Uses USB bus power
- Operation clock: USB PIE & CPU at 30Mhz, others at 60Mhz

- Operation voltage: 3.3V IO 2.5 Core logic

Firmware

- Supports Auto Exposure (AE)
- Supports Auto White Balance (AWB)
- Supports Auto Gain Control (AGC)

Software

- Supports still image capture
- TWAIN/WDM software driver
- Compatible with Windows98SE/2000/ME/XP

CMOS Sensors Supported

- CMOS sensor

  1.3M: Micron MI1300

  Omnivision OV9630

  VGA: ICMedia ICM-105C

  Hynix HV7131E, HV7131R

  Micron MI0360

  Omnivision OV7660

2. SYSTEM OVERVIEW

The SQ930C contains an image processor, a JPEG encoder, a PIE, a SRAM controller, and a SRAM buffer for video use. Figure 2-1 shows the internal block diagram.

2.1 Block Diagram

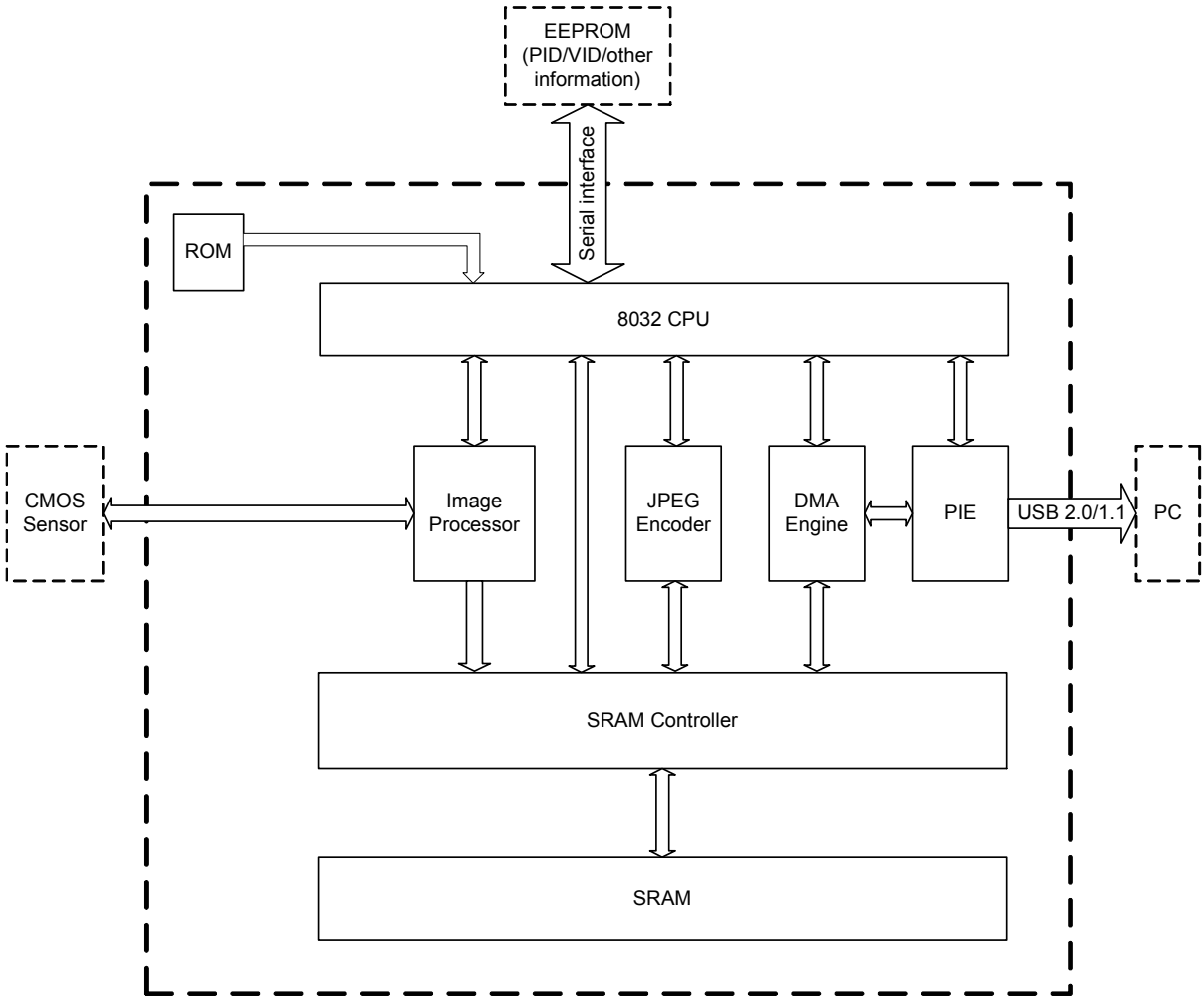


FIGURE 2–1: SQ930C INTERNAL BLOCK DIAGRAM

2.2 LFBGA 64-pin

2.2.1 LFBGA 64 Pin Assignment

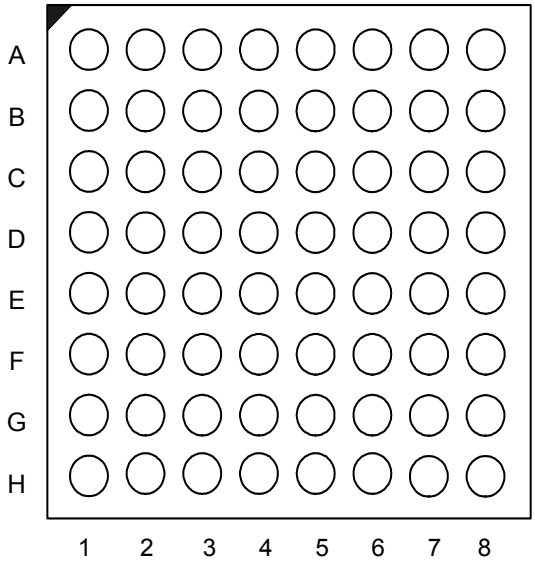


FIGURE 2–2: LFBGA 64 PIN ASSIGNMENT DIAGRAM

2.2.2 LFBGA 64 Pin List

TABLE 2–1: PIN LIST (LFBGA 64)

PIN NO	NAME	PIN NO	NAME
C3	AGND2	**H8**	CPU_ALE
B1	RPU	**G7**	SEN_DATA0
C1	DMRS	**G8**	SEN_DATA1
C2	DPRS	**F6**	SEN_DATA2
D2	AVCC2	**F7**	SEN_DATA3
C4	AGND3	**F8**	SEN_DATA4
D3	AVCC3	**E6**	SEN_DATA5
C5	VCCIO	**E7**	SEN_DATA6
D5	GND	**E8**	SEN_DATA7
E3	CPU_P2.6	**D7**	SUSPEND
E1	CPU_P2.5	**D8**	N.C
F1	CPU_P2.4	**F4**	ZREGO2.5
E2	CPU_P2.3	**D4**	ZREGO3.3
F2	CPU_P2.2	**C8**	SEN_CLK_OUT
G1	CPU_P2.1	**C7**	SEN_HCLK
H1	CPU_P2.0	**B8**	SEN_HSYNC
H2	CPU_PSEN	**A8**	SEN_VSYNC
G2	CPU_P1.3	**A7**	SEN_DATA9
F3	CPU_P1.2	**B7**	SEN_DATA8
H3	CPU_P1.1	**A6**	NRES
G3	CPU_P1.0	**A5**	USB_POWER
B5	VCCK	**E5**	GND
D6	GND	**D1**	CPU_P3.1
C6	VCCIO	**B6**	VCCK
H4	CPU_P0.7	**E4**	GND
G4	CPU_P0.6	**A4**	XOSCI
G5	CPU_P0.5	**A3**	XOSCO
H5	CPU_P0.4	**B3**	AVCC1
F5	CPU_P0.3	**B4**	AGND1
G6	CPU_P0.2	**A2**	RREF
H6	CPU_P0.1	**B2**	DM
H7	CPU_P0.0	**A1**	DP

2.2.3 LFBGA 64 Pin Descriptions

TABLE 2–2: POWER SUPPLY PINS (LFBGA 64)

PIN NO	NAME	I/O	DESCRIPTION
C3	AGND2	PWR	Analog ground
D2	AVCC2	PWR	Power, Analog AVCC=3.3
C4	AGND3	PWR	Analog ground
D3	AVCC3	PWR	Power, Analog AVCC=3.3
C5	VCCIO	PWR	Power, Digital VCC=3.3
D5	GND	PWR	Digital ground
B5	VCCK	PWR	Power, Digital VCCK=2.5
D6	GND	PWR	Digital ground
C6	VCCIO	PWR	Power, Digital VCC=3.3
D4	ZREGO3.3	PWR	Power, Digital VCC=3.3
F4	ZREGO2.5	PWR	Power, Digital VCCK=2.5
E5	GND	PWR	Digital ground
B6	VCCK	PWR	Power, Digital VCCK=2.5
E4	GND	PWR	Digital ground
B3	AVCC1	PWR	Analog AVCC=3.3
B4	AGND1	PWR	Analog ground

TABLE 2–3: SYSTEM PINS (LFBGA 64)

PIN NO	NAME	I/O	DESCRIPTION
A6	NRES	I	Digital input Pull high to force ASIC normal action, low will into reset state.
A4	XOSCI	I	12M Crystal in
A3	XOSCO	O	12M Crystal out

TABLE 2–4: 8032 CPU INTERFACE PINS (LFBGA 64)

PIN NO	NAME	I/O	DESCRIPTION
D1	CPU_P3.1	I/O	Port 3.1 bi-directional I/O port
E3, E1, F1, E2, F2, G1, H1	CPU_P2.6~ CPU_P2.0	O	Microprocessor High Address Bus
H2	CPU_PSEN	O	Program Store Enable is the read strobe to external program memory.
G2, F3, H3, G3	CPU_P1.3~ CPU_P1.0	I/O	Port 1.3~ Port 1.0 is an 4-bit bi-directional I/O port
H4, G4, G5, H5, F5, G6, H6, H7	CPU_P0.7~ CPU_P0.0	I/O	Microprocessor Data / Low Address Bus
H8	CPU_ALE	O	Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.

TABLE 2–5: USB INTERFACE PINS (LFBGA 64)

PIN NO	NAME	I/O	DESCRIPTION
B1	RPU	I	Connect external resistor (1.5kΩ ± 0.1%) to AVCC (Analog power 3.3V)
C1	DMRS	I/O	USB1.1 data in Data negative pin terminal, connect to external resistor (39Ω ± 0.1%)
C2	DPRS	I/O	USB1.1 data in Data positive pin terminal, connect to external resistor (39Ω ± 0.1%)
D7	SUSPEND	O	Device entry normal mode when drive 'L' Device entry suspend mode when high impedance
A5	USB_POWER	I	Connect to the USBVCC pin of USB Connector
A2	RREF	I	Connect external reference resistor (12.1kΩ ±0.1%) to Analog ground
B2	DM	I/O	USB2.0 data pin Data negative pin terminal
A1	DP	I/O	USB2.0 data pin Data positive pin terminal

TABLE 2–6: CMOS SENSOR INTERFACE PINS (LFBGA 64)

PIN NO	NAME	I/O	DESCRIPTION
C8	SEN_CLK_OUT	O	CMOS Sensor Clock Output
C7	SEN_HCLK	I	CMOS Sensor Master Clock
B8	SEN_HSYNC	I	CMOS Sensor Vertical Synchronization Signal
A8	SEN_VSYNC	I	CMOS Sensor Horizontal Synchronization Signal
A7, B7, E8, E7, E6, F8, F7, F6, G8, G7	SEN_DATA[9:0]	I	Sensor Image Data [9:0]

TABLE 2–7: CONFIGURATION PINS (LFBGA 64)

PIN NO	NAME	I/O	DESCRIPTION
E3	IM6	I	Connect external resistor 10kΩ to VCCIO (3.3V)
E1	IM5	I	Connect external resistor 10kΩ to GND
F1	IM4	I	Connect external resistor 10kΩ to GND
E2	IM3	I	Connect external resistor 10kΩ to VCCIO (3.3V)
F2	IM2	I	Connect external resistor 10kΩ to VCCIO (3.3V)
G1	IM1	I	Connect external resistor 10kΩ to VCCIO (3.3V)
H1	IM0	I	Connect external resistor 10kΩ to VCCIO (3.3V)
H8	IM9	I	Connect external resistor 10kΩ to VCCIO (3.3V)
F5	IM16	I	Connect external resistor 10kΩ to GND
H5	IM17	I	Connect external resistor 10kΩ to GND
G5	IM18	I	Connect external resistor 10kΩ to GND

Note: These configuration pins determine the SQ930C function modes. These modes are defined when ASIC entries normal operation from reset state.

2.3 LQFP 80-pin

2.3.1 LQFP 80 Pin Assignment

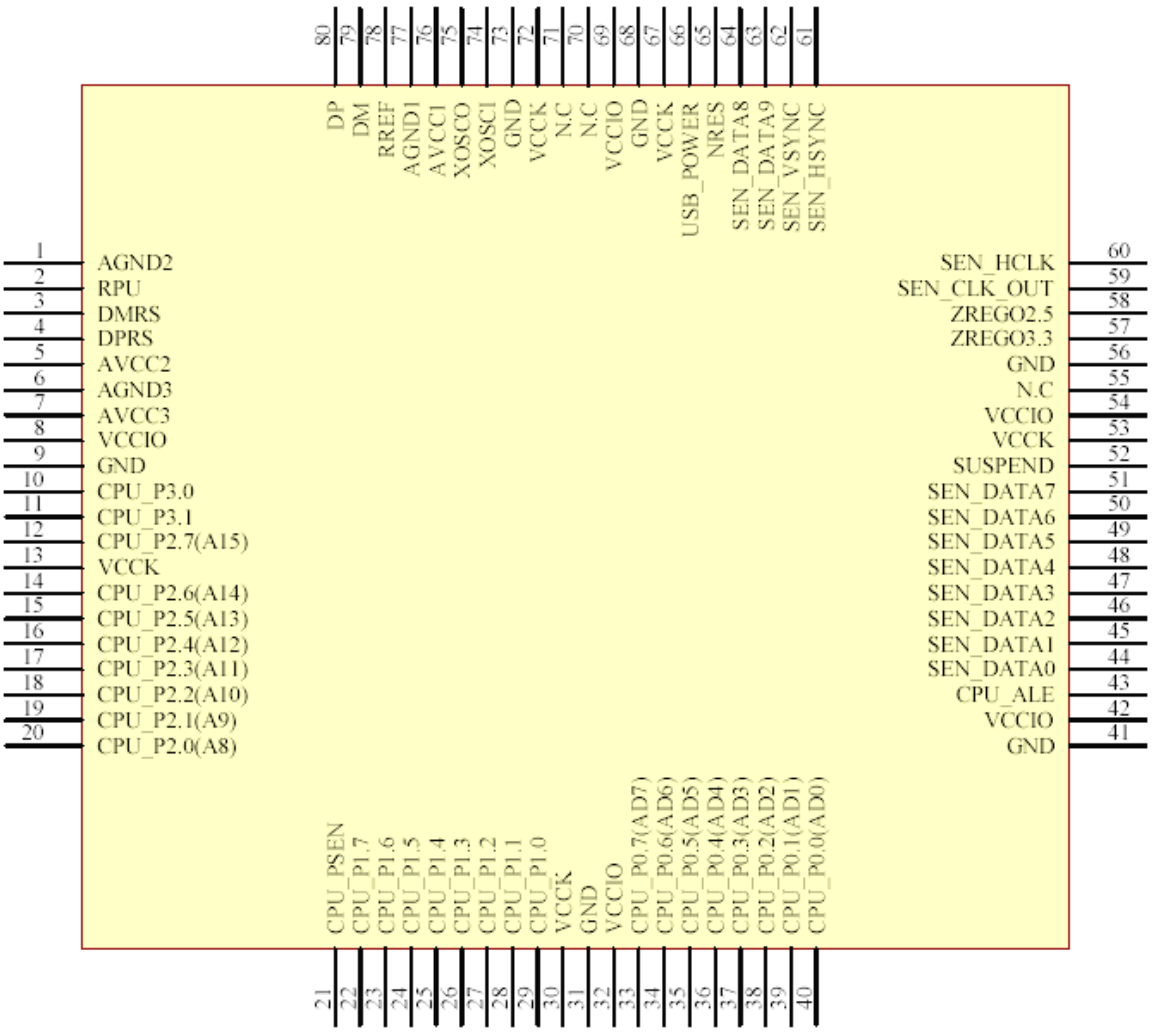


FIGURE 2–3: LQFP 80 PIN ASSIGNMENT DIAGRAM

2.3.2 LQFP 80 Pin List

TABLE 2–7: PIN LIST (LQFP 80)

PIN NO	NAME	PIN NO	NAME
1	AGND2	36	CPU_P0.4
2	RPU	37	CPU_P0.3
3	DMRS	38	CPU_P0.2
4	DPRS	39	CPU_P0.1
5	AVCC2	40	CPU_P0.0
6	AGND3	41	GND
7	AVCC3	42	VCCIO
8	VCCIO	43	CPU_ALE
9	GND	44	SEN_DATA0
10	CPU_P3.0	45	SEN_DATA1
11	CPU_P3.1	46	SEN_DATA2
12	CPU_P2.7	47	SEN_DATA3
13	VCCK	48	SEN_DATA4
14	CPU_P2.6	49	SEN_DATA5
15	CPU_P2.5	50	SEN_DATA6
16	CPU_P2.4	51	SEN_DATA7
17	CPU_P2.3	52	SUSPEND
18	CPU_P2.2	53	VCCK
19	CPU_P2.1	54	VCCIO
20	CPU_P2.0	55	N.C
21	CPU_PSEN	56	GND
22	CPU_P1.7	57	ZREGO3.3
23	CPU_P1.6	58	ZREGO2.5
24	CPU_P1.5	59	SEN_CLK_OUT
25	CPU_P1.4	60	SEN_HCLK
26	CPU_P1.3	61	SEN_HSYNC
27	CPU_P1.2	62	SEN_VSYNC
28	CPU_P1.1	63	SEN_DATA9
29	CPU_P1.0	64	SEN_DATA8
30	VCCK	65	NRES
31	GND	66	USB_POWER
32	VCCIO	67	VCCK
33	CPU_P0.7	68	GND
34	CPU_P0.6	69	VCCIO
35	CPU_P0.5	70	N.C

PIN NO	NAME	PIN NO	NAME
71	N.C	**76**	AVCC1
72	VCCK	**77**	AGND1
73	GND	**78**	RREF
74	XOSCI	**79**	DM
75	XOSCO	**80**	DP

2.3.3 LQFP 80 Pin Descriptions

TABLE 2–8: POWER SUPPLY PINS (LQFP 80)

PIN NO	NAME	I/O	DESCRIPTION
1	AGND2	PWR	Analog ground
5	AVCC2	PWR	Power, analog AVCC=3.3
6	AGND3	PWR	Analog ground
7	AVCC3	PWR	Power, analog AVCC=3.3
8	VCCIO	PWR	Power, digital VCC=3.3
9	GND	PWR	Digital ground
13	VCCK	PWR	Power, digital VCCK=2.5
30	VCCK	PWR	Power, digital VCCK=2.5
31	GND	PWR	Digital ground
32	VCCIO	PWR	Power, digital VCC=3.3
41	GND	PWR	Digital ground
42	VCCIO	PWR	Power, digital VCC=3.3
53	VCCK	PWR	Power, digital VCCK=2.5
54	VCCIO	PWR	Power, digital VCC=3.3
56	GND	PWR	Digital ground
57	ZREGO3.3	PWR	Power, digital VCC=3.3
58	ZREGO2.5	PWR	Power, digital VCCK=2.5
67	VCCK	PWR	Power, digital VCCK=2.5
68	GND	PWR	Digital ground
69	VCCIO	PWR	Power, digital VCC=3.3
72	VCCK	PWR	Power, digital VCCK=2.5
73	GND	PWR	Digital ground
76	AVCC1	PWR	Analog AVCC=3.3
77	AGND1	PWR	Analog ground

TABLE 2–9: SYSTEM PINS (LQFP 80)

PIN NO	NAME	I/O	DESCRIPTION
65	NRES	I	System reset, active low
74	XOSCI	I	12M Crystal in
75	XOSCO	O	12M Crystal out

TABLE 2–10: 8032 CPU INTERFACE PINS (LQFP 80)

PIN NO	NAME	I/O	DESCRIPTION
10	CPU_P3.0	O	Port 3 - 0, output port only
11	CPU_P3.1	I/O	Port 3 - 1, bi-directional I/O port
12, 14~20	CPU_P2.7~ CPU_P2.0	O	Microprocessor High Address Bus
21	CPU_PSEN	O	Program Store Enable is the read strobe to external program memory.
22~29	CPU_P1.7~ CPU_P1.0	I/O	Port 1 is an 8-bit bi-directional I/O port.
33~40	CPU_P0.7~ CPU_P0.0	I/O	Microprocessor Data / Low Address Bus
43	CPU_ALE	O	Address Latch Enable Output pulse for latching the low byte of the address during accesses to external memory

TABLE 2–11: USB INTERFACE PINS (LQFP 80)

PIN NO	NAME	I/O	DESCRIPTION
2	RPU	I	Connect external resistor (1.5kΩ ± 0.1%) to AVCC (Analog power 3.3V)
3	DMRS	I/O	USB1.1 data in Data negative pin terminal, connecting to external resistor (39Ω ± 0.1%)
4	DPRS	I/O	USB1.1 data in Data positive pin terminal, connecting to external resistor (39Ω ± 0.1%)
52	SUSPEND	O	Device entry normal mode when drive 'L' Device entry suspend mode when high impedance
66	USB_POWER	I	Connect to the USBVCC pin of USB Connector
78	RREF	I	Connect external reference resistor (12.1kΩ ±0.1%) to Analog ground
79	DM	I/O	USB2.0 data pin Data negative pin terminal
80	DP	I/O	USB2.0 data pin Data positive pin terminal

TABLE 2–12: CMOS SENSOR INTERFACE PINS (LQFP 80)

PIN NO	NAME	I/O	DESCRIPTION
59	SEN_CLK_OUT	O	CMOS Sensor Clock Output
60	SEN_HCLK	I	CMOS Sensor Master Clock
61	SEN_HSYNC	I	CMOS Sensor Vertical Synchronization Signal
62	SEN_VSYNC	I	CMOS Sensor Horizontal Synchronization Signal
63, 64, 51~44	SEN_DATA[9:0]	I	Sensor Image Data [9:0]

TABLE 2–13: CONFIGURATION PINS (LQFP 80)

PIN NO	NAME	I/O	DESCRIPTION
14	IM6	I	Connect external resistor 10kΩ to VCCIO (3.3V)
15	IM5	I	Connect external resistor 10kΩ to VCCIO (3.3V)
16	IM4	I	Connect external resistor 10kΩ to GND
17	IM3	I	Connect external resistor 10kΩ to VCCIO (3.3V)
18	IM2	I	Connect external resistor 10kΩ to VCCIO (3.3V)
19	IM1	I	Connect external resistor 10kΩ to VCCIO (3.3V)
20	IM0	I	Connect external resistor 10kΩ to VCCIO (3.3V)
35	IM18	I	Connect external resistor 10kΩ to GND
36	IM17	I	Connect external resistor 10kΩ to GND
37	IM16	I	Connect external resistor 10kΩ to GND
43	IM9	I	Connect external resistor 10kΩ to VCCIO (3.3V)

NOTE: These configuration pins determine the SQ930C function modes. These modes are defined when ASIC entries normal operation from reset state.

3. ELECTRICAL CHARACTERISTIC

3.1 Operation Conditions

TABLE 3-1: OPERATION CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VCC	Power Supply	3	3.3	3.6	V
VIN3	Input Voltage of 3.3V with 5V Tolerance I/O	0	3.3	5.25	V
TJ	Junction Operating Temperature: Commercial	-40	25	125	℃

3.2 DC Characteristics

TABLE 3-2: DC CHARACTERISTICS OF 3.3V I/O CELLS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VCC	Power Supply	-	3.0	3.3	3.6	V
AVCC	Power Supply	-	3.0	3.3	3.6	V
VCCK	Power Supply	-	2.25	2.5	2.75	V
VIL	Input Low Voltage	LVTTL spec.	-	-	0.8	V
VIH	Input High Voltage	LVTTL spec.	2	-	-	V
NRES-	Schmitt Trigger Negative Going Threshold	-	0.9	1.2	-	V
NRES+	Schmitt Trigger Positive Going Threshold	-	-	2.1	2.5	V
VOL	Output Low Voltage	IOl = 4 mA	-	-	0.4	V
VOH	Output High Voltage	IOH = -4 mA	2.4	-	-	V

4. PACKAGING

4.1 LFBGA 64-pin Package

Body size: 7 x 7 mm

Ball pitch: 0.8 mm

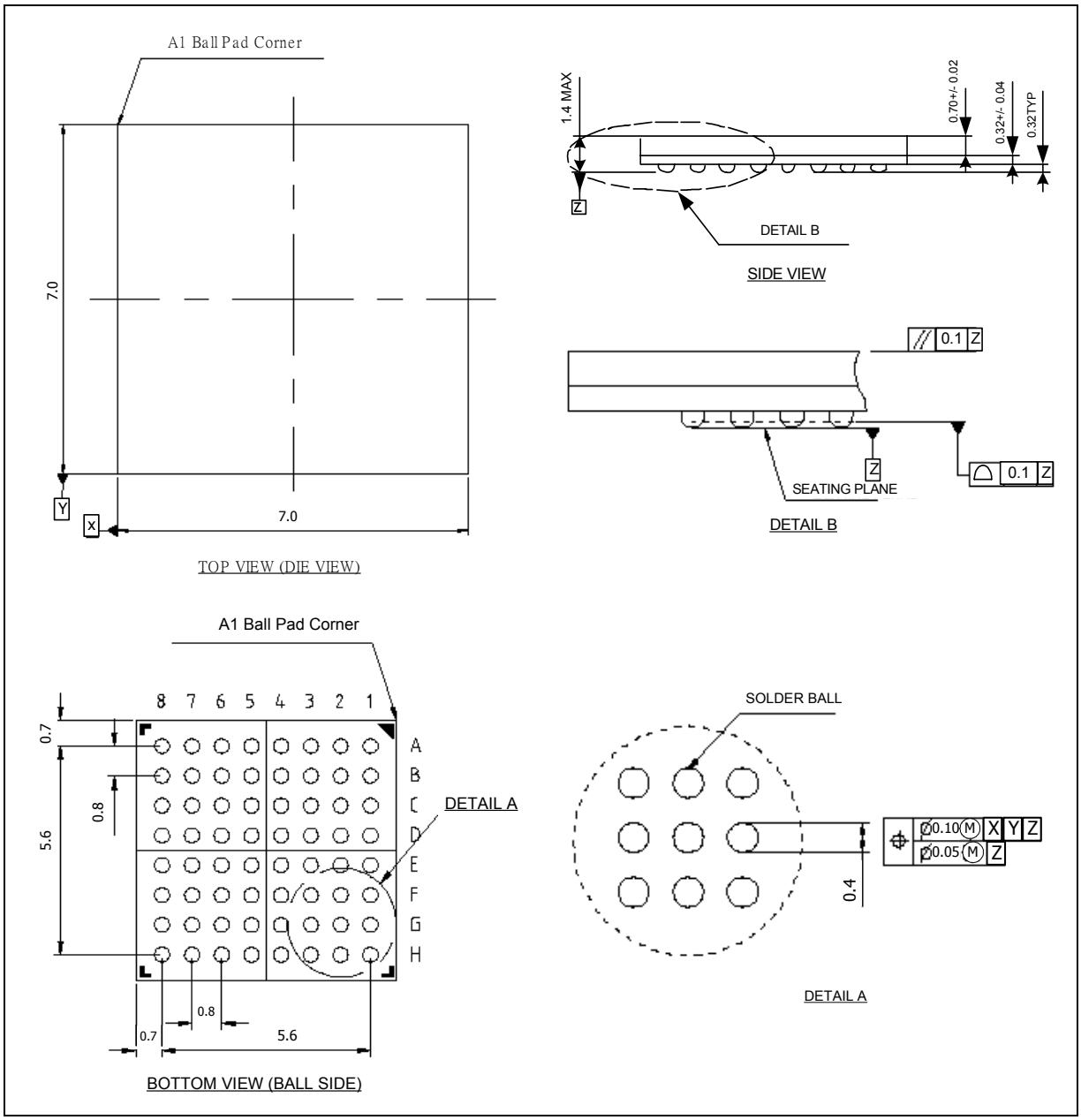
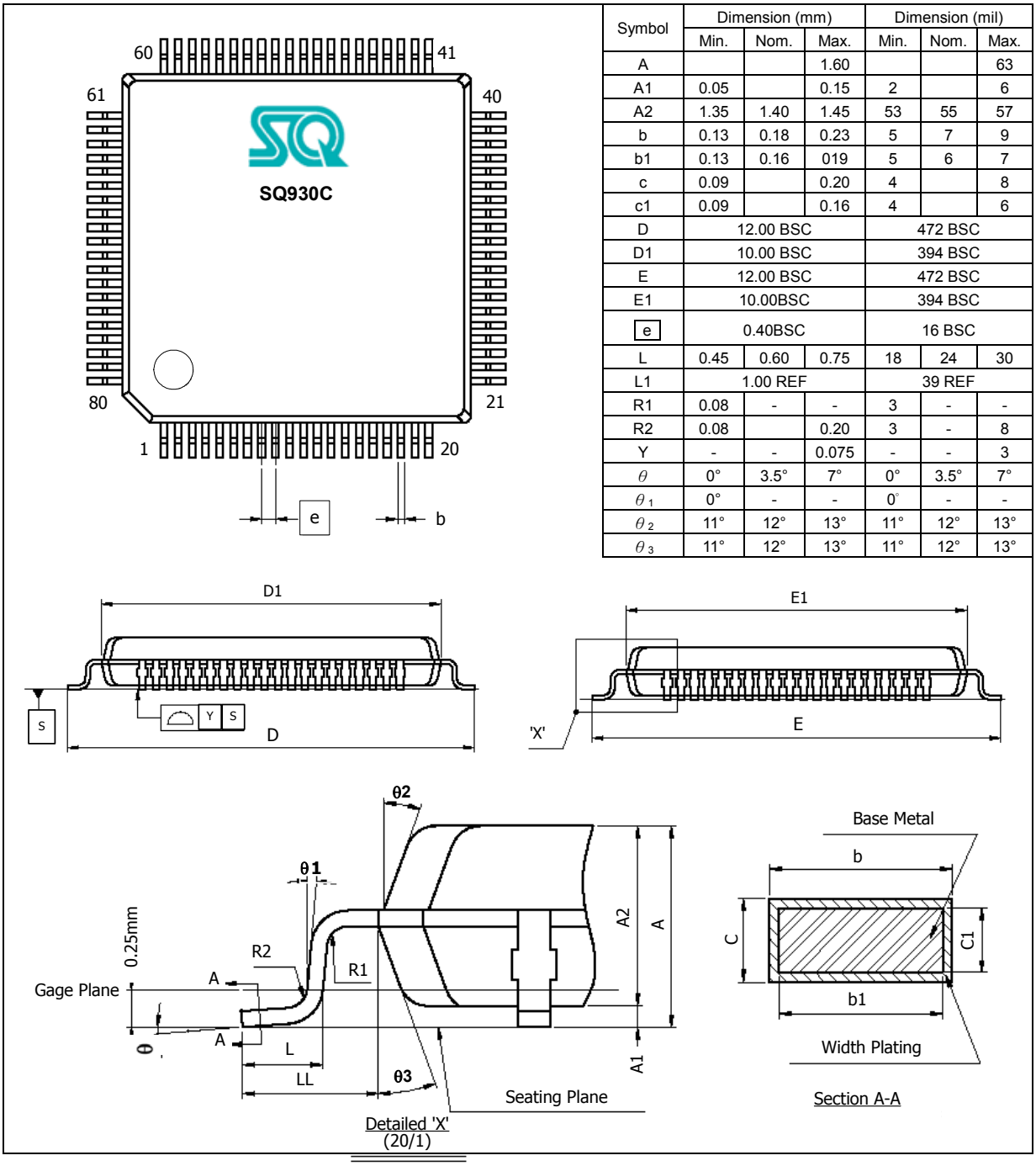


FIGURE 4–1: LFBGA 64-PIN PACKAGE DIAGRAM

4.2 LQFP 80-pin Package

Body size: 10 x 10 x 1.4 mm



Symbol	Dimension (mm)			Dimension (mil)		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	019	5	6	7
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	12.00 BSC			472 BSC		
D1	10.00 BSC			394 BSC		
E	12.00 BSC			472 BSC		
E1	10.00BSC			394 BSC		
e	0.40BSC			16 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08	-	-	3	-	-
R2	0.08		0.20	3	-	8
Y	-	-	0.075	-	-	3
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	-	-	0°	-	-
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°

FIGURE 4–2: LQFP 80-PIN PACKAGE DIAGRAM

1. Dimension D1 and C1 do not include mold protrusion. Allowable protrusion is 0.25mm Per side D1 and C1 are maximum plastic body size dimension including mold mismatch.
2. Dimension b does not include DAMBAR protrusion. Allowable DAMBAR protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm.

4.3 Ordering Information

TABLE 4–1: ORDERING INFORMATION TABLE

TYPE NO	PACKAGE	DESCRIPTION
SQ930C	LFBGA64	Low-profile Fine-pitch Ball Grid Array Package, 64-ball
	LQFP80	Low-profile Quad Flat Package, 80-pin