

FEATURES

“Clickless” Bilateral Audio Switching
Four SPST Switches in a 20-Pin Package
Ultralow THD+N: 0.0008% @ 1 kHz (2 V rms,
 $R_L = 100\text{ k}\Omega$ **)**
Low Charge Injection: 35 pC typ
High OFF Isolation: -100 dB typ ($R_L = 10\text{ k}\Omega$ @ 1 kHz)
Low Crosstalk: -94 dB typ ($R_L = 10\text{ k}\Omega$ @ 1 kHz)
Low ON Resistance: 28 Ω typ
Low Supply Current: 900 μA typ
Single or Dual Supply Operation: +11 V to +24 V or
 $\pm 5.5\text{ V}$ **to $\pm 12\text{ V}$**
Guaranteed Break-Before-Make
TTL and CMOS Compatible Logic Inputs
Low Cost-Per-Switch

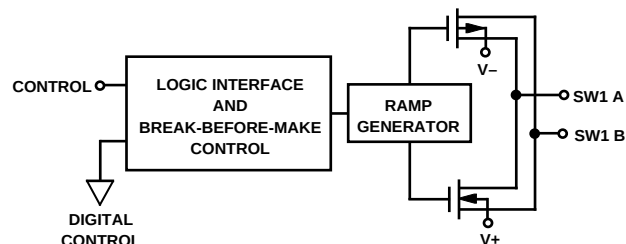
GENERAL DESCRIPTION

The SSM2404 integrates four SPST analog switches in a single 20-pin package. Developed specifically for high performance audio applications, distortion and noise are negligible over the full operating range of 20 Hz to 20 kHz. With very low charge injection of 35 pC, “clickless” audio switching is possible, even under the most demanding conditions.

Switch control is realized by conventional TTL or CMOS logic. Guaranteed “break-before-make” operation assures that all switches in a large system will open before any switch reaches the ON state.

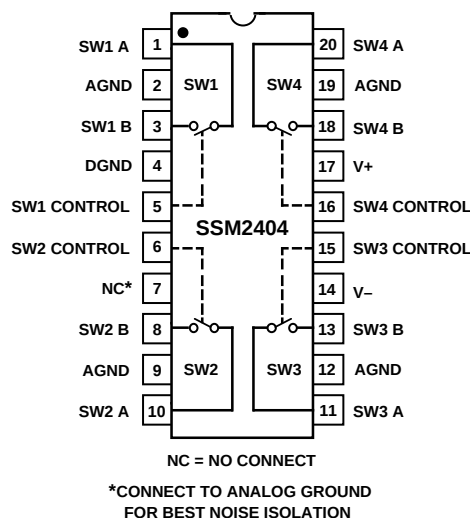
Single or dual supply operation is possible. Additional features include -100 dB OFF isolation, -94 dB crosstalk and 28 Ω ON resistance. Optional current-mode switching permits an extended signal-handling range. Although optimized for large load impedances, the SSM2404 maintains good audio performance even under low load impedance conditions.

BLOCK DIAGRAM OF ONE SWITCH CHANNEL



PIN CONNECTIONS

Epoxy Mini-DIP (P Suffix)
and SOIC (S Suffix)



REV. B

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SSM2404—SPECIFICATIONS

($V_S = \pm 12\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.
Typical specifications apply at $T_A = +25^\circ\text{C}$.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD+N	@ 1 kHz, with 80 kHz Filter, $R_L = 100\text{ k}\Omega$, $V_{IN} = 2\text{ V rms}$		0.0008		%
Spectral Noise Density	e_n	20 Hz to 20 kHz		0.8		nV/ $\sqrt{\text{Hz}}$
Wideband Noise Density	e_n p-p	20 Hz to 20 kHz		0.6		$\mu\text{V p-p}$
ANALOG SIGNAL SECTION						
Analog Voltage Range	V_A	$V_{INH} = 2.4\text{ V}$, $I_A = \pm 2\text{ mA}$		± 12		V
Analog Current Range	I_A	$V_{INH} = 2.4\text{ V}$, $V_A = 0\text{ V}$		± 10		mA
ON Resistance	R_{ON}	$I_A = \pm 10\text{ mA}$, $V_A = \pm 10\text{ V dc}$		28	45	Ω
R_{ON} Matching	R_{ON} Match	$I_A = \pm 10\text{ mA}$, $V_A = 0\text{ V}$		1		%
ON Leakage Current	$I_{S(ON)}$	$V_A = \pm 10\text{ V}$	-20	0.1	+20	nA
OFF Leakage Current	$I_{S(OFF)}$	$V_A = \pm 10\text{ V}$	-20	0.1	+20	nA
Charge Injection	Q			35		pC
ON-State Input Capacitance	C_{ON}	$V_A = 5\text{ V rms}$		31		pF
OFF-State Input Capacitance	C_{OFF}	$V_A = 5\text{ V rms}$		17		pF
OFF Isolation	$I_{SO(OFF)}$	$V_A = 50\text{ mV rms}$, $f = 1\text{ kHz}$, $R_L = 10\text{ k}\Omega$		-100		dB
Channel-to-Channel Crosstalk	C_T	$V_A = 50\text{ mV rms}$, $f = 1\text{ kHz}$, $R_L = 10\text{ k}\Omega$		-94		dB
CONTROL SECTION						
Digital Input High	V_{INH}	DGND = 0 V	2.4		V_S	V
Digital Input Low	V_{INL}	DGND = 0 V	0		0.8	V
Turn-On Time ¹	t_{ON}	See Test Circuit		8	50	ms
Turn-Off Time ²	t_{OFF}	See Test Circuit		5	30	ms
Break-Before-Make Time Delay	$t_{ON}-t_{OFF}$			3	20	ms
Logic Input Current						
Logic HI		$V_{INH} = 2.4\text{ V}$	-1000	1.3	+1000	nA
Logic LO		$V_{INL} = 0.8\text{ V}$	-1000	1.0	+1000	nA
POWER SUPPLY						
Supply Voltage Range	V_S	Single Supply	+11		+24	V
		Dual Supply	± 5.5		± 12	V
Positive Supply Current	I_{SY+}	All Channels On		0.9	5	mA
Negative Supply Current	I_{SY-}	All Channels On	-1.5	-0.6		mA
Ground Current		All Channels On	-2.0	-0.3		mA

NOTES

¹Turn-on time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the final value.

²Turn-off time is measured from the time the logic input reaches the 50% point to the time the output reaches 50% of the initial value.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage

Single Supply +27 V

Dual Supply $\pm 13.5\text{ V}$

Analog Input Voltage (V_A) V_S

Logic Input Voltage ($V_{INL/INH}$) V_S

Maximum Current Through Any Switch 20 mA

Operating Temperature Range -40°C to $+85^\circ\text{C}$

Storage Temperature Range -65°C to $+150^\circ\text{C}$

Junction Temperature (T_J) $+150^\circ\text{C}$

Lead Temperature (Soldering, 60 sec) $+300^\circ\text{C}$

Thermal Resistance¹

20-Pin Plastic DIP (P): $\theta_{JA} = 74$, $\theta_{JC} = 32$ $^\circ\text{C/W}$

20-Pin SOIC (S): $\theta_{JA} = 90$, $\theta_{JC} = 27$ $^\circ\text{C/W}$

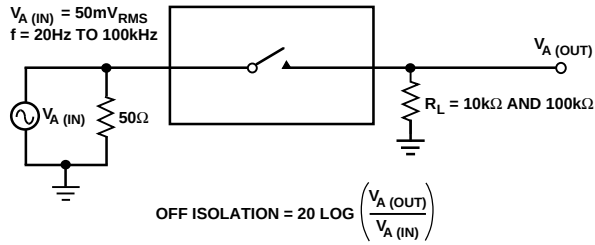
NOTE

¹ θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package.

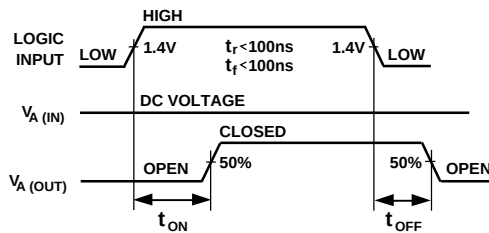
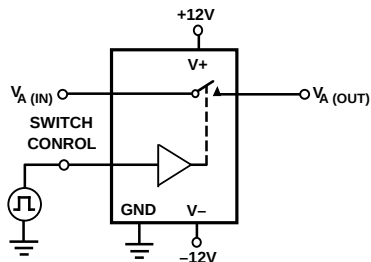
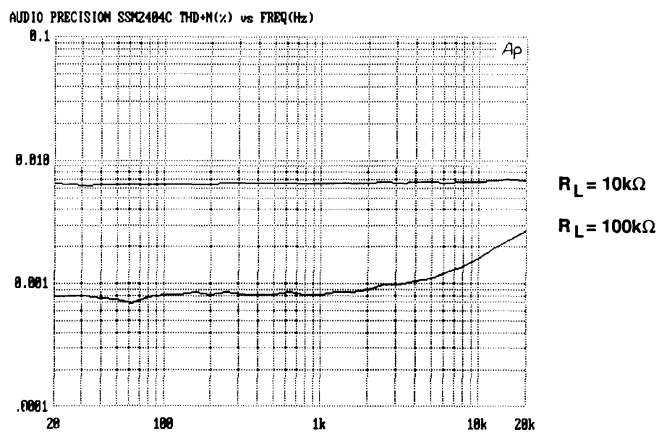
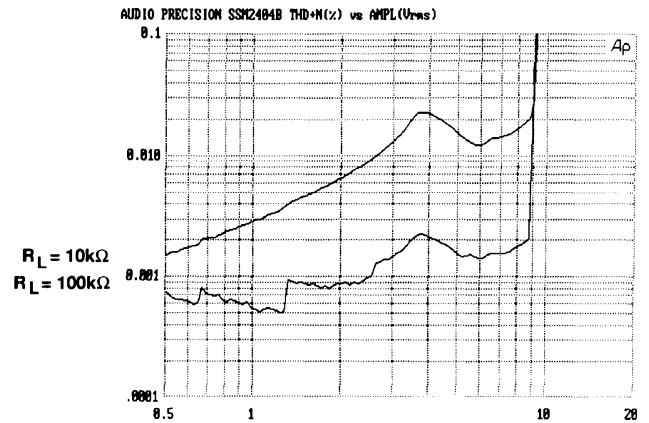
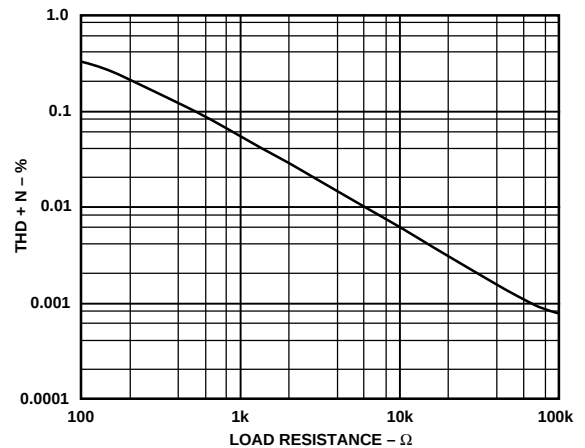
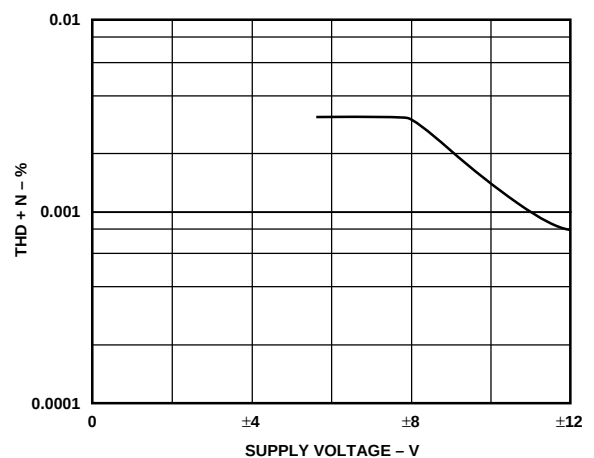
ORDERING GUIDE

Model	Operating Temperature Range	Package	Package Option*
SSM2404P	-40°C to $+85^\circ\text{C}$	20-Pin Plastic DIP	N-20
SSM2404S	-40°C to $+85^\circ\text{C}$	20-Pin SOIC	R-20

*N = Plastic DIP, R = SOIC.



OFF Isolation Test Circuit

 t_{ON}/t_{OFF} Timing DiagramTest Circuit for t_{ON}/t_{OFF} Timing Specification, t_{ON}/t_{OFF} Switching Response, and ON/OFF Transition PhotosFigure 1. THD+N vs. Frequency ($V_S = \pm 12$ V, $V_A = 2$ V rms, with 80 kHz Filter)Figure 2. Headroom ($V_S = \pm 12$ V, $f = 1$ kHz, with 80 kHz Filter)Figure 3. THD+N vs. Load ($V_S = \pm 12$ V, $V_A = 2$ V rms, $f = 1$ kHz, with 80 kHz Filter)Figure 4. THD+N vs. Supply Voltage ($V_A = 2$ V rms, $f = 1$ kHz, $R_L = 100$ kΩ, with 80 kHz Filter)

SSM2404

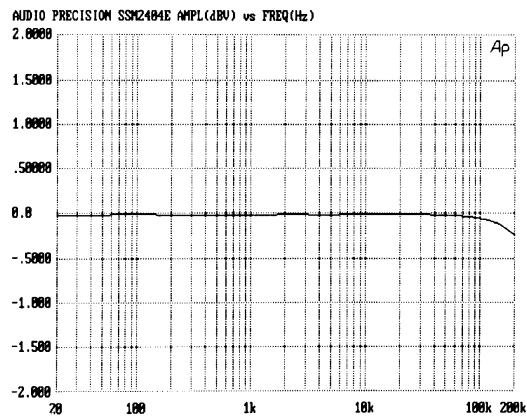


Figure 5. Frequency Response ($V_S = \pm 12\text{ V}$, $V_A = 1\text{ V rms}$, $R_L = 100\text{ k}\Omega$)

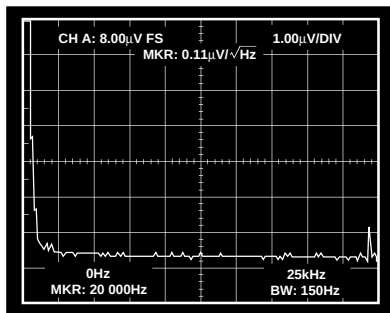


Figure 6. SSM2404 Spectral Noise Density e_n [5 Devices (20 Switches) Chained Together]

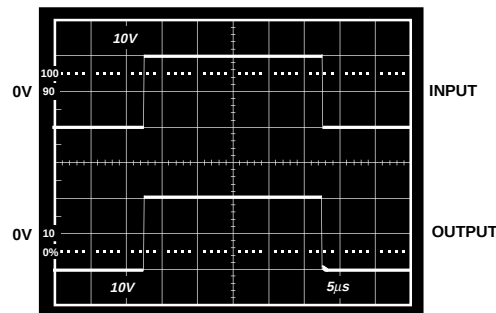


Figure 7. Square Wave Response ($T_A = +25^\circ\text{C}$, $V_S = \pm 12\text{ V}$, $R_L = 100\text{ k}\Omega$, $f = 20\text{ kHz}$)

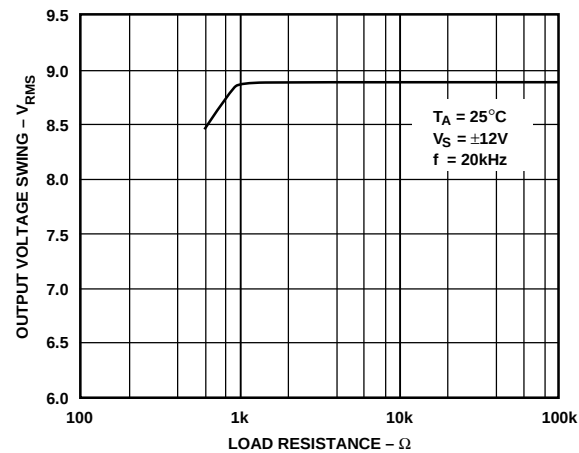


Figure 8. Output Voltage Swing vs. Load Resistance

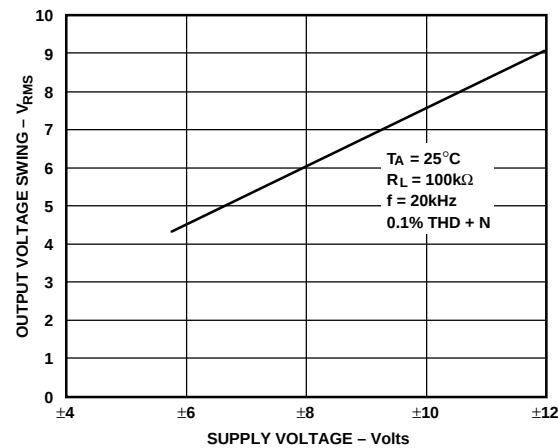


Figure 9. Output Voltage Swing vs. Supply Voltage

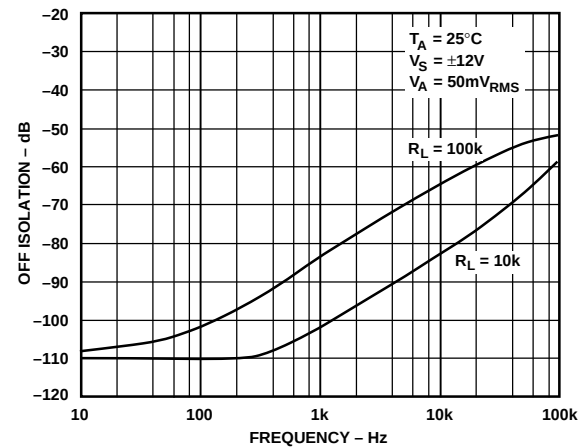


Figure 10. OFF-Isolation vs. Frequency

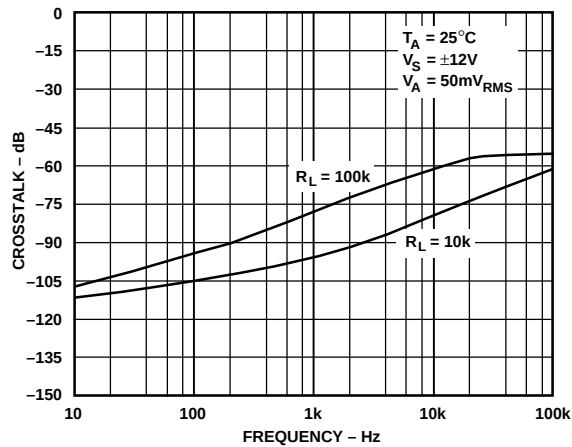


Figure 11. Channel-to-Channel Crosstalk vs. Frequency (Worst Case Conditions, as Measured Between Switches 1 and 4, or 2 and 3)

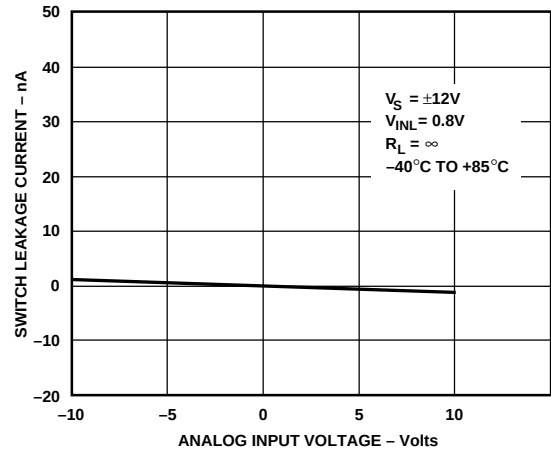


Figure 14. Leakage Current vs. Analog Voltage

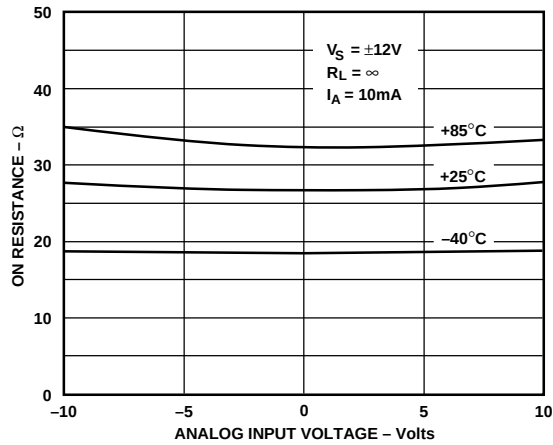


Figure 12. ON Resistance vs. Analog Voltage

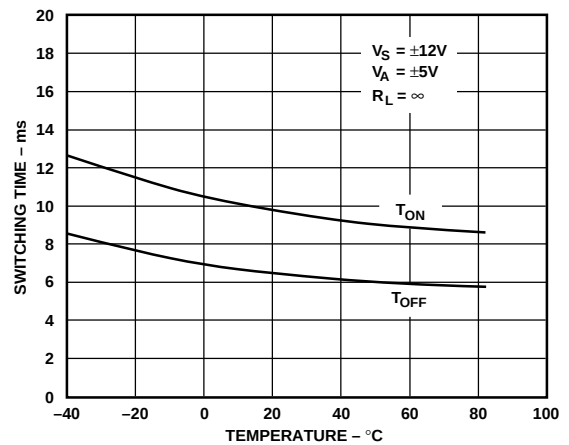


Figure 15. Switching Time vs. Temperature

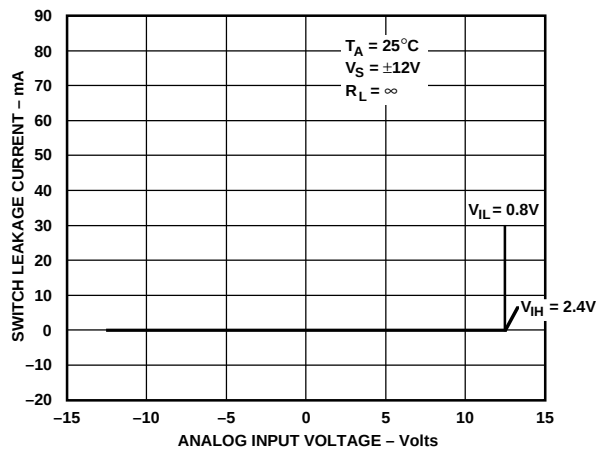


Figure 13. Overvoltage Characteristics

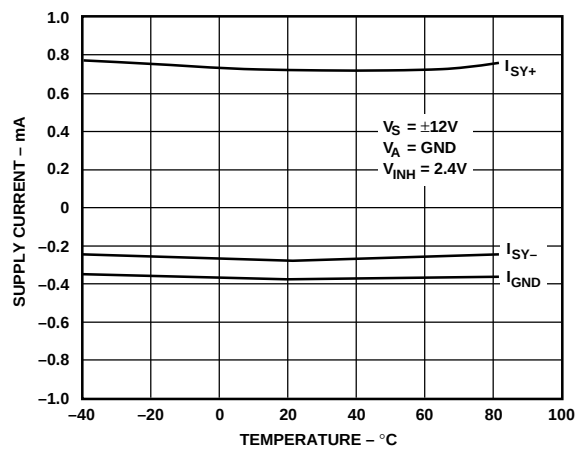


Figure 16. Supply Current vs. Temperature

SSM2404

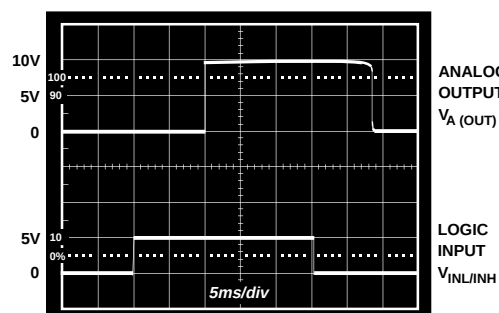


Figure 17. t_{ON}/t_{OFF} Switching Response

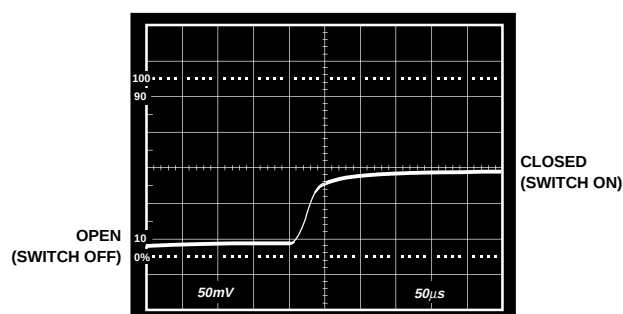


Figure 18. Switch OFF-to-ON Transition ($R_L = 5 \text{ k}\Omega$)

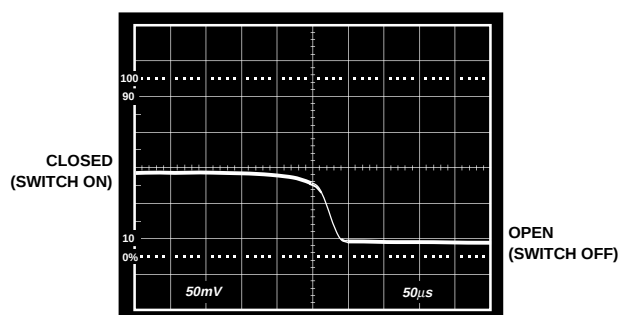


Figure 19. Switch ON-to-OFF Transition ($R_L = 5 \text{ k}\Omega$)

APPLICATIONS INFORMATION

The SSM2404 integrates four analog CMOS switches with guaranteed “break-before-make” operation to provide high quality audio switching. Each switch has complementary N-channel and P-channel MOSFETs to allow the analog input voltage range to include the positive and negative rails and improve linearity. In addition, the topology permits fully bilateral switching. When using the SSM2404 there is full flexibility in configuring the switches. For example, they can be used individually as shown in Figure 20, or as a double-pole, double-throw (DPDT) switch, which is explained later. The

SSM2404 can also be configured as a 4:1 multiplexer, or by using additional packages, as 8:1 or 16:1 and up. The break-before-make feature is guaranteed from part to part allowing such multiple-package applications.

As Figure 20 shows, the SSM2404 is easy to use, and no additional devices are needed. The load resistors are recommended for improved OFF-isolation and charge injection. The ON resistance of the switch is only 28Ω typically, which causes very little signal attenuation even with a load resistor.

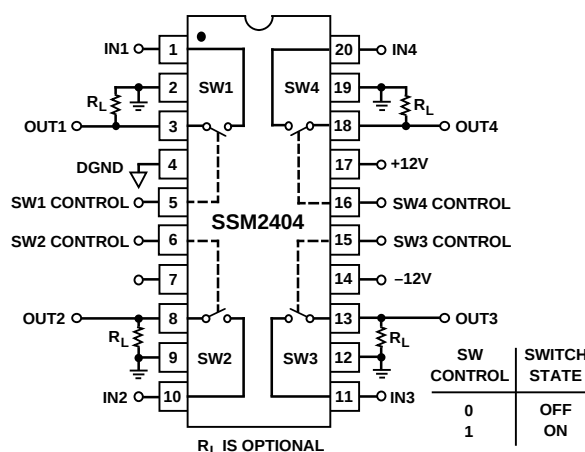


Figure 20. Basic Circuit Configuration

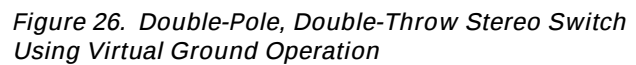
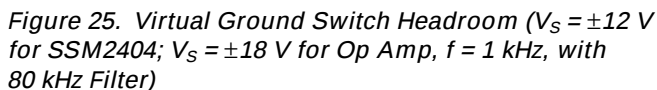
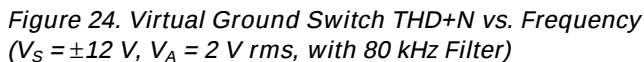
OPTIMIZING PERFORMANCE

As the performance curves show, the switch is optimized for high impedance loads. The distortion performance is at its best when the switch has a load impedance of $100 \text{ k}\Omega$ or greater as shown in Figure 1. However, even at lower values of load resistances, the 1 kHz distortion performance is still excellent, 0.006% for a $10 \text{ k}\Omega$ load. The main trade-off with THD is OFF-isolation and crosstalk. This is shown in Figures 10 and 11, again with two different load conditions. As these graphs show, the $10 \text{ k}\Omega$ load yields approximately a 16 dB improvement in both characteristics.

Thus, the optimum operating point depends on the most critical parameters. When THD is critical then high load impedances should be used; however, when crosstalk and OFF-isolation are critical, lower impedances on the order of $10 \text{ k}\Omega$ should be used. An additional benefit of using the smaller load resistor is that any charge injected onto the output will be shunted to ground through the resistor. If improved OFF-isolation is needed, the SSM2404 dual audio switch should be considered with its excellent 120 dB OFF-isolation at 20 kHz .

It is important that all of the AGND pins be connected to the system analog ground. These pins isolate the input and output of each switch. Without connecting these pins, the OFF-isolation will degrade significantly.

The circuit was tested with an SSM2131 high slew rate audio amplifier and the results are shown in Figures 24 and 25. This configuration yields excellent THD performance that is primarily determined by the amplifier. Also, the headroom is now +24 dBu (0 dBu = 0.775 V rms), which is due to the amplifier's output voltage swing. Thus, even though the SSM2404 has a ± 12 V limitation on its supplies, it can be used in systems with much higher voltage ranges. For example, the double-pole double-throw switch from Figure 22 can be reconfigured in the virtual ground mode to allow higher voltage swings, as shown in Figure 26. This application realizes the excellent performance of Figures 24 and 25 while providing a low cost switching solution.



Dimensions shown in inches and (mm).

Figure 1: Mechanical drawing of the test specimen. The drawing shows a top view and a side view of a rectangular specimen. The top view includes dimensions for the overall size (1.060 x 0.280), a central hole (0.925 x 0.240), and a pin location (0.210 from the left edge). The side view shows a thickness of 0.060 and a central slot (0.015 wide). A detailed view of the bottom edge shows a series of pins with dimensions for their spacing (0.022, 0.100, 0.070) and heights (0.200, 0.125). A 'SEATING PLANE' is indicated at the bottom right.