

Data Sheet

### **FEATURES:**

- High Gain:
  - Typically 32 dB gain across 2.4–2.5 GHz over temperature 0°C to +85°C
- · High linear output power:
  - >29 dBm P1dB
    - Please refer to "Absolute Maximum Stress Ratings" on page 4
  - Meets 802.11g OFDM ACPR requirement up to 25 dBm
  - Added EVM~4% up to 23 dBm for 54 Mbps 802.11g signal
  - Added EVM~3.5% up to 23 dBm for application over 2.3–2.4 GHz or 2.5–2.6 GHz WiBro/WiMax frequency bands
  - Meets 802.11b ACPR requirement up to 25 dBm
- High power-added efficiency/Low operating current for both 802.11g/b applications
  - $\sim 26\%/300 \text{ mA } @ P_{OUT} = 24 \text{ dBm for } 802.11g$
  - $\sim 27\%/350 \text{ mA}$  @  $P_{OUT} = 25 \text{ dBm for } 802.11 \text{ b}$
- Built-in Ultra-low I<sub>REF</sub> power-up/down control
  - I<sub>BFF</sub> ~2 mA
- Low idle current
  - ~70 mA  $I_{CQ}$

### • High-speed power-up/down

- Turn on/off time (10%-90%) <100 ns
- Typical power-up/down delay with driver delay included <200 ns</li>
- · High temperature stability
  - ~1 dB gain/power variation between 0°C to +85°C
  - ~1 dB detector variation over 0°C to +85°C
- Low shut-down current (< 0.1 μA)
- · On-chip power detection
- 25 dB dynamic range on-chip power detection
- Simple input/output matching
- Packages available
  - 16-contact VQFN (3mm x 3mm)
- All non-Pb (lead-free) devices are RoHS compliant

### **APPLICATIONS:**

- WLAN (IEEE 802.11g/b)
- Home RF
- · Cordless phones
- 2.4 GHz ISM wireless equipment

### PRODUCT DESCRIPTION

The SST12LP15A is a high-power and high-gain power amplifier based on the highly-reliable InGaP/GaAs HBT technology.

The SST12LP15A can be easily configured for high-power applications with superb power-added efficiency while operating over the 2.4-2.5 GHz frequency band. It typically provides 32 dB gain with 26% power-added efficiency @  $P_{OUT} = 24$  dBm for 802.11g and 27% power-added efficiency @  $P_{OUT} = 25$  dBm for 802.11b.

The SST12LP15A has excellent linearity, typically ~4% added EVM at 23 dBm output power which is essential for 54 Mbps 802.11g operation while meeting 802.11g spectrum mask at 25 dBm. This device can be configured for applications with an added EVM of approximately 3.5%, up to 23 dBm over 2.3–2.4 GHz or 2.5–2.6 GHz WiBro/WiMax frequency bands. SST12LP15A also has widerange (>25 dB), temperature-stable (~1 dB over 85°C), single-ended/differential power detectors which lower users' cost on power control.

The power amplifier IC also features easy board-level usage along with high-speed power-up/down control. Ultra-low reference current (total I<sub>REF</sub> ~2 mA) makes the SST12LP15A controllable by an on/off switching signal directly from the baseband chip. These features coupled with low operating current make the SST12LP15A ideal for the final stage power amplification in battery-powered 802.11g/b WLAN transmitter applications.

The SST12LP15A is offered in 16-contact VQFN package. See Figure 2 for pin assignments and Table 1 for pin descriptions.

**Data Sheet** 

### **FUNCTIONAL BLOCKS**

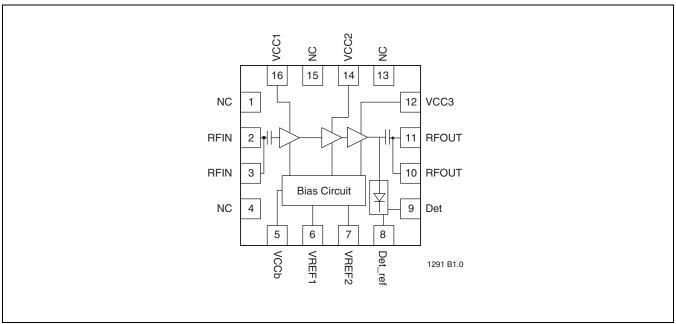


FIGURE 1: Functional Block Diagram



### **PIN ASSIGNMENTS**

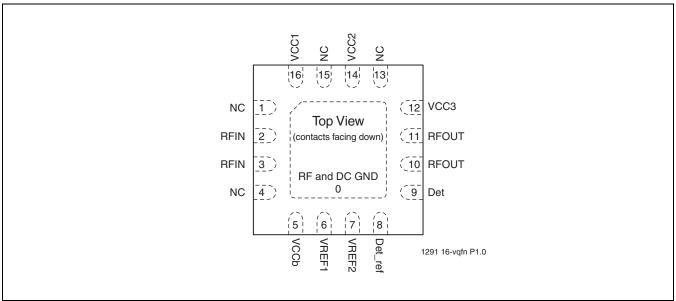


FIGURE 2: Pin Assignments for 16-contact VQFN

### **PIN DESCRIPTIONS**

**TABLE 1: Pin Description** 

| Symbol  | Pin No. | Pin Name      | Type <sup>1</sup> | Function  |  |  |
|---------|---------|---------------|-------------------|---|--|--|
| GND     | 0       | Ground        |                   | The center pad should be connected to RF ground with several low inductance, low resistance vias. |  |  |
| NC      | 1       | No Connection |                   | Unconnected pins.   |  |  |
| RFIN    | 2       |               | ı                 | RF input, DC decoupled  |  |  |
| RFIN    | 3       |               | I                 | RF input, DC decoupled  |  |  |
| NC      | 4       | No Connection |                   | Unconnected pins.   |  |  |
| VCCb    | 5       | Power Supply  | PWR               | Supply voltage for bias circuit   |  |  |
| VREF1   | 6       |               | PWR               | 1st and 2nd stage idle current control  |  |  |
| VREF2   | 7       |               | PWR               | 3rd stage idle current control  |  |  |
| Det_ref | 8       |               | 0                 | On-chip power detector reference  |  |  |
| Det     | 9       |               | 0                 | On-chip power detector  |  |  |
| RFOUT   | 10      |               | 0                 | RF output   |  |  |
| RFOUT   | 11      |               | 0                 | RF output   |  |  |
| VCC3    | 12      | Power Supply  | PWR               | Power supply, 3rd stage   |  |  |
| NC      | 13      | No Connection |                   | Unconnected pins.   |  |  |
| VCC2    | 14      | Power Supply  | PWR               | Power supply, 2nd stage   |  |  |
| NC      | 15      | No Connection |                   | Unconnected pins.   |  |  |
| VCC1    | 16      | Power Supply  | PWR               | Power supply, 1st stage   |  |  |

1. I=Input, O=Output

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### **ELECTRICAL SPECIFICATIONS**

The AC and DC specifications for the power amplifier interface signals. Refer to Table 2 for the DC voltage and current specifications. Refer to Figures 3 through 12 for the RF performance.

**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

| Input power to pins 2 and 3 (P <sub>IN</sub> )                                  | +5 dBm               |
|---|----------------------|
| Average output power (P <sub>OUT</sub> ) <sup>1</sup>                           | +28 dBm              |
| Supply Voltage at pins 5, 12, 14, 16 (V <sub>CC</sub> )                         | 0.3V to +4.6V        |
| Reference voltage to pins 6 (V <sub>REF1</sub> ) and pin 7 (V <sub>REF2</sub> ) | 0.3V to +3.6V        |
| DC supply current (I <sub>CC</sub> )  | 500 mA               |
| Operating Temperature (T <sub>A</sub> )   | 40°C to +85°C        |
| Storage Temperature (T <sub>STG</sub> )   | 40°C to +120°C       |
| Maximum Junction Temperature (T <sub>J</sub> )                                  | +150°C               |
| Surface Mount Solder Reflow Temperature   | 260°C for 10 seconds |

<sup>1.</sup> Never measure with CW source. Pulsed single-tone source with <50% duty cycle is recommended. Exceeding the maximum rating of average output power could cause permanent damage to the device.

### **Operating Range**

| Range      | Ambient Temp   | V <sub>CC</sub> |  |  |
|------------|----------------|-----------------|--|--|
| Industrial | -40°C to +85°C | 3.3V            |  |  |

### **TABLE 2: DC Electrical Characteristics**

| Symbol            | Parameter   | Min. | Тур  | Max. | Unit | Test Conditions |
|-------------------|---|------|------|------|------|-----------------|
| V <sub>CC</sub>   | Supply Voltage at pins 5, 12, 14, 16                        | 3.0  | 3.3  | 4.2  | V    |                 |
| I <sub>CC</sub>   | Supply Current  |      |      |      |      |                 |
|                   | for 802.11g, 24 dBm   |      | 300  |      | mA   |                 |
|                   | for 802.11b, 25 dBm   |      | 350  |      | mA   |                 |
| I <sub>CQ</sub>   | Idle current for 802.11g to meet EVM<4% @ 23dBm             |      | 70   |      | mA   |                 |
| I <sub>OFF</sub>  | Shut down current   |      |      | 0.1  | μΑ   |                 |
| V <sub>REG1</sub> | Reference Voltage for 1st Stage, with 169 $\Omega$ resistor | 2.85 | 2.90 | 2.95 | V    |                 |
| $V_{REG2}$        | Reference Voltage for 2nd Stage, with $140\Omega$ resistor  | 2.85 | 2.90 | 2.95 | V    |                 |

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**TABLE 3: AC Electrical Characteristics for Configuration** 

| Symbol                    | Parameter   | Min. | Тур | Max. | Unit   |
|---------------------------|---|------|-----|------|--------|
| F <sub>L-U</sub>          | Frequency range in 802.11b/g applications (see Figure 13)                               | 2400 |     | 2485 | MHz    |
| F <sub>L-U</sub>          | Frequency range in 2.3-2.4 GHz applications (see Figure 14)                             | 2300 |     | 2400 | MHz    |
| F <sub>L-U</sub>          | Frequency range in 2.5-2.6 GHz applications (see Figure 15)                             | 2500 |     | 2600 | MHz    |
| Pout                      | Output power  |      |     |      |        |
|                           | @ PIN = -10 dBm 11b signals   |      | 23  |      | dBm    |
|                           | @ PIN = -10 dBm 11g signals   |      | 23  |      | dBm    |
| G                         | Small signal gain   | 31   | 32  |      | dB     |
| G <sub>VAR1</sub>         | Gain variation over each band (2400-2485 MHz)   |      |     | ±0.5 | dB     |
| G <sub>VAR2</sub>         | Gain ripple over channel (Gain variation over 20 MHz)                                   |      | 0.2 |      | dB     |
| Output VSWR<br>Ruggedness | Survivable time @ 25 dBm (to $50\Omega$ ) 54 Mbps OFDM signal when VSWR=10:1 all phases | 10   |     |      | second |
| ACPR                      | Meet 11b spectrum mask  | 24   | 25  |      | dBm    |
|                           | Meet 11g OFDM 54 MBPS spectrum mask   | 24   | 25  |      | dBm    |
| Added EVM                 | @ 23 dBm output with 11g OFDM 54 MBPS signal  |      | 3.5 |      | %      |
| 2f, 3f, 4f, 5f            | Harmonics at 22 dBm, without trapping capacitors  |      |     | -40  | dBc    |

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### TYPICAL PERFORMANCE CHARACTERISTICS

TEST CONDITIONS:  $V_{CC} = 3.3V$ ,  $T_A = 25^{\circ}C$ 

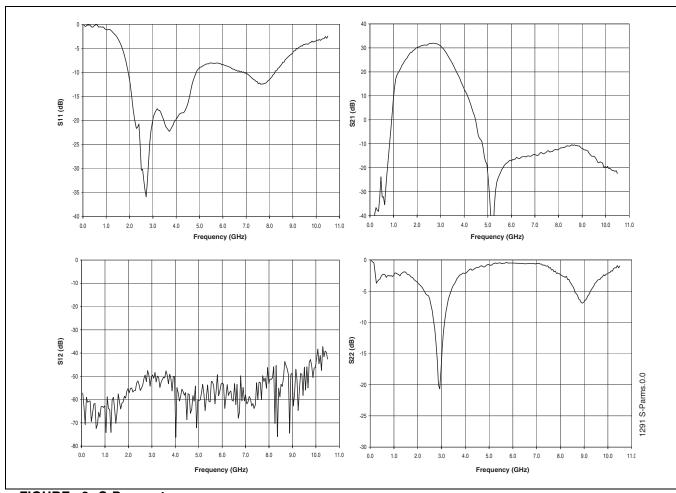


FIGURE 3: S-Parameters

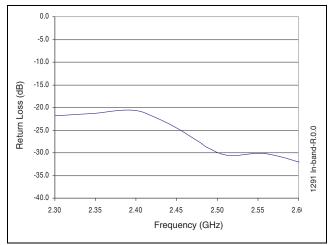


FIGURE 4: In-band Return Loss

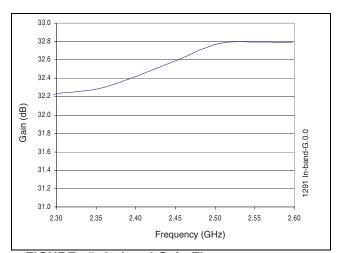


FIGURE 5: In-band Gain Flatness



# TYPICAL PERFORMANCE CHARACTERISTICS TEST CONDITIONS: F1 = 2.45 GHz, F2 = 2.451 GHz, $V_{CC}$ = 3.3V, $T_A$ = 25°C

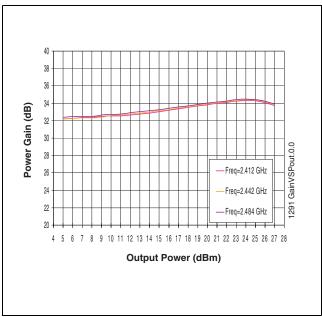


FIGURE 6: Gain vs Pout

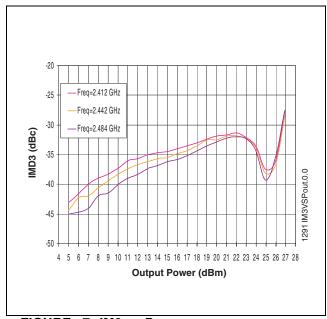


FIGURE 7: IM3 vs Pout

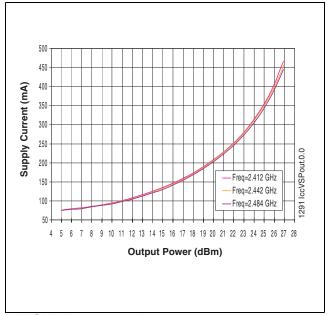


FIGURE 8: I<sub>CC</sub> vs P<sub>OUT</sub>

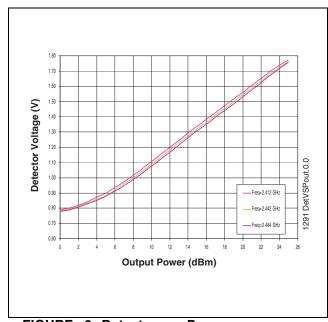


FIGURE 9: Detectors vs Pout



### TYPICAL PERFORMANCE CHARACTERISTICS

TEST CONDITIONS: V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C, 54 MBPS 802.11G OFDM SIGNAL

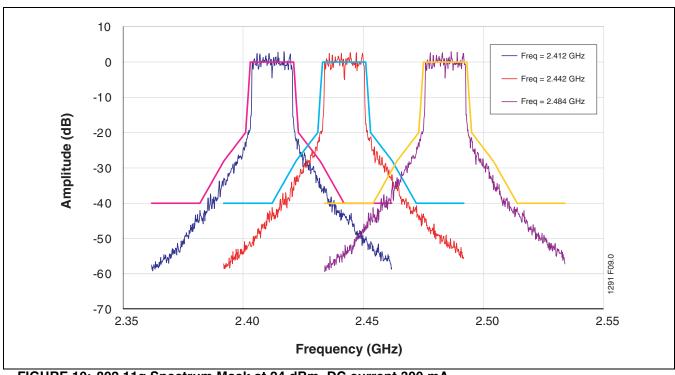


FIGURE 10: 802.11g Spectrum Mask at 24 dBm, DC current 300 mA

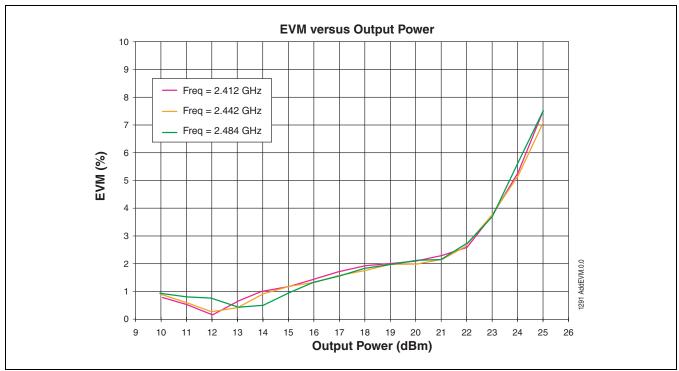


FIGURE 11: 802.11g Spectrum Mask at 23/24 dBm, DC current 240/290 mA



## TYPICAL PERFORMANCE CHARACTERISTICS TEST CONDITIONS: $V_{CC} = 3.3V$ , $T_{A}=25^{\circ}C$ , 1 MBPS 802.11B CCK SIGNAL

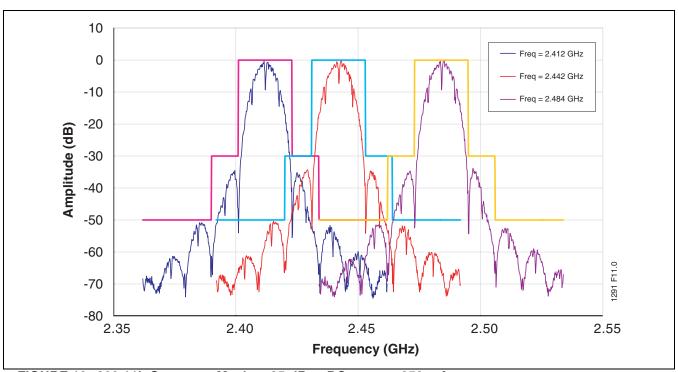


FIGURE 12: 802.11b Spectrum Mask at 25 dBm, DC current 350 mA

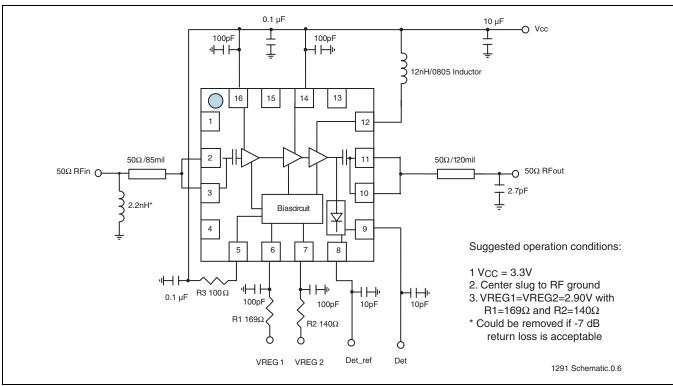


FIGURE 13: Typical Schematic for High-Power, High-Efficiency 802.11b/g Applications

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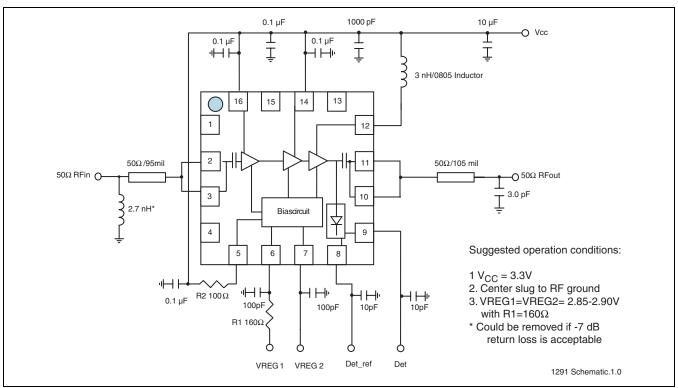


FIGURE 14: Typical Schematic for High-Power, High-Efficiency 2.3-2.4 GHz Applications

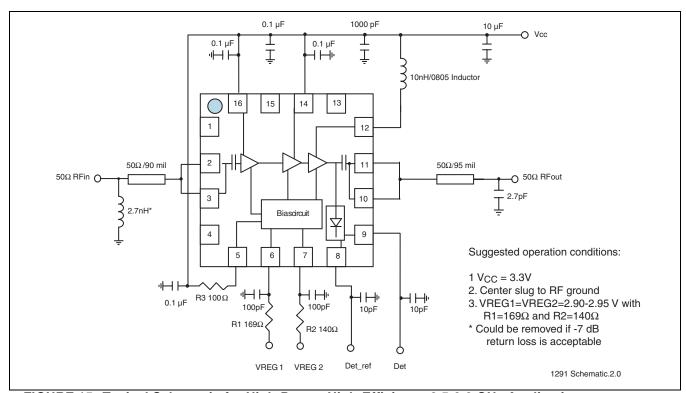
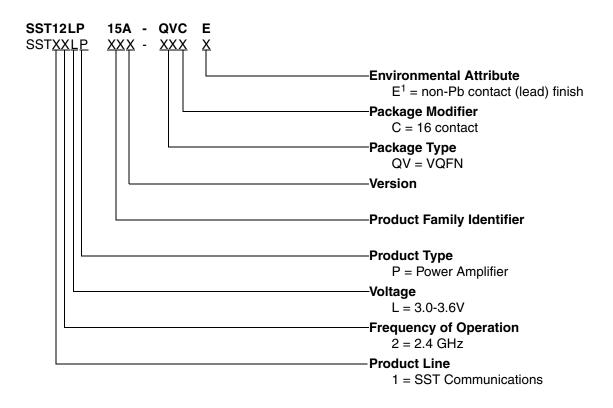


FIGURE 15: Typical Schematic for High-Power, High-Efficiency 2.5-2.6 GHz Applications



### PRODUCT ORDERING INFORMATION



Environmental suffix "E" denotes non-Pb solder. SST non-Pb solder devices are "RoHS Compliant".

### Valid combinations for SST12LP15A

SST12LP15A-QVCE

### SST12LP15A Evaluation Kits

SST12LP15A-QVCE-K

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

**Data Sheet** 

### **PACKAGING DIAGRAMS**

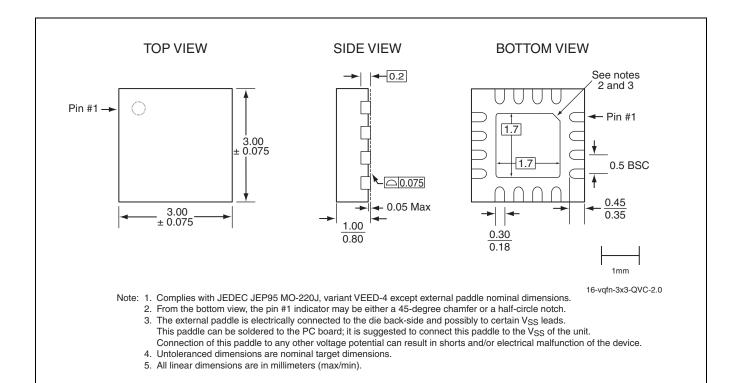


FIGURE 16: 16-contact Very-thin Quad Flat No-lead (VQFN)
SST Package Code: QVC

**TABLE 4: Revision History** 

| Revision |  | Description   |          |  |
|----------|--|---|----------|--|
| 00       | •  | Initial release of data sheet                           | Mar 2005 |  |
| 01       | •  | Updated values for gain and efficiency on page 1        | Mar 2006 |  |
|          | •  | Updated values for VREG1 and VREG2 in Table 2 on page 4 |          |  |
|          | Removed stability parameter from Table 3 on page 5 |   |          |  |
|          | •  | Updated the typical application schematic on page 9     |          |  |
|          | •  | Updated QVC package drawing.                            |          |  |
|          | •  | Updated "Absolute Maximum Stress Ratings" on page 4     |          |  |
| 02       | •  | Added information for 2.3-2.4 and 2.5-2.6 applications  | Jul 2006 |  |
|          | •  | Removed leaded part numbers                             |          |  |



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