



# STGB20NB37LZ

## N-CHANNEL CLAMPED 20A D<sup>2</sup>PAK INTERNALLY CLAMPED PowerMESH™ IGBT

PRELIMINARY DATA

TYPE	V <sub>CES</sub>	V <sub>CE(sat)</sub>	I <sub>C</sub>
STGB20NB37LZ	CLAMPED	< 2.0 V	20 A

- POLYSILICON GATE VOLTAGE DRIVEN
- LOW THRESHOLD VOLTAGE
- LOW ON-VOLTAGE DROP
- HIGH CURRENT CAPABILITY
- HIGH VOLTAGE CLAMPING FEATURE
- SURFACE-MOUNTING D<sup>2</sup>PAK (TO-263)  
POWER PACKAGE IN TUBE (NO SUFFIX)  
OR IN TAPE & REEL (SUFFIX "T4")

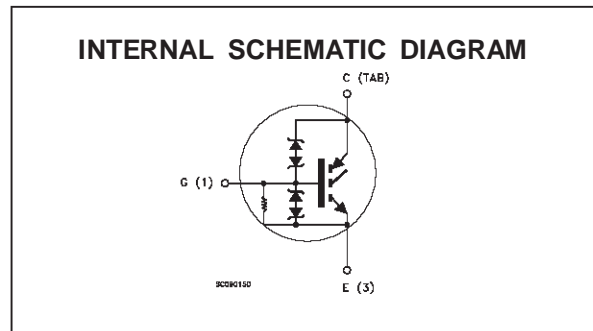
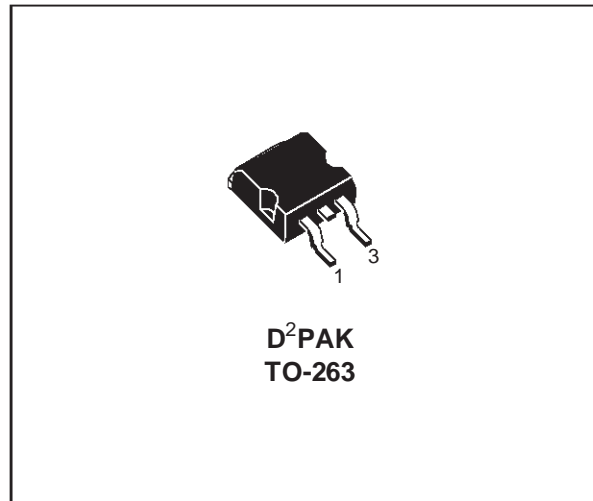
### DESCRIPTION

Using the latest high voltage technology based on patented strip layout, STMicroelectronics has designed an advanced family of IGBTs with outstanding performances.

The built in collector-gate zener exhibits a very precise active clamping while the gate-emitter zener supplies an ESD protection.

### APPLICATIONS

- AUTOMOTIVE IGNITION



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CES</sub>	Collector-Emitter Voltage (V <sub>GS</sub> = 0)	CLAMPED	V
V <sub>ECR</sub>	Reverse Battery Protection	20	V
V <sub>GE</sub>	Gate-Emitter Voltage	CLAMPED	V
I <sub>C</sub>	Collector Current (continuous) at T <sub>c</sub> = 25 °C	40	A
I <sub>C</sub>	Collector Current (continuous) at T <sub>c</sub> = 100 °C	30	A
I <sub>CM(•)</sub>	Collector Current (pulsed)	80	A
E <sub>AS</sub>	Single Pulse Energy T <sub>c</sub> = 25 °C	700	mJ
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	150	W
	Derating Factor	1	W/°C
E <sub>SD</sub>	ESD (Human Body Model)	4	KV
T <sub>stg</sub>	Storage Temperature	-65 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

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### THERMAL DATA

R <sub>thj-case</sub>	Thermal Resistance Junction-case	Max	1	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient	Max	62.5	°C/W
R <sub>thc-sink</sub>	Thermal Resistance Case-sink	Typ	0.2	°C/W

### ELECTRICAL CHARACTERISTICS (T<sub>j</sub> = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV <sub>(CES)</sub>	Clamped Voltage	I <sub>C</sub> = 2mA V <sub>GE</sub> = 0 T <sub>C</sub> = - 40°C	380	405	430	V
		I <sub>C</sub> = 2mA V <sub>GE</sub> = 0 T <sub>C</sub> = 25°C	375	400	425	V
		I <sub>C</sub> = 2mA V <sub>GE</sub> = 0 T <sub>C</sub> = 150°C	370	395	420	V
BV <sub>(ECR)</sub>	Emitter Collector Break-down Voltage	I <sub>C</sub> = 75 mA T <sub>C</sub> = 25°C	20	28		V
BV <sub>GE</sub>	Gate Emitter Break-down Voltage	I <sub>G</sub> = ± 2 mA	12	14	16	V
I <sub>CES</sub>	Collector cut-off Current (V <sub>GE</sub> = 0)	V <sub>CE</sub> = 15 V V <sub>GE</sub> = 0 T <sub>C</sub> = 150 °C			10	μA
		V <sub>CE</sub> = 200 V V <sub>GE</sub> = 0 T <sub>C</sub> = 150 °C			100	μA
I <sub>GES</sub>	Gate-Emitter Leakage Current (V <sub>CE</sub> = 0)	V <sub>GE</sub> = ± 10 V V <sub>CE</sub> = 0	± 300	± 660	± 1000	μA
R <sub>GE</sub>	Gate Emitter Resistance		10	15	30	KΩ

ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GE(th)</sub>	Gate Threshold Voltage	V <sub>CE</sub> = V <sub>GE</sub> I <sub>C</sub> = 250μA T <sub>C</sub> = - 40°C	1.2			V
		V <sub>CE</sub> = V <sub>GE</sub> I <sub>C</sub> = 250μA T <sub>C</sub> = 25°C	1.0	1.4	2	V
		V <sub>CE</sub> = V <sub>GE</sub> I <sub>C</sub> = 250μA T <sub>C</sub> = 150°C	0.6			V
V <sub>CE(SAT)</sub>	Collector-Emitter Saturation Voltage	V <sub>GE</sub> = 4.5 V I <sub>C</sub> = 10 A T <sub>C</sub> = 25°C		1.1	1.8	V
		V <sub>GE</sub> = 4.5 V I <sub>C</sub> = 10 A T <sub>C</sub> = 150 °C		1.0	1.7	V
		V <sub>GE</sub> = 4.5 V I <sub>C</sub> = 20 A T <sub>C</sub> = 25°C		1.35	2.0	V
		V <sub>GE</sub> = 4.5 V I <sub>C</sub> = 20 A T <sub>C</sub> = 150 °C		1.25	2.0	V

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub>	Forward Transconductance	V <sub>CE</sub> = 25 V I <sub>C</sub> = 20 A		35		S
C <sub>ies</sub>	Input Capacitance	V <sub>CE</sub> = 25 V f = 1 MHz V <sub>GE</sub> = 0		2300		pF
C <sub>oes</sub>	Output Capacitance			165		pF
C <sub>res</sub>	Reverse Transfer Capacitance			28		pF
Q <sub>G</sub>	Gate Charge	V <sub>CE</sub> = 280 V I <sub>C</sub> = 20 A V <sub>GE</sub> = 5 V		51		nC

## FUNCTIONAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
II	Latching Current	$V_{CLAMP} = 250\text{ V}$ $R_{G\text{OFF}} = 1\text{ K}\Omega$	80			A
U.I.S.	Functional Test Open Secondary Coil	$R_{G\text{OFF}}=1\text{ K}\Omega$ L =3 mH $T_C = 25\text{ }^\circ\text{C}$	21.6	26		A
		$R_{G\text{OFF}}=1\text{ K}\Omega$ L =3 mH $T_C = 150\text{ }^\circ\text{C}$	15	18		A

## SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(\text{on})}$	Delay Time	$V_{CC} = 250\text{ V}$		2.3		$\mu\text{s}$
$t_r$	Rise Time	$V_{GE} = 4.5\text{ V}$ $R_G = 1\text{ K}\Omega$		0.6		$\mu\text{s}$
$(di/dt)_{\text{on}}$	Turn-on Current Slope	$V_{CC} = 250\text{ V}$ $R_G = 1\text{ K}\Omega$		550		A/ $\mu\text{s}$
$E_{\text{on}}$	Turn-on Switching Losses	$V_{CC}=250\text{V}$ $I_C =20\text{A}$ $T_C = 25\text{ }^\circ\text{C}$		8.8		mJ
		$R_G =1\text{ K}\Omega$ $V_{GE} =4.5\text{V}$ $T_C = 150\text{ }^\circ\text{C}$		9.2		mJ

## SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_c$	Cross-Over Time	$V_{CC} = 250\text{ V}$		4.8		$\mu\text{s}$
$t_r(V_{\text{off}})$	Off Voltage Rise Time	$R_{GE} = 1\text{ K}\Omega$		2.6		$\mu\text{s}$
$t_f$	Fall Time	$V_{GE} = 4.5\text{ V}$		2.0		$\mu\text{s}$
$t_{d(\text{off})}$	Off Voltage Delay Time			11.5		$\mu\text{s}$
$E_{\text{off}}^{(**)}$	Turn-off Switching Loss			11.8		mJ
$t_c$	Cross-Over Time	$V_{CC} = 250\text{ V}$		7.8		$\mu\text{s}$
$t_r(V_{\text{off}})$	Off Voltage Rise Time	$R_{GE} = 1\text{ K}\Omega$		3.5		$\mu\text{s}$
$t_f$	Fall Time	$T_C = 150\text{ }^\circ\text{C}$		3.9		$\mu\text{s}$
$t_{d(\text{off})}$	Off Voltage Delay Time			12.0		$\mu\text{s}$
$E_{\text{off}}^{(**)}$	Turn-off Switching Loss			17.8		mJ

(\*) Pulse width limited by safe operating area (\*) Pulsed: Pulse duration = 300 ms, duty cycle 1.5 % (\*\*)Losses Include Also The Tail (jedec Standardization)

Fig. 1: Unclamped Inductive Load Test Circuit

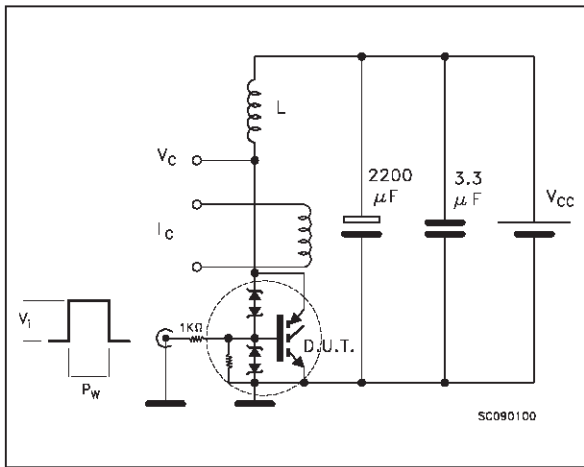


Fig. 2: Unclamped Inductive Waveform

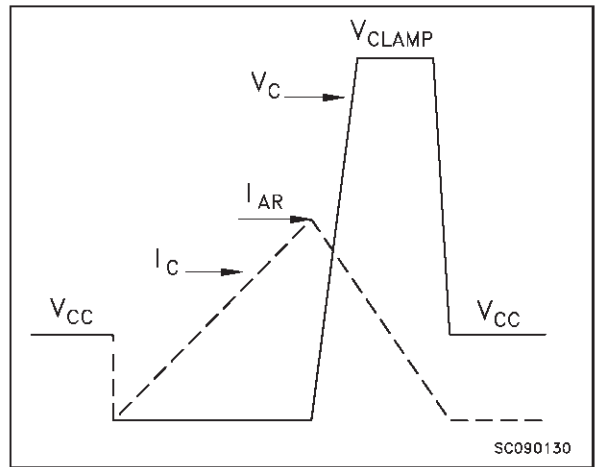


Fig. 3: Switching Times Test Circuits For Resistive Load

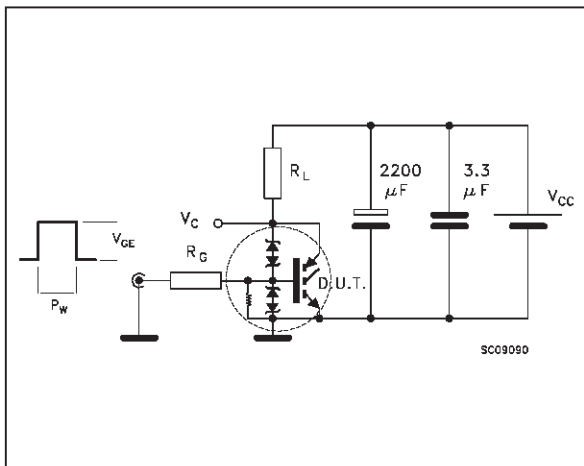


Fig. 4: Gate Charge test Circuit

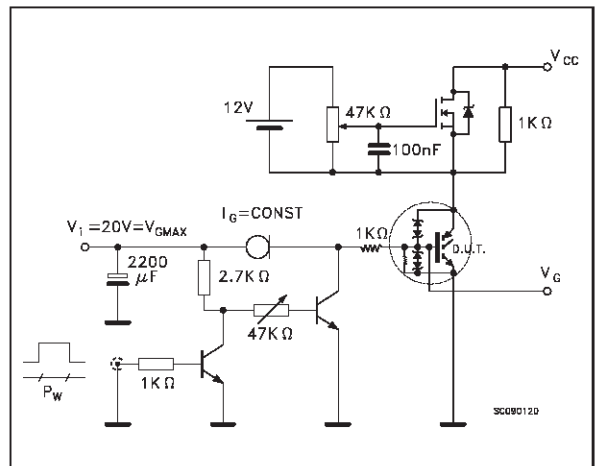
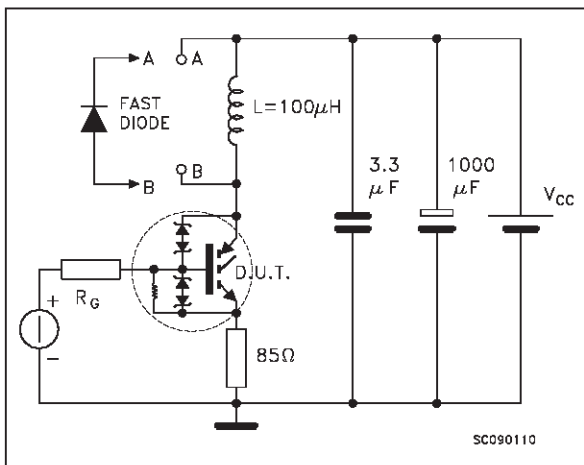
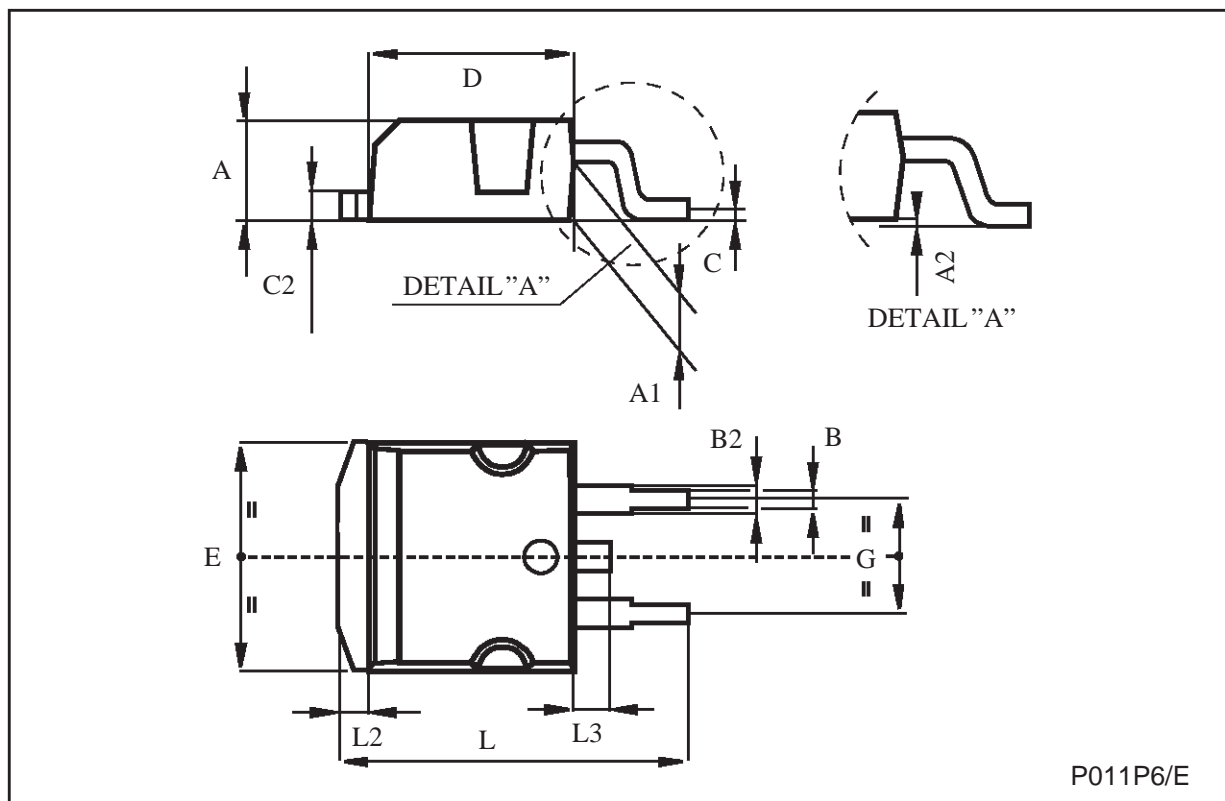


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-263 (D<sup>2</sup>PAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.21		1.36	0.047		0.053
D	8.95		9.35	0.352		0.368
E	10		10.4	0.393		0.409
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068



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