



STL27N15

N-CHANNEL 150V - 0.045 Ω - 27A PowerFLAT™ LOW GATE CHARGE STRIPFET™ MOSFET

TARGET DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STL15N15	150 V	<0.060 Ω	27 A ⁽¹⁾

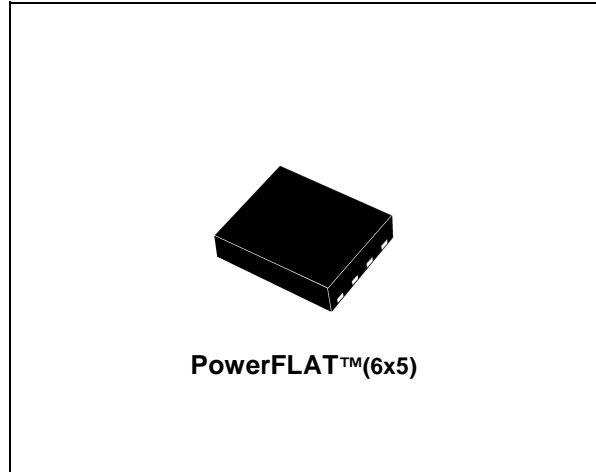
- TYPICAL R_{DS(on)} = 0.045 Ω
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE (1mm MAX)
- VERY LOW THERMAL RESISTANCE
- VERY LOW GATE CHARGE

DESCRIPTION

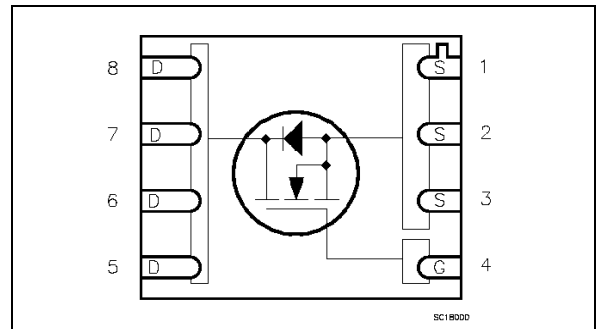
This MOSFET series realized with STMicroelectronics unique "StripFET™" process has specifically been designed to minimize input capacitance and gate charge. It's therefore suitable as primary switch in advanced high efficiency, high frequency isolated DC-DC converter for telecom and computer application. The new PowerFLAT™ package allows a significant reduction in a board space without compromising performance.

APPLICATIONS

- HIGH-EFFICIENCY ISOLATED DC-DC CONVERTERS
- TELECOM AND BATTERY CHARGER ADAPTOR
- SYNCHRONOUS RECTIFICATION



INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STL27N15	L27N15	PowerFLAT	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	150	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	150	V
V _{GS}	Gate- source Voltage	\pm 20	V
I _D	Drain Current (continuous) at T _C = 25°C (Steady State)	6	A
I _D	Drain Current (continuous) at T _C = 100°C	4	A
I _{DM} ⁽³⁾	Drain Current (pulsed)	24	A
P _{tot} ⁽²⁾	Total Dissipation at T _C = 25°C (Steady State)	4	W
P _{tot} ⁽¹⁾	Total Dissipation at T _C = 25°C	80	W
	Derating Factor	0.03	W/°C
dv/dt ⁽⁵⁾	Peak Diode Recovery voltage slope	TBD	V/ns
T _{stg}	Storage Temperature	-55 to 150	°C
T _j	Operating Junction Temperature		

STL27N15

THERMAL DATA

Rthj-F	Thermal Resistance Junction-Foot (Drain)	1.56	°C/W
Rthj-pcb(2)	Thermal Operating Junction-pcb	31.2	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	100			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			±100	nA

ON (6)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	1			V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 3 A		0.045	0.060	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (6)	Forward Transconductance	V _{DS} = 50 V I _D = 5 A		TBD		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		TBD		pF
C _{oss}	Output Capacitance			TBD		pF
C _{rss}	Reverse Transfer Capacitance			TBD		pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 50\text{ V}$ $I_D = 3\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		TBD TBD		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 50\text{ V}$ $I_D = 6\text{ A}$ $V_{GS} = 10\text{ V}$		TBD TBD TBD	28	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 50\text{ V}$ $I_D = 3\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		TBD TBD		ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(3)}$	Source-drain Current Source-drain Current (pulsed)				6 24	A A
$V_{SD}^{(6)}$	Forward On Voltage	$I_{SD} = 3\text{ A}$ $V_{GS} = 0$			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 6\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $j = 150^\circ\text{C}$ (see test circuit, Figure 5)		TBD TBD TBD		ns nC A

(1) The value is rated according R_{thj-F} .(2) When Mounted on FR-4 board of 1 inch², 2oz Cu

(3) Pulse width limited by safe operating area.

(5) $I_{SD} \leq 6\text{ A}$, $di/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.(6) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

Fig. 1: Unclamped Inductive Load Test Circuit

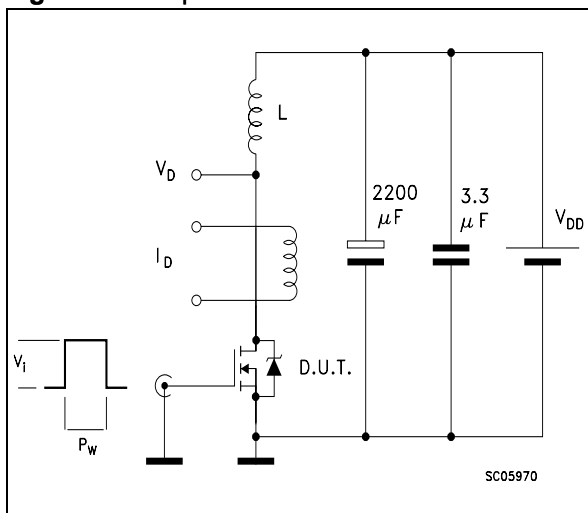


Fig. 2: Unclamped Inductive Waveform

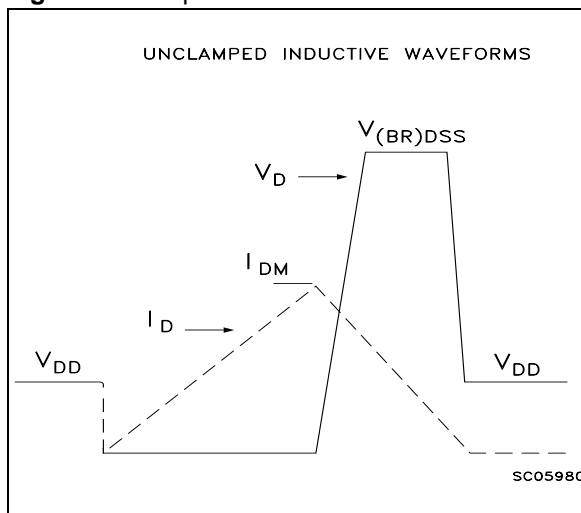


Fig. 3: Switching Times Test Circuits For Resistive Load

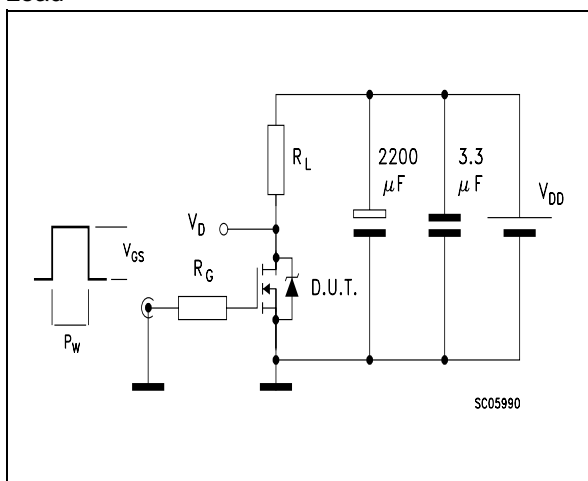


Fig. 4: Gate Charge test Circuit

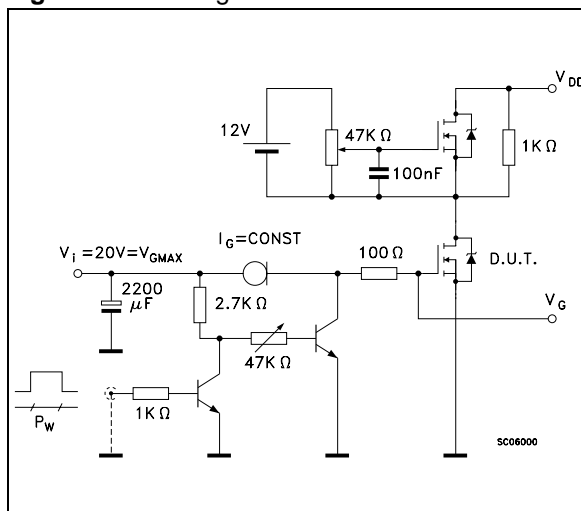
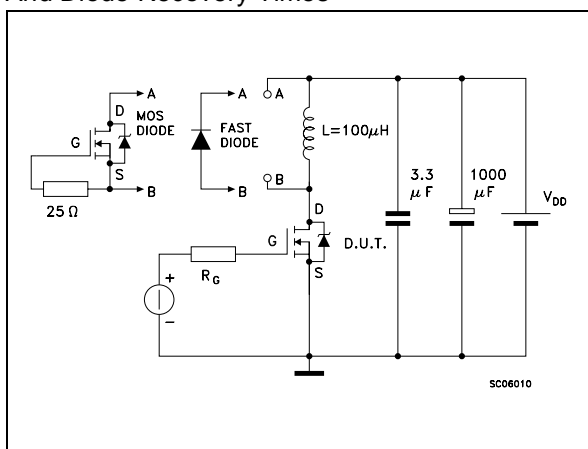
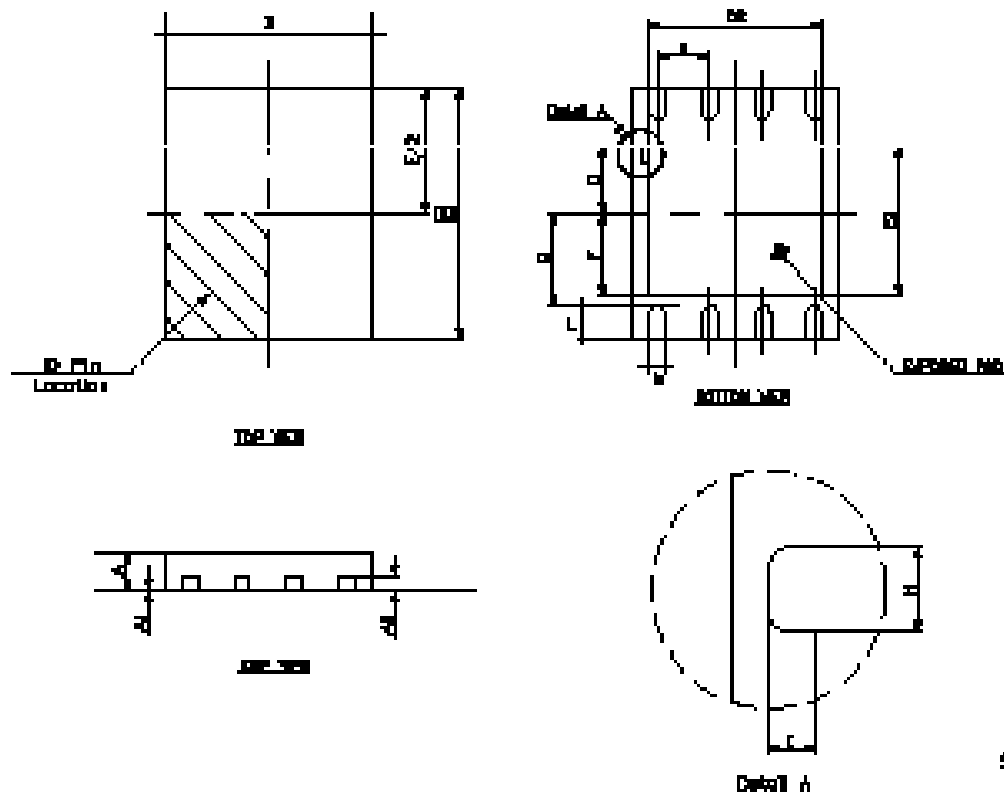


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



PowerFLAT™(6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80		1.00	0.031		0.039
A1		0.02			0.001	
b	0.35		0.47	0.014		0.018
C		1.61			0.063	
D		5.00			0.197	
D2	4.15		4.25	0.163		0.167
E		6.00			0.236	
E2	3.65		3.65	0.140		0.144
e		1.27			0.049	
F		1.99			0.078	
G		2.20			0.086	
H		0.40			0.015	
I		0.219			0.0086	
L	0.70		0.90	0.028		0.035



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is registered trademark of STMicroelectronics
© 2003 STMicroelectronics - All Rights Reserved

All other names are the property of their respective owners.

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

<http://www.st.com>