STL80NF3LL

N-CHANNEL 30V - 0.0045Ω - 80A PowerFLAT™ (6X5) STripFET™ II MOSFET

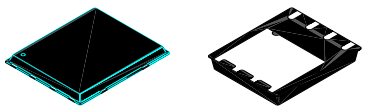
PRODUCT PREVIEW

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STL80NF3LL	30 V	< 0.0055 Ω	20 A (2)

- TYPICAL R_{DS}(on) = 0.0045 Ω @ 10V
- IMPROVED DIE-TO-FOOTPRINT RATIO
- VERY LOW PROFILE PACKAGE (1mm MAX)
- VERY LOW THERMAL RESISTANCE
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED

Figure 1: Package

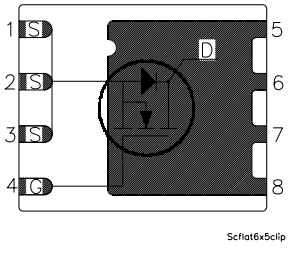


PowerFLAT™(6x5)

DESCRIPTION

The STL80NF3LL utilizes the second generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. Such features make it the best choice in high efficiency DC-DC converters for Telecom and Computer industries. The Chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

Figure 2: Internal Schematic Diagram



TOP VIEW

APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- SYNCHRONOUS RECTIFICATION

Table 2: Order Codes

Part Number	Marking	Package	Packaging
STL80NF3LL	L80NF3LL	PowerFLAT™ (6x5)	TAPE & REEL

Rev. 3

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS}= 0)	30	V
V_{GS}	Gate- source Voltage	± 16	V
I_D (1)	Drain Current (continuous) at T_C= 25°C	80	A
I_D (1)	Drain Current (continuous) at T_C= 100°C	50	A
I_{DM} (3)	Drain Current (pulsed)	320	A
I_D (2)	Drain Current (continuous) at T_C= 25°C	20	A
P_{TOT} (2)	Total Dissipation at T_C= 25°C	4	W
P_{TOT} (1)	Total Dissipation at T_C= 25°C	80	W
	Derating Factor(2)	0.03	W/°C
T_{stg}	Storage Temperature	– 55 to 150	°C
T_j	Max. Operating Junction Temperature		

Table 4: Thermal Data

Rthj-$_C$	Thermal Resistance Junction-Case (Drain)	1.56	°C/W
Rthj-pcb (2)	Thermal Operating Junction-pcb	31.3	°C/W

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 5: On /Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 16 V			± 10	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D= 250µA	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS}= 10 V, I_D= 10 A V_{GS}= 4.5 V, I_D= 10 A		0.0045 0.0055	0.0055 0.007	Ω Ω

Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (4)	Forward Transconductance	V_{DS}= 10V, I_D= 10 A		37		S
C_{iss}	Input Capacitance	V_{DS}= 25V, f= 1 MHz, V_{GS}= 0		2160		pF
C_{oss}	Output Capacitance			614		pF
C_{rss}	Reverse Transfer Capacitance			98		pF
R_G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		4.1		Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Switching On

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	V_{DD}= 15 V, I_D= 10 A R_G = 4.7Ω, V_{GS} = 4.5V (see Figure 15)		23.5 39 47.5 37		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}= 15V, I_D= 10 A, V_{GS}= 4.5 V (see Figure 17)		26 7 12	35	nC nC nC

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				20	A
I_{SDM} (3)	Source-drain Current (pulsed)				80	A
V_{SD} (4)	Forward On Voltage	I_{SD}= 20 A, V_{GS}= 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse RecoveryCharge Reverse Recovery Current	I_{SD}= 20 A, di/dt= 100 A/µs, V_{DD}= 15 V, T_j = 150°C (see Figure 16)		39 45 2.3		ns nC A

(1) The value is rated according $R_{thj\text{-}C}$.
(2) When mounted on FR-4 board of 1in², 2oz Cu., t<10sec
(3) Pulse width limited by safe operating area.
(4) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Figure 3: Safe Operating Area

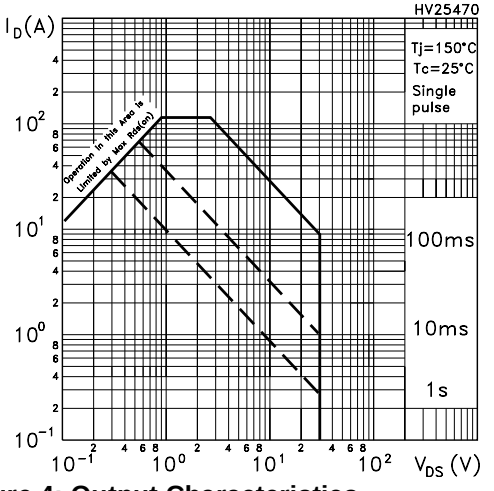


Figure 4: Output Characteristics

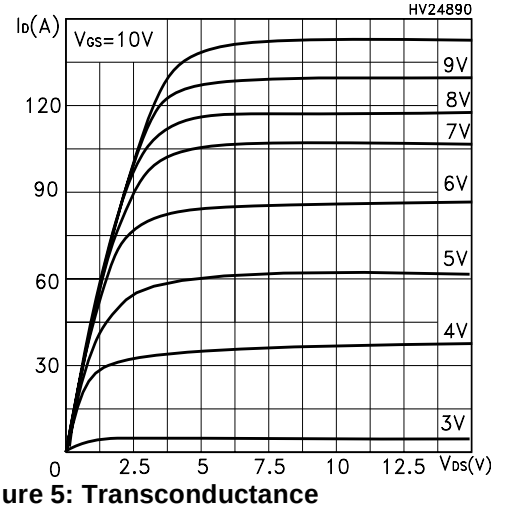


Figure 5: Transconductance

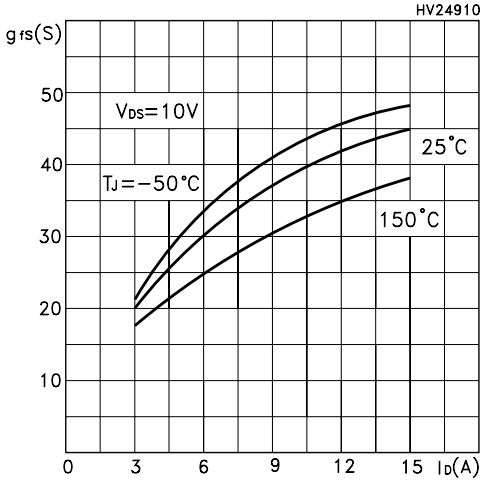


Figure 6: Thermal Impedance

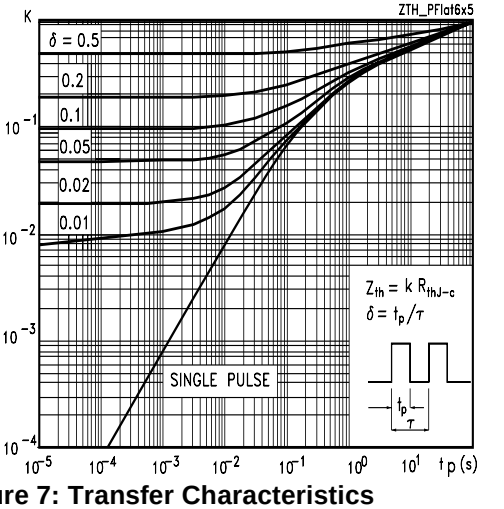


Figure 7: Transfer Characteristics

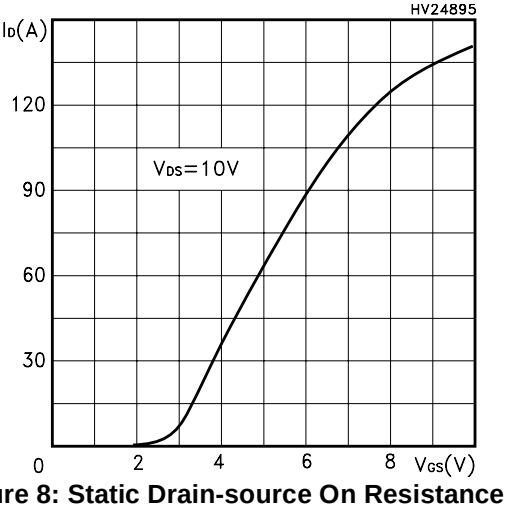


Figure 8: Static Drain-source On Resistance

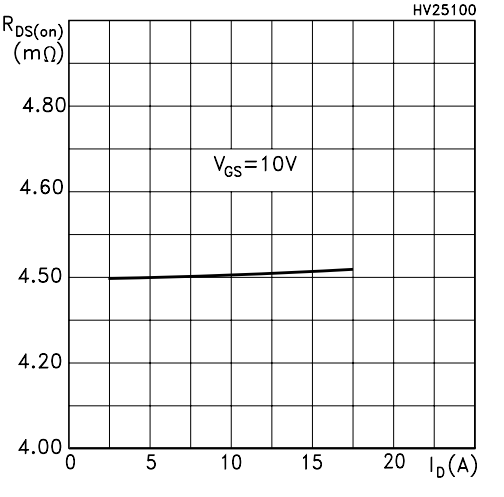


Figure 9: Gate Charge vs Gate-source Voltage

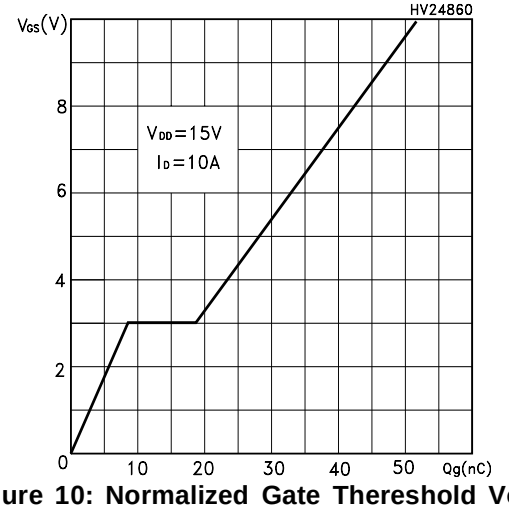


Figure 10: Normalized Gate Thereshold Voltage vs Temperature

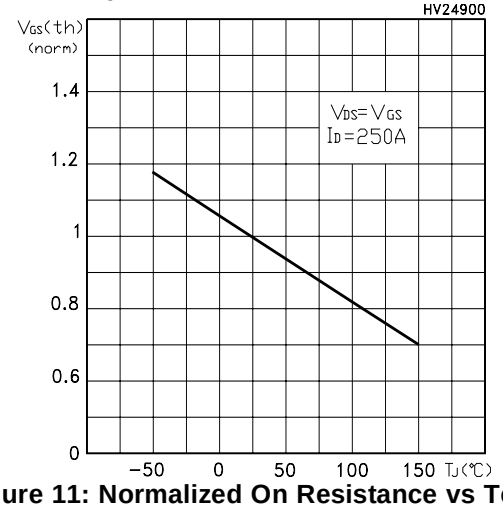


Figure 11: Normalized On Resistance vs Temperature

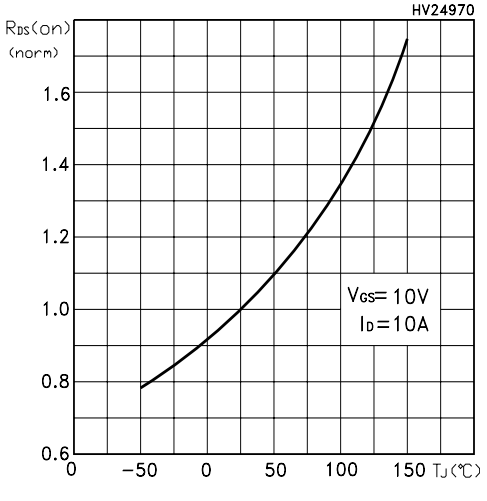


Figure 12: Capacitance Variations

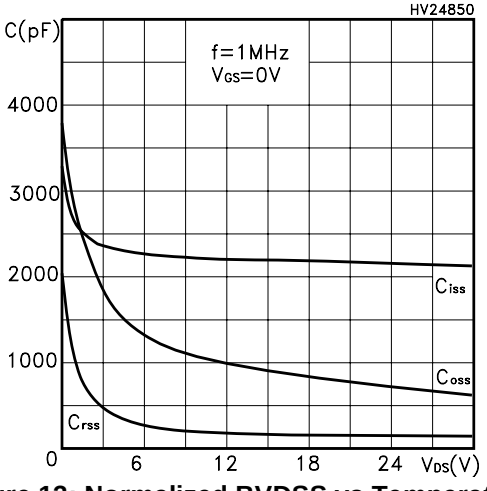


Figure 13: Normalized BVDSS vs Temperature

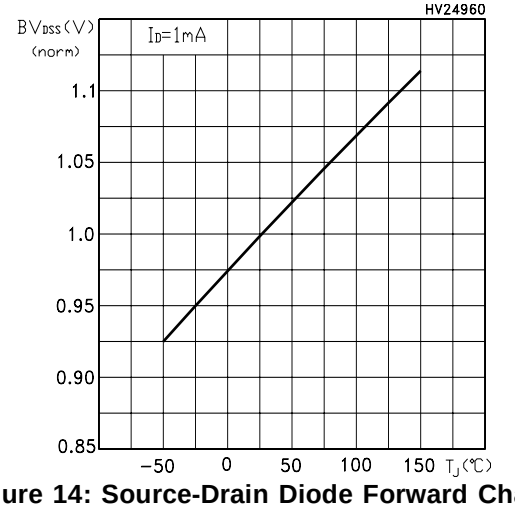


Figure 14: Source-Drain Diode Forward Characteristics

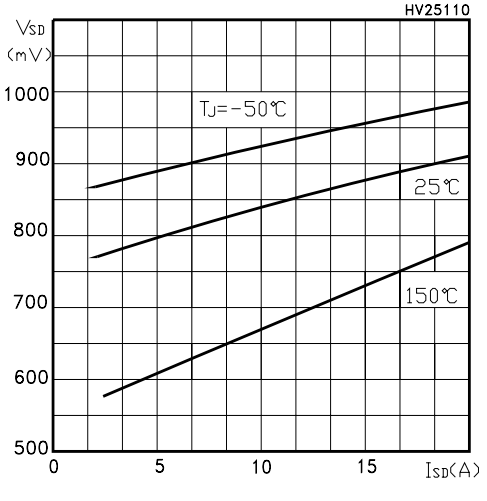


Figure 15: Switching Times Test Circuit For Resistive Load

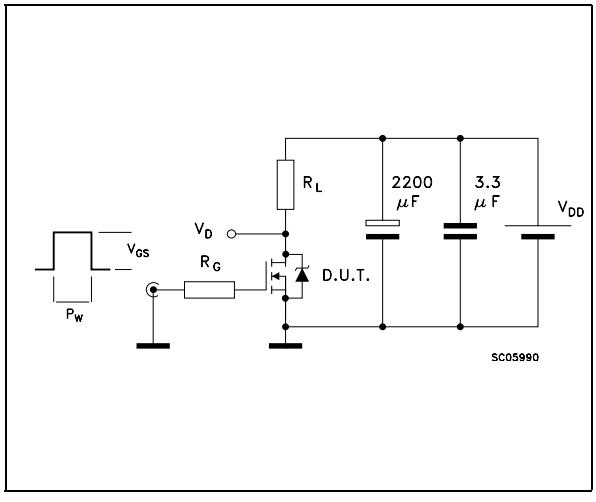


Figure 16: Test Circuit For Diode Recovery Times

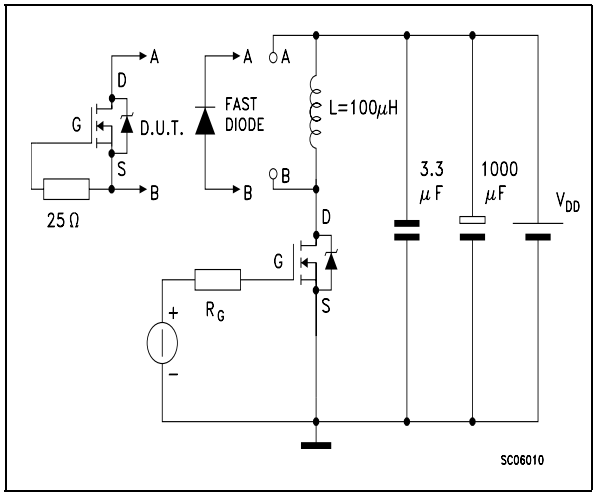
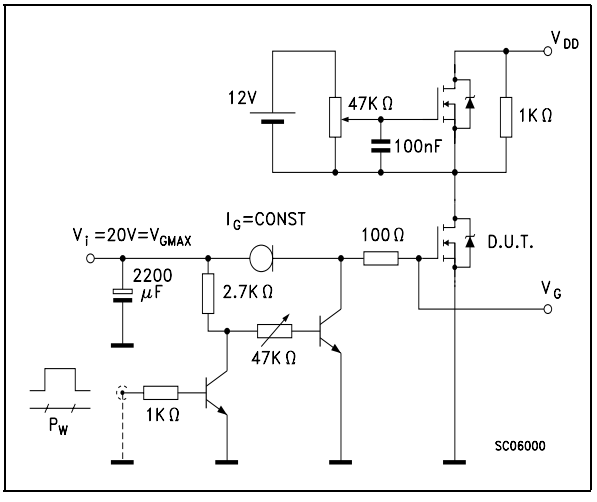
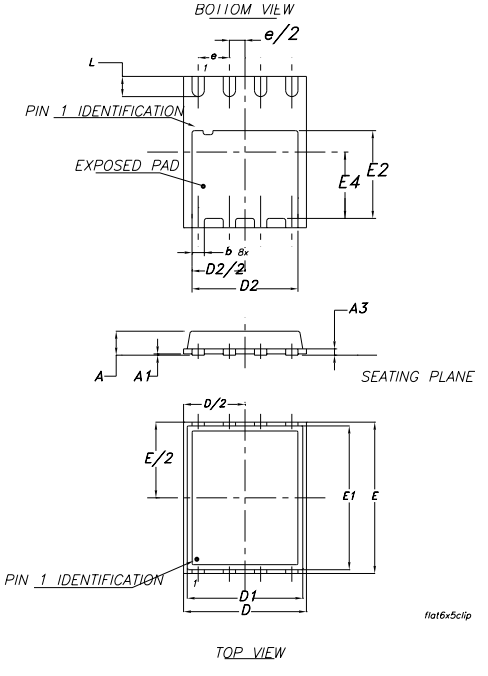


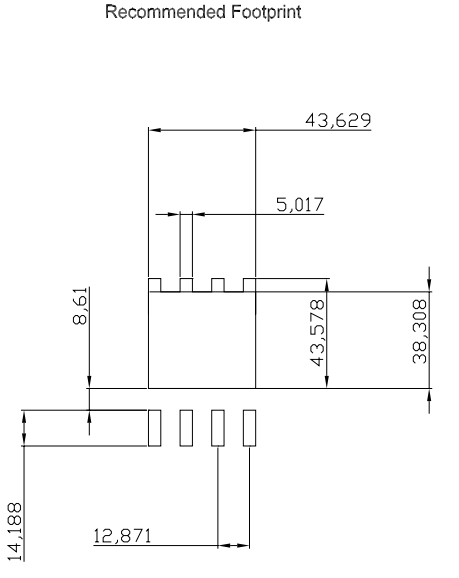
Figure 17: Gate Charge Test Circuit



PowerFLAT™ (6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035





Note: all dimentions are in mm.

Table 9: Revision History

Date	Revision	Description of Changes
18-Apr-2005	1	First Release.
20-Jun-2005	2	Updated mechanical data
22-Jun-2005	3	New R_G value on table 6