STLC2415

BLUETOOTH® BASEBAND WITH INTEGRATED FLASH

PRELIMINARY DATA

1 FEATURES

- Bluetooth® V1.1 specification compliant
- SW compatible with STLC2410B-M28R400CT combination
- 2 layer class 4 PCB compatible
- Point-to-point, point-to-multi-point (up to 7 slaves) and scatternet capability
- Asynchronous Connection Less (ACL) link support giving data rates up to 721 kbps
- Synchronous Connection Oriented (SCO) link
- Standard BlueRF bus interface
- Clock support
  - System clock input: 13 MHz external clock
  - LPO clock input at 3.2 and 32 kHz or via the embedded 32 kHz crystal oscillator cell
- ARM7TDMI 32-bit CPU
- Memory organization
  - Integrated 4 Mbit flash
  - 64 KByte on-chip RAM
  - 4 KByte on-chip boot ROM
  - Hold-acknowledge bus arbitration support
- HW support for all packet types
  - ACL: DM1, 3, 5 and DH1, 3, 5
  - SCO: HV1, 2, 3 and DV1
- Communication interfaces
  - Serial Synchronous Interface
  - Two enhanced 16550 UART's with 128 byte fifo depth
  - 12 Mbps USB interface
  - Fast master I2C bus interface
  - Multi slot PCM interface
  - 16 programmable GPIO
  - 2 external interrupts and various interrupt possibilities through other interfaces
- Ciphering support for up to 128-bit key
- Receiver Signal Strenght Indication (RSSI) support for power-controlled links
- Separate control for external power amplifier (PA) for class1 power support.
- Software support
  - Low level (up to HCI) stack or embedded stack with profiles
  - Support of UART and USB HCI transport layers.
- Idle and power down modes
  - Ultra low power in idle mode
  - Low standby current

Figure 1. Package

LFBGA120 (10x10x1.4mm)

Table 1. Order Codes

Part Number	Package	Temp. Range
STLC2415	LFBGA120	-40 to +85 °C

1.1 Applications Features

Typical applications in which the STLC2415 can be used are:

- Cable replacement
- Portable computers, PDA
- Modems
- Handheld data transfer devices
- Cameras
- Computer peripherals
- Other type of devices that require the wireless communication provided by Bluetooth®

2 DESCRIPTION

The STLC2415 from STMicroelectronics is a Bluetooth® baseband controller with integrated 4 Mbit flash memory. Together with a Bluetooth® Radio this product offers a compact and complete solution for short-range wireless connectivity. It incorporates all the lower layer functions of the Bluetooth® protocol.

The microcontroller allows the support of all data packets of Bluetooth® in addition to voice. The embedded controller can be used to run the Bluetooth® protocol and application layers if required. The software is located in the integrated flash memory.

3 QUICK REFERENCE DATA

3.1 Absolute Maximum Ratings

Operation of the device beyond these conditions is not guaranteed.
Sustained exposure to these limits will adversely affect device reliability

Table 2. Absolute Maximum Ratings

Symbol	Conditions	Min	Max	Unit
V_{DD}	Supply voltage baseband core	V_{SS} – 0.5	2.5	V
V_{DDF}	Supply voltage flash	V_{SS} – 0.5	2.5	V
V_{PP}	Fast Program Voltage	V_{SS} – 0.5	13	V
V_{DDIO}	Supply voltage baseband I/O		4	V
V_{DDQ}	Supply voltage flash I/O	V_{SS} – 0.5	2.5	V
V_{IN}	Input voltage on any digital pin (excluding FLASH input pins)	V_{SS} – 0.5	V_{DDIO} + 0.3	V
T_{amb}	Operating ambient temperature	-40	+85	°C
T_{stg}	Storage temperature	-55	+150	°C
T_{lead}	Lead temperature < 10s		+240	°C

3.2 Operating Ranges

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not implied.

Table 3. Operating Ranges

Symbol	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage baseband core and EMI pads	1.55	1.8	1.95	V
V_{DDF}	Supply voltage flash	1.55	1.8	1.95	V
V_{DDIO}	Supply voltage baseband I/O	2.7	3.3	3.6	V
V_{DDQ}	Supply voltage flash I/O ($V_{DDQ} \leq V_{DDF}$)	1.55	1.8	1.95	V
T_{amb}	Operating ambient temperature	-40		+85	°C

3.3 I/O Specifications

Depending on the interface, the I/O voltage is typical 1.8V (interface to the flash memory) or typical 3.3V (all the other interfaces). These I/Os comply to the EIA/JEDEC standard JESD8-B.

3.3.1 Specifications for 3.3V I/Os

Table 4. LVTTL DC Input Specification ($3V<V_{DDIO}<3.6V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{il}	Low level input voltage				0.8	V
V_{ih}	High level input voltage		2			V
V_{hyst}	Schmitt trigger hysteresis		0.4			V

Table 5. LVTTL DC Output Specification ($3V<V_{DDIO}<3.6V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ol}	Low level output voltage	I_{ol} = X mA			0.15	V
V_{oh}	High level output voltage	I_{oh} =-X mA	V_{DDIO}-0.15			V

Note: X is the source/sink current under worst case conditions according to the drive capability. (See table 8, pad information for value of X).

3.3.2 Specifications for 1.8V I/Os

Table 6. DC Input Specification (1.55V<V_{DD}<1.95V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{il}	Low level input voltage				0.35*V_{DD}	V
V_{ih}	High level input voltage		0.65*V_{DD}			V
V_{hyst}	Schmitt trigger hysteresis		0.2	0.3	0.5	V

Table 7. DC Output Specification (1.55V<V_{DD}<1.95V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ol}	Low level output voltage	I_{ol} = X mA			0.15	V
V_{oh}	High level output voltage	I_{oh} =-X mA	V_{DD}-0.15			V

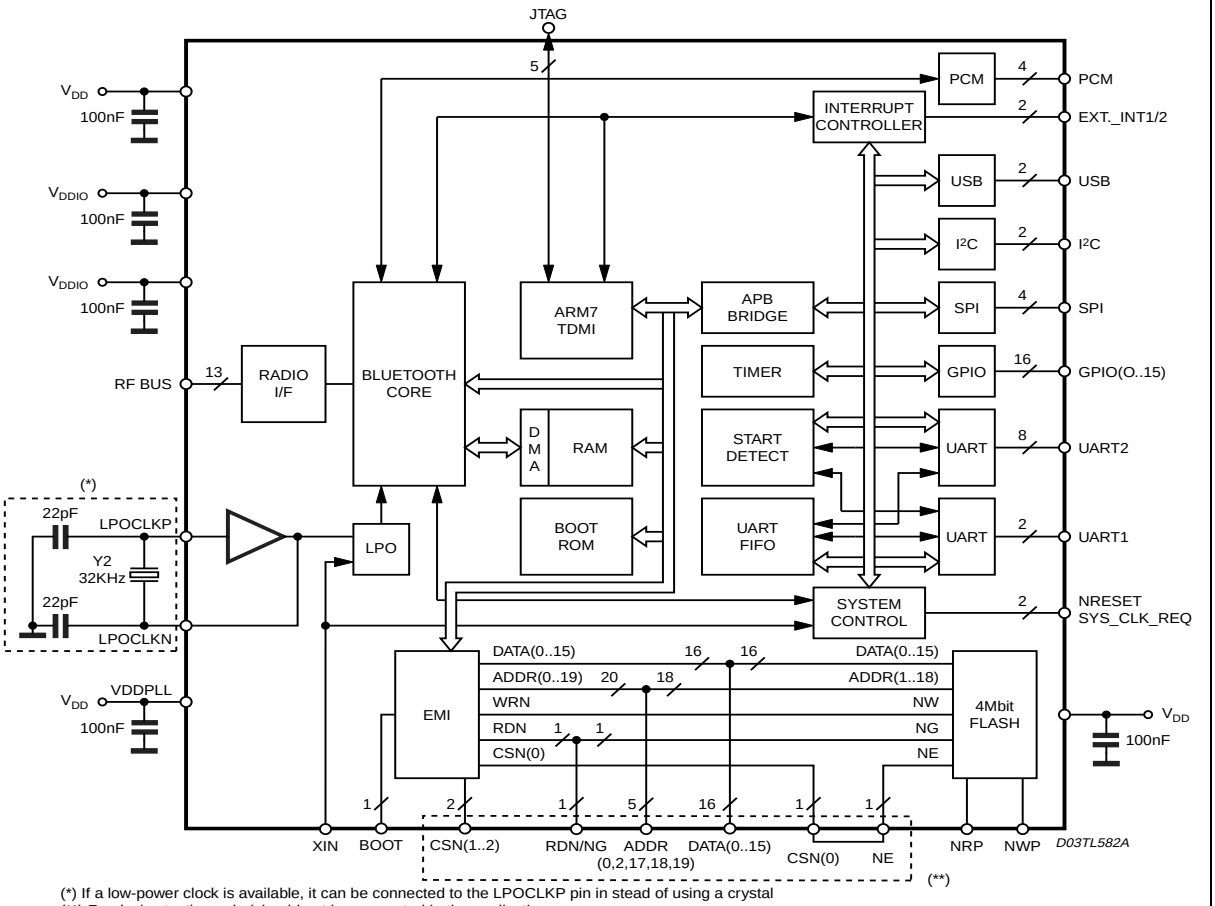
Note: X is the source/sink current under worst case conditions according to the drive capability. (See table 8, pad information for value of X).

3.4 Current Consumption

Table 8. Typical Power Consumption of the STLC2415 (V_{DD} = V_{DD} Flash = PLLV_{DD} = 1.8V, V_{DDIO} = 3.3V)

STLC2415 State	Core		IO	Unit
	Slave	Master		
Standby (no low power mode)	5.10	5.10	0.13	mA
Standby (low power mode enabled)	0.94	0.94	0.13	mA
ACL connection (no transmission)	7.60	6.99	0.13	mA
ACL connection (data transmission)	7.90	7.20	0.13	mA
SCO connection (no codec connected)	8.70	7.90	0.14	mA
Inquiry and Page scan (low power mode enabled)	127	n.a.	5	µA
Low Power mode (32 kHz crystal)	20	20	0	µA

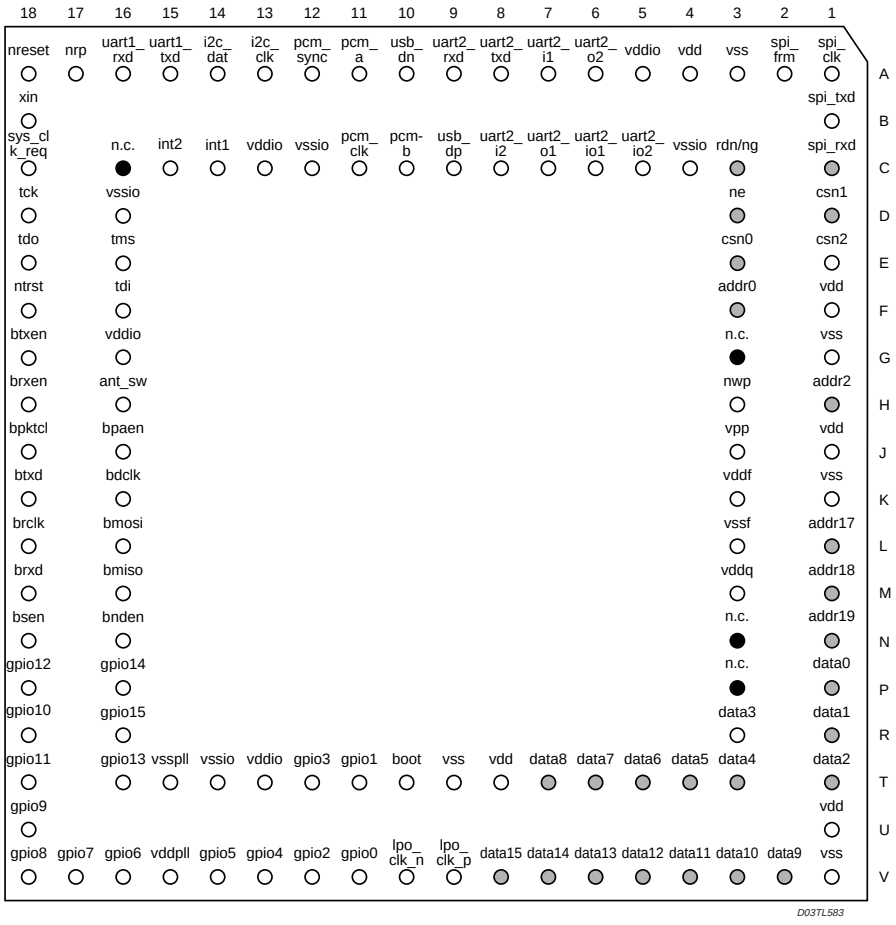
Figure 2. Block Diagram and Electrical Schematic



(*) If a low-power clock is available, it can be connected to the LPOCLKP pin in stead of using a crystal
(**) For device testing only (should not be connected in the application.

4 PINOUT

Figure 3. Pinout (Bottom view)



4.1 Pin Description and Asthe signment

Table 9 shows the pin list of STLC2415. There are 91 functional pins of which 25 are used for device testing only (should not be connected in the application) and 24 supply pins. The column "PU/PD" shows the pads implementing an internal weak pull-up/down, to fix value if the pin is left open. This can not replace an external pull-up/down.

The pads are grouped according to two different power supply values, as shown in column "VDD":

– V1 for 3.3 V typical 2.7 - 3.6 V range

– V2 for 1.8 V typical 1.55 - 1.95 V range

Finally the column "DIR" describes the pin directions:

– I for inputs

– O for outputs

– I/O for input/outputs

– O/t for tristate outputs

Table 9. Pin List

Name	Pin #	Description	DIR	PU/PD	VDD	PAD
Clock and test pins						
xin	B18	System clock	I		V1	CMOS, 3.3V TTL compatible schmitt trigger
nreset	A18	Reset	I			
nrp	A17	External flash reset	I		V2	
nwp	H3	Flash Write Protect	I		V2	CMOS 1.8V
sys_clk_req	C18	System clock request	I/O		V1	CMOS, 3.3V TTL compatible, 2mA tristate slew rate control
lpo_clk_p	V9	Low power oscillator + / Slow clock input	I	(1)	V2	
lpo_clk_n	V10	Low power oscillator -	O			
int1	C14	External Interrupt used also as external wakeup	I	(1)	V1	CMOS, 3.3V TTL compatible schmitt trigger
int2	C15	Second external interrupt	I	(1)		
boot	T10	Select external boot from EMI or internal from ROM	I	(1)	V2	CMOS 1.8V
SPI interface						
spi_frm	A2	Synchronous Serial Interface frame sync	I/O		V1	CMOS, 3.3V TTL compatible, 2mA tristate slew rate control schmitt trigger
spi_clk	A1	Synchronous Serial Interface clock	I/O			
spi_txd	B1	Synchronous Serial Interface transmit data	O/t		V1	CMOS, 3.3V TTL compatible, 2mA slew rate control
spi_rxd	C1	Synchronous Serial Interface receive data	I	(1)	V1	CMOS, 3.3V TTL compatible schmitt trigger
UART interface						
uart1_txd	A15	Uart1 transmit data	O/t		V1	CMOS, 3.3V TTL compatible, 2mA slew rate control
uart1_rxd	A16	Uart1 receive data	I	(2)	V1	CMOS, 3.3V TTL compatible schmitt trigger
uart2_o1	C7	Uart2 modem output	O		V1	CMOS, 3.3V TTL compatible, 2mA slew rate control
uart2_o2	A6	Uart2 modem output	O/t		V1	CMOS, 3.3V TTL compatible, 2mA slew rate control
uart2_i1	A7	Uart2 modem input	I	(2)	V1	CMOS, 3.3V TTL compatible
uart2_i2	C8	Uart2 modem input	I	(2)	V1	
uart2_io1	C6	Uart2 modem input/output	I/O	(2)	V1	CMOS, 3.3V TTL compatible, 2mA tristate slew rate control
uart2_io2	C5	Uart2 modem input/output	I/O	(2)	V1	

Table 9. Pin List (continued)

Name	Pin #	Description	DIR	PU/PD	VDD	PAD
uart2_txd	A8	Uart2 transmit data	O/t		V1	CMOS, 3.3V TTL compatible, 2mA slew rate control
uart2_rxd	A9	Uart2 receive data	I	(2)	V1	CMOS, 3.3V TTL compatible
I2C interface						
i2c_dat	A14	I2C data pin	I/O	(3)	V1	CMOS, 3.3V TTL compatible, 2mA tristate slew rate control
i2c_clk	A13	I2C clock pin	I/O	(3)	V1	
USB interface						
usb_dn	A10	USB - pin	I/O	(1)	V1	
usb_dp	C9	USB + pin	I/O	(1)	V1	
GPIO interface						
gpio0	V11	Gpio port 0	I/O	PU	V1	CMOS, 3.3V TTL compatible, 4mA tristate slew rate control
gpio1	T11	Gpio port 1	I/O	PU		
gpio2	V12	Gpio port 2	I/O	PU		
gpio3	T12	Gpio port 3	I/O	PU	V1	CMOS, 3.3V TTL compatible, 4mA tristate slew rate control schmitt trigger
gpio4	V13	Gpio port 4	I/O	PU	V1	CMOS, 3.3V TTL compatible, 4mA tristate slew rate control
gpio5	V14	Gpio port 5	I/O	PU		
gpio6	V16	Gpio port 6	I/O	PU		
gpio7	V17	Gpio port 7	I/O	PU		
gpio8	V18	Gpio port 8	I/O	PU	V1	CMOS, 3.3V TTL compatible, 2mA tristate slew rate control
gpio9	U18	Gpio port 9	I/O	PU		
gpio10	R18	Gpio port 10	I/O	PU		
gpio11	T18	Gpio port 11	I/O	PU		
gpio12	P18	Gpio port 12	I/O	PU		
gpio13	T16	Gpio port 13	I/O	PU		
gpio14	P16	Gpio port 14	I/O	PU		
gpio15	R16	Gpio port 15	I/O	PU		
JTAG interface						
ntrst	F18	JTAG pin	I	PD	V1	CMOS, 3.3V TTL compatible
tck	D18	JTAG pin	I	(1)	V1	CMOS, 3.3V TTL compatible schmitt trigger
tms	E16	JTAG pin	I	PU	V1	CMOS, 3.3V TTL compatible
tdi	F16	JTAG pin	I	PU		

Table 9. Pin List (continued)

Name	Pin #	Description	DIR	PU/PD	VDD	PAD
tdo	E18	JTAG pin (should be left open)	O/t		V1	CMOS, 3.3V TTL compatible, 2mA slew rate control
PCM interface						
pcm_a	A11	PCM data	I/O	PD	V1	CMOS, 3.3V TTL compatible, 2mA tristate slew rate control
pcm_b	C10	PCM data	I/O	PD		
pcm_sync	A12	PCM 8kHz sync	I/O	PD		
pcm_clk	C11	PCM clock	I/O	PD	V1	CMOS, 3.3V TTL compatible, 2mA tristate slew rate control schmitt trigger
Radio interface						
brclk	L18	Transmit clock	I	(1)	V1	CMOS, 3.3V TTL compatible schmitt trigger
brxd	M18	Receive data	I			
bmiso	M16	RF serial interface input data	I	(1)	V1	CMOS, 3.3V TTL compatible
bnden	N16	RF serial interface control	O		V1	CMOS, 3.3V TTL compatible, 2mA slew rate control
bmosi	L16	RF serial interface output data	O			
bdclk	K16	RF serial interface clock	O			
btxd	K18	Transmit data	O			
bsen	N18	Synthesizer ON	O			
bpaen	J16	Open PLL	O			
brxen	H18	Receive ON	O			
btxen	G18	Transmit ON	O			
bpktctl	J18	Packet ON	O			
ant_sw	H16	Antenna switch	O		V1	CMOS, 3.3V TTL compatible, 8mA slew rate control

(1) Should be strapped to vssio if not used
(2) Should be strapped to vddio if not used
(3) Must have a 10 kOhm pull-up.

Table 9. Pin List (continued)

Name	Pin #	Description
Power Supply		
vsspll	T15	PLL ground
vddpll	V15	1.8V supply for PLL
vdd	A4	1.8V Digital supply
vdd	F1	1.8V Digital supply
vdd	J1	1.8V Digital supply
vdd	U1	1.8V Digital supply
vdd	T8	1.8V Digital supply
vddf	K3	1.8V Digital supply Flash
vddq	M3	1.8V I/O's supply Flash
vpp	J3	12V fast program supply Flash
vddio	C13	3.3V I/O's supply
vddio	A5	3.3V I/O's supply
vddio	T13	3.3V I/O's supply
vddio	G16	3.3V I/O's supply
vss	A3	Digital ground
vss	G1	Digital ground
vss	K1	Digital ground
vss	V1	Digital ground
vss	T9	Digital ground
vssf	L3	Digital ground Flash
vssio	C12	I/O's ground
vssio	C4	I/O's ground
vssio	T14	I/O's ground
vssio	D16	I/O's ground

Table 9. Pin List (continued)

Name	Pin #	Description	DIR	PU/PD	VDD	PAD
To be connected together on the PCB's top layer						
ne	D3	Flash chip enable	I			
csn0	E3	External chip select bank 0	O			
Test Only (Do NOT connect)						
rdn/ng	C3	External read	O		V2	CMOS 1.8V 4mA slew rate control
csn1	D1	External chip select bank 1	O			
csn2	E1	External chip select bank 2	O			
addr0	F3	External address bit 0	O			
addr2	H1	External address bit 2	O			
addr17	L1	External address bit 17	O			
addr18	M1	External address bit 18	O			
addr19	N1	External address bit 19	O			
data0	P1	External data bit 0	I/O	PD		
data1	R1	External data bit 1	I/O	PD		
data2	T1	External data bit 2	I/O	PD		
data3	R3	External data bit 3	I/O	PD		
data4	T3	External data bit 4	I/O	PD		
data5	T4	External data bit 5	I/O	PD		
data6	T5	External data bit 6	I/O	PD	V2	CMOS 1.8V 4mA slew rate control
data7	T6	External data bit 7	I/O	PD		
data8	T7	External data bit 8	I/O	PD		
data9	V2	External data bit 9	I/O	PD		
data10	V3	External data bit 10	I/O	PD		
data11	V4	External data bit 11	I/O	PD		
data12	V5	External data bit 12	I/O	PD		
data13	V6	External data bit 13	I/O	PD		
data14	V7	External data bit 14	I/O	PD		
data15	V8	External data bit 15	I/O	PD		
Not Connected						
n.c.	C16, G3, N3, P3	Not Connected				

5 FUNCTIONAL DESCRIPTION

5.1 Baseband

5.1.1 Overview

The baseband is based on Ericsson Technology Licensing Baseband Core (EBC) and it is fully compliant with the Bluetooth® specification 1.1:

- Point to multipoint (up to 7 Slaves)
- Asynchronous Connection Less (ACL) link support giving data rates up to 721 kbps.
- Synchronous Connection Oriented (SCO) link with support for 1 voice channel over the air interface.
- HW support for all packet types:
  - ACL: DM1, 3, 5 and DH1, 3, 5
  - SCO: HV1, 2, 3, and DV1.
- Support for three PCM channels in the PCM interface .
- Architecture gives ultra-low power consumption.
- Ciphering support up to 128 bits key, configurable by software.
- Receiver Signal Strenght Indication (RSSI) support for power-controlled links
- Flexible voice formats to Host and over air (CVSD, PCM 16/8-bit, A-law, µ-law)
- High quality filtering of voice packets enabling excellent audio quality.
- Scatternet support, communication between two simultaneously running piconets.
- Full Bluetooth® software stack available.
- Low level link controller.
- Specific external power amplifier (PA) control for class1 support
- Extended wake-up and interrupt functionality for HID support

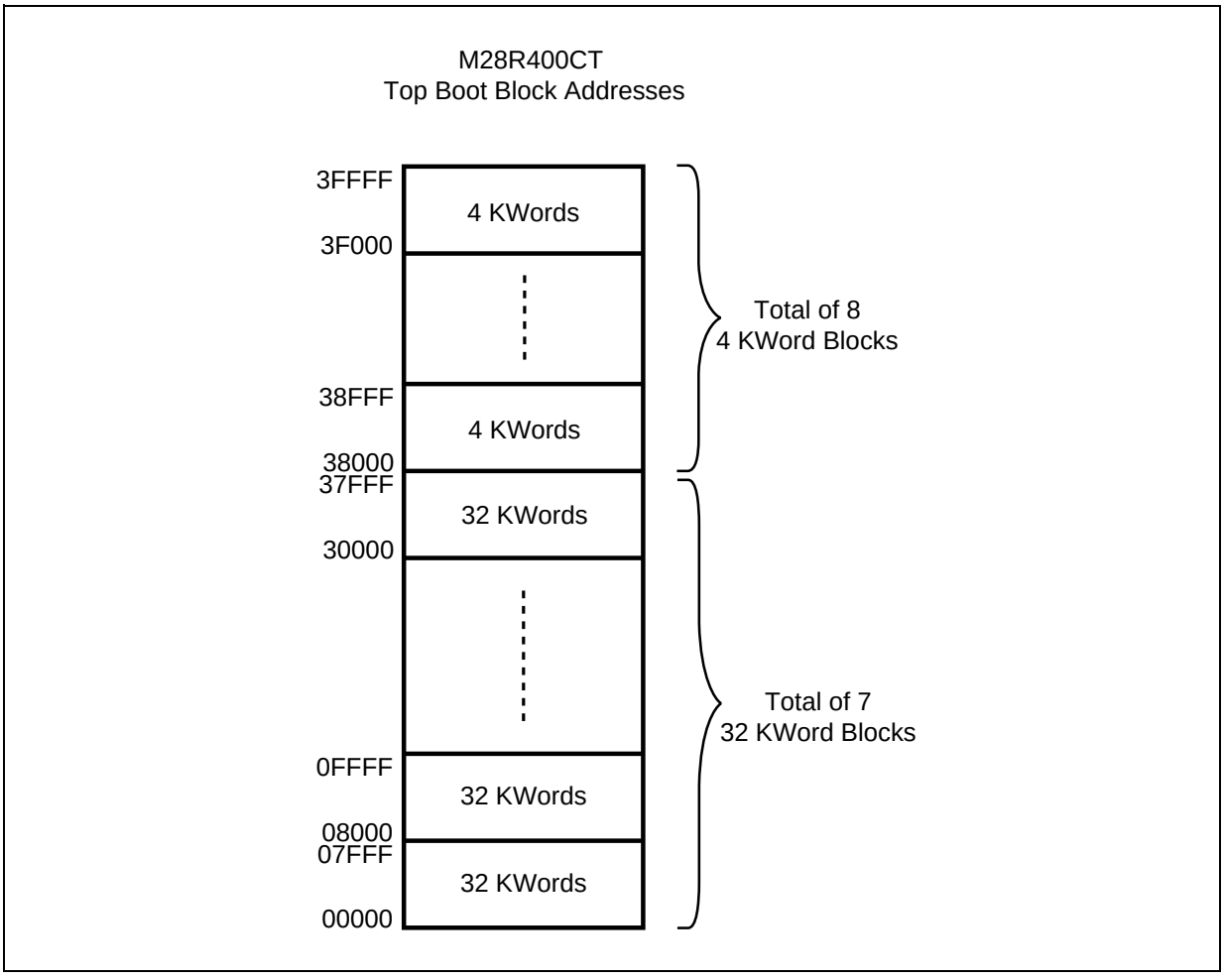
5.2 Processor and Memory

- ARM7TDMI
- 64 Kbyte of static RAM.
- 4 Kbyte of metal programmable ROM
- Extension of the ARM Bus to access the program in the integrated 4 MBit FLASH

5.3 Integrated Flash Memory

- 4 Mbit size
- 8 parameter blocks of 4 Kword (top configuration)
- 7 main blocks of 32 Kword
- 120 ns access time
- See datasheet of standalone product M28R400CT for more detailed information.

Figure 4. Block Addresses



5.3.1 Flash Signal Descriptions

– **Write Protect (nwp)**
Write protect is an input that gives an additional hardware protection for each block. When Write Protect is ≤ 0.4V the Lock-Down is enabled and the protection status of the flash blocks cannot be changed. When Write Protect is ≥ (vddq - 0.4V), the Lock-Down is disabled and the flash memory blocks can be locked or unlocked.

– **Reset (nrp)**
The Reset input provides a hardware reset of the memory. When reset is ≤ 0.4V, the memory is in reset mode: the outputs are high impedant and the current consumption is minimized. After Reset all blocks are in Locked state. When Reset is ≥ (vddq - 0.4V), the device is in normal operation. Exiting reset mode the device enters read array mode, but a negative transition of Chip Enable or a change of the address is required to ensure valid data outputs.

– **Vdd Supply Voltage (vddf)**
Vdd provides the power supply to the internal core of the flash memory device. It is the main power supply for all operations (Read, Program and Erase)

– **Vddq Supply Voltage (vddq)**
Vddq provides the power supply to the I/O pins and enables all Outputs to be powered independently from Vddf. Vddq can be tied to Vddf or can use separate supply.

– **Vpp Program Supply Voltage (vpp)**
Vpp is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin. The supply voltage Vddf and the program supply voltage Vpp can be applied in any order.
If Vpp is kept in a low voltage range (0V to 3.6V) Vpp is seen as a control input. In this case a voltage lower than 1V gives protection agains program or block erase, while 1.65V<Vpp<3.6V enables these functions. Vpp is only sampled at the beginning of a program or block erase; a change in its value after the operation has started does not have any effect and program or erase opereations continue.
If Vpp is in the range 11.4V to 12.6V it acts as a power supply pin. In this condition Vpp must be stable until the Program/Erase algorithm is completed.

– **Vssf Flash Ground (vssf)**
Vssf is the reference for all voltage measurements.

– **Address Inputs (Addr(1-18)/Addr(0-19))*, Data Input/Output (Data(0-15)/Data(0-15))*, Chip Enable (ne/csn(0))*, Ouput Enable (ng/rdn)*, Write Enable (nw/wrn)*** are connected and controlled by the Bluetooth® baseband controller.

*(flash memory signals / baseband controller signals)

6 GENERAL SPECIFICATION

6.1 System Clock

The STLC2415 works with a single clock provided on the XIN pin. The value of this external clock should be 13MHz ±20ppm (overall).

6.1.1 Slow Clock

The slow clock is used by the baseband as reference clock during the low power modes. Compared to the 13MHz clock, the slow clock only requires an accuracy of ±250ppm (overall).
Several options are foreseen in order to adjust the STLC2415 behaviour according to the features of the radio used:

– if the system clock (e.g. 13MHz) is not provided at all times (power consumption saving) and no slow clock is provided by the system, a 32 kHz crystal must be used by the STLC2415 (default mode).
– if the system clock (e.g. 13MHz) is not provided at all times (power consumption saving) and the system provides a slow clock at 32kHz or 3.2kHz, this signal is simply connected to the STLC2415 (lpo_clk_p).
– if the system clock (e.g. 13MHz) is provided at all times, the STLC2415 generates from the 13MHz reference clock an internal 32kHz clock. This mode is not an optimized mode for power consumption.

6.2 Boot Procedure

The boot code instructions are the first that ARM7TDMI executes after an HW reset. All the internal device's registers are set to their default value.

There are 2 types of boot:

– Flash boot.

When boot pin is set to `1` (connected to VDD), the STLC2415 boots on its flash memory.

– UART download boot from ROM.

When boot pin is set to `0` (connected to GND), the STLC2415 boots on its internal ROM (needed to download the new firmware in the flash). When booting on the internal ROM, the STLC2415 will monitor the UART interface for approximately 1.4 second. If there is no request for code downloading during this period, the ROM jumps to flash.

6.3 Clock Detection

The STLC2415 has an automatic slow clock frequency detection (32kHz, 3.2kHz or none).

6.4 Master Reset

When the device's reset is held active (NRESET is low), UART1_TXD and UART2_TXD are set to input state. When the NRESET returns high, the device starts to boot.

Remark: The device should be held in active reset for minimum 20ms in order to guarantee a complete reset of the device.

6.5 Interrupts/Wake-up

The external pins int1 and int2, and up to 8 GPIOs can be used both as external interrupt source and as wake-up source. In addition the chip can be woken-up by USB, UART1_RXD, UART2_RXD.

7 INTERFACES

7.1 UART Interface

The chip contains two enhanced (128 byte transmit FIFO and 128 byte receive FIFO, sleep mode, 127 Rx and 128 Tx interrupt tresholds) UARTs, named UART1 and UART2, compatible with the standard M16550 UART.

For UART1, only Rx and Tx signals are available (used for debug purposes).

UART2 features:

- standard HCI UART transport layer:
  - all HCI commands as described in the Bluetooth® specification 1.1
  - ST specific HCI command (check STLC2415 Software Interface document for more information)
- RXD, TXD, CTS, RTS on permanent external pins
- 128-byte FIFOs, for transmit and for receive
- Default configuration: 57.600 kbps
- Specific HCI command to change to the following baud rates:

Table 10. List of Supported Baud Rates

Baud rate		
–	**57.6 kbps (default)**	4800
921.6k	38.4 k	2400
460.8 k	28.8 k	1800
230.4 k	19.2 k	1200
153.6 k	14.4 k	900
115.2 k	9600	600
76.8 k	7200	300

7.2 Synchronous Serial Interface

The Synchronous Serial Interface (SSI) (or the Synchronous Peripheral Interface (SPI)) is a flexible module supporting full-duplex and half-duplex synchronous communications with external devices in Master and Slave mode. It allows the STLC2415 to communicate with peripheral devices.
The Synchronous Serial Interface is also capable of inter processor communications in a multiple-master system. This interface is flexible enough to interface directly with numerous standard product peripherals. This Synchronous Serial Interface peripheral features:

- full duplex, four-wire synchronous transfers.
- Microwire half duplex transfer using 8-bit control message
- programmable clock polarity and phase.
- transmit data pin tri state able when not transmitting
- Master or Slave operation
- Programmable clock bit rate up to XIN/4
- Programmable data frame from 4 bits to 16 bits.
- Independent transmit and receive 16 words FIFO.
- Internal loopback

7.3 I2C Interface

Used to access I2C peripherals.

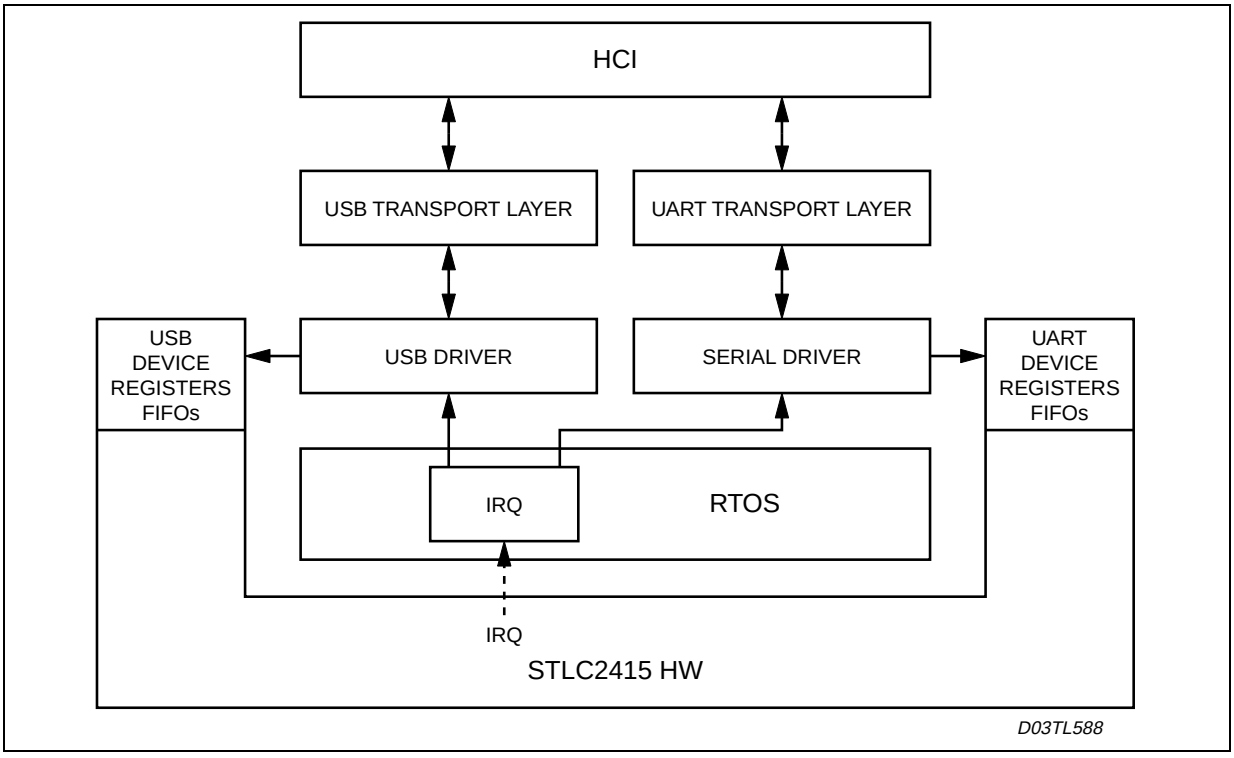
The interface is a fast master I2C; it has full control of the interface at all times. I2C slave functionality is not supported.

7.4 USB Interface

A USB device interface compliant to USB specification v1.1 is connected to the ARM processor. This allows the chip to be connected to a Universal Serial Bus that can transmit data and/or voice through the internal USB transceiver.

Figure 5 gives an overview of the main components needed for supporting the USB interface, as specified in the Bluetooth® Core Specification (Part H:2). For clarity, the serial interface (including the UART Transport Layer) is also shown.

Figure 5. USB Interface



The USB device registers and FIFOs are memory mapped. The USB Driver will use these registers to access the USB interface. The equivalent exists for the HCI communication over UART.

For transmission to the host, the USB & Serial Drivers interface with the HW via a set of registers and FIFOs, while in the other direction, the hardware may trigger the Drivers through a set of interrupts (identified by the RTOS, and directed to the appropriate Driver routines).

7.5 JTAG Interface

The JTAG interface is compliant with the JTAG IEEE Std 1149.1. Its allows both the boundary scan of the digital pins and the debug of the ARM7TDMI application when connected with the standard ARM7 development tools.

7.6 RF Interface

The STLC2415 radio interface is compatible to BlueRF (unidirectional RxMode2 for data and unidirectional serial interface for control).

7.7 PCM Voice Interface

The PCM interface is a direct PCM interface to connect to a standard CODEC (e.g. STw5093 or STw5094)

including internal decimator and interpolator filters. The data can be linear PCM (13-16bit), µ-Law (8bit) or A-Law (8bit). By default the codec interface is configured as master. The encoding on the air interface is programmable to be CVSD, A-Law or µ-Law.

The PCM block is able to manage the PCM bus with up to 3 timeslots.

In master mode, PCM clock and data can operate at 2 MHz or at 2.048 MHz to allow interfacing of standard codecs.

The four signals of the PCM interface are:

– PCM_CLK : PCM clock

– PCM_SYNC : PCM 8kHz sync

– PCM_A : PCM data

– PCM_B : PCM data

Directions of PCM_A and PCM_B are software configurable.

Figure 6. PCM (A-law, µ-law) Standard Mode

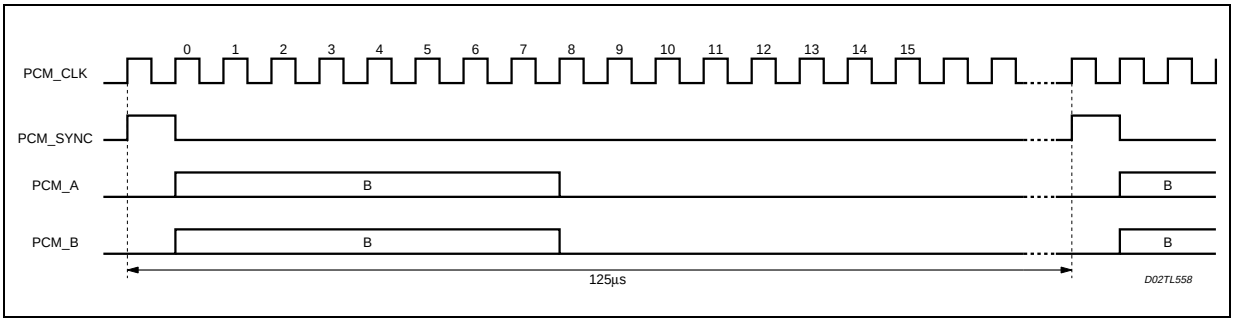


Figure 7. Linear Mode

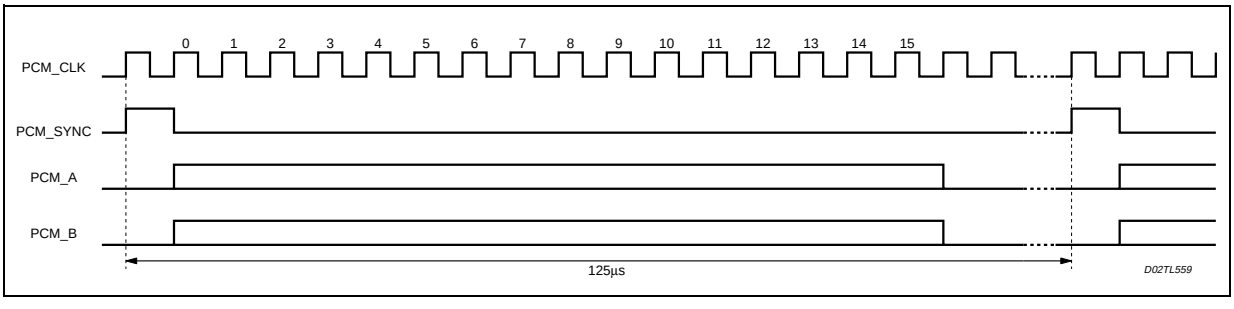
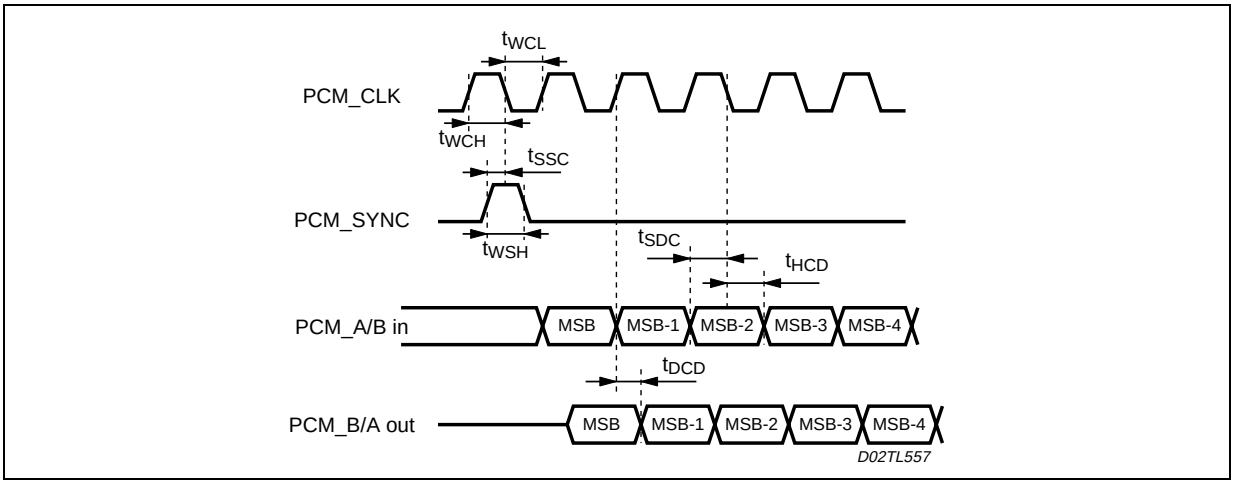


Table 11. PCM Interface Timing.

Symbol	Description	Min	Typ	Max	Unit
PCM Interface					
F_{pcm_clk}	Frequency of PCM_CLK (master)	-	2048		kHz
F_{pcm_sync}	Frequency of PCM_SYNC		8		kHz
t_{WCH}	High period of PCM_CLK	200			ns
t_{WCL}	Low period of PCM_CLK	200			ns
t_{WSH}	High period of PCM_SYNC	200			ns
t_{SSC}	Setup time, PCM_SYNC high to PCM_CLK low	100			ns
t_{SDC}	Setup time, PCM_A/B input valid to PCM_CLK low	100			ns
t_{HCD}	Hold time, PCM_CLK low to PCM_A/B input invalid	100			ns
t_{DCD}	Delay time, PCM_CLK high to PCM_A/B output valid			150	ns

Figure 8. PCM Interface Timing



8 HCI UART TRANSPORT LAYER

The UART Transport Layer has been specified by the Bluetooth® SIG (Part H:3), and allows HCI level communication between a host controller (STLC2415) and a host (e.g. PC), via a RS232 interface.
The objective of this HCI UART Transport Layer is to make it possible to use the Bluetooth® HCI over a serial interface between two UARTs on the same PCB. The HCI UART Transport Layer assumes that the UART communication is free from line errors.

8.1 UART Settings

The HCI UART Transport Layer uses the following settings:

– Baud rate: Configurable (Default baud rate: 57.600 kbps)

– Number of data bits: 8

– Parity bit: no parity

– Stop bit: 1 stop bit

– Flow control: RTS/CTS

– Flow-off response time: 3 ms

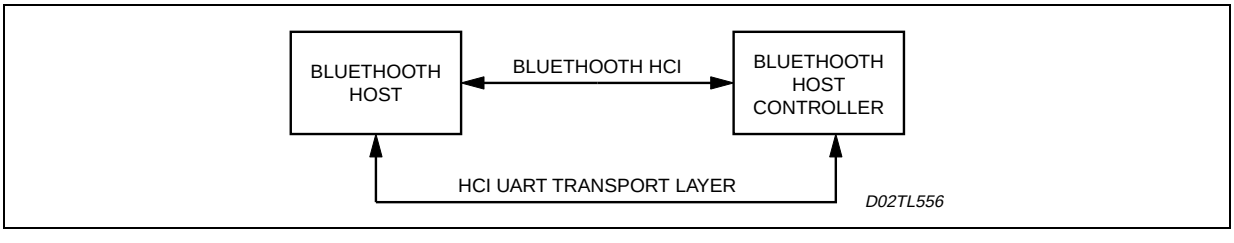
Flow control with RTS/CTS is used to prevent temporary UART buffer overrun. It should not be used for flow control of HCI, since HCI has its own flow control mechanisms for HCI commands, HCI events and HCI data.

If CTS is 1, then the Host/Host Controller is allowed to send.

If CTS is 0, then the Host/Host Controller is not allowed to send.

The flow-off response time defines the maximum time from setting RTS to 0 until the byte flow actually stops. The signals should be connected in a null-modem fashion; i.e. the local TXD should be connected to the remote RXD and the local RTS should be connected to the remote CTS and vice versa.

Figure 9. UART Transport Layer



9 HCI USB TRANSPORT LAYER

The USB Transport Layer has been specified by the Bluetooth® SIG (Part H:2), and allows HCI level communication between a host controller (STLC2415) and a host (e.g. PC), via a USB interface. The USB Transport Layer is completely implemented in SW. It accepts HCI messages from the HCI Layer, prepares it for transmission over a USB bus, and sends it to the USB Driver. It reassembles the HCI messages from USB data received from the USB Driver, and sends these messages to the HCI Layer. The Transport Layer does not interprete the contents (payload) of the HCI messages; it only examines the header.

10 POWER CLASS1 SUPPORT

The chip can control an external power amplifier (PA). Several signals are duplicated on GPIOs for this purpose in order to avoid digital/analog noise loops in the radio.

The Class1_En register enables the alternate functions of GPIO[15:6] to generate the signals for driving an external PA in a Bluetooth® power class1 application.

Every bit enables a dedicated signal on a GPIO pin, as described in table 12.

Table 12. Power Class 1 Functionality

Class1_En bit	involved GPIO	description (when class1_En bit = '1')
rxon	gpio[6]	outputs a copy of rx_on pin to switch LNA/RF switch on/off
not rxon	gpio[7]	outputs an inverted copy of rx_on pin to switch LNA/RF switch on/off
PA0	gpio[8]	Bit 0 of the PA value for the current connection
PA1	gpio[9]	Bit 1 of the PA value for the current connection
PA2	gpio[10]	Bit 2 of the PA value for the current connection
PA3	gpio[11]	Bit 3 of the PA value for the current connection
PA4	gpio[12]	Bit 4 of the PA value for the current connection
PA5	gpio[13]	Bit 5 of the PA value for the current connection
PA6	gpio[14]	Bit 6 of the PA value for the current connection
PA7	gpio[15]	Bit 7 of the PA value for the current connection

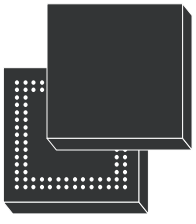
rx_on is the same as the rx_on output pin. Not rx_on is the inverted signal, in order to save components on the application board.

PA7 to PA0 are the power amplifier control lines. They are managed, on a connection basis, by the baseband core. The Power Level programmed for a certain Bluetooth® connection is manged by the firmware, as specified in the Bluetooth® SIG spec.

Figure 10. LFBGA120 (Low Fne Ball Grid Array) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.40			0.055
A1	0.20			0.008		
A2		1			0.039	
b	0.25	0.30	0.35	0.010	0.012	0.014
D	9.90	10.00	10.10	0.390	0.394	0.398
D1		8.50			0.335	
D2		6.50			0.256	
E	9.90	10.00	10.10	0.390	0.394	0.398
E1		8.50			0.335	
E2		6.50			0.256	
eD	0.50 basic			0.020 basic		
eE	0.50 basic			0.020 basic		
FD		0.75			0.029	
FE		0.75			0.029	
mD	18					
mE	18					
n	120 balls					
SE	0.25 basic			0.0098 basic		
SD	0.25 basic			0.0098 basic		
Tolerance						
aaa	0.15			0.006		
bbb	0.10			0.0039		
ddd	0.08			0.0031		
eee	0.15			0.006		
fff	0.05			0.002		

OUTLINE AND MECHANICAL DATA



Body: 10 x 10 x 1.4mm

LFBGA120
Low Fine Ball Grid Array

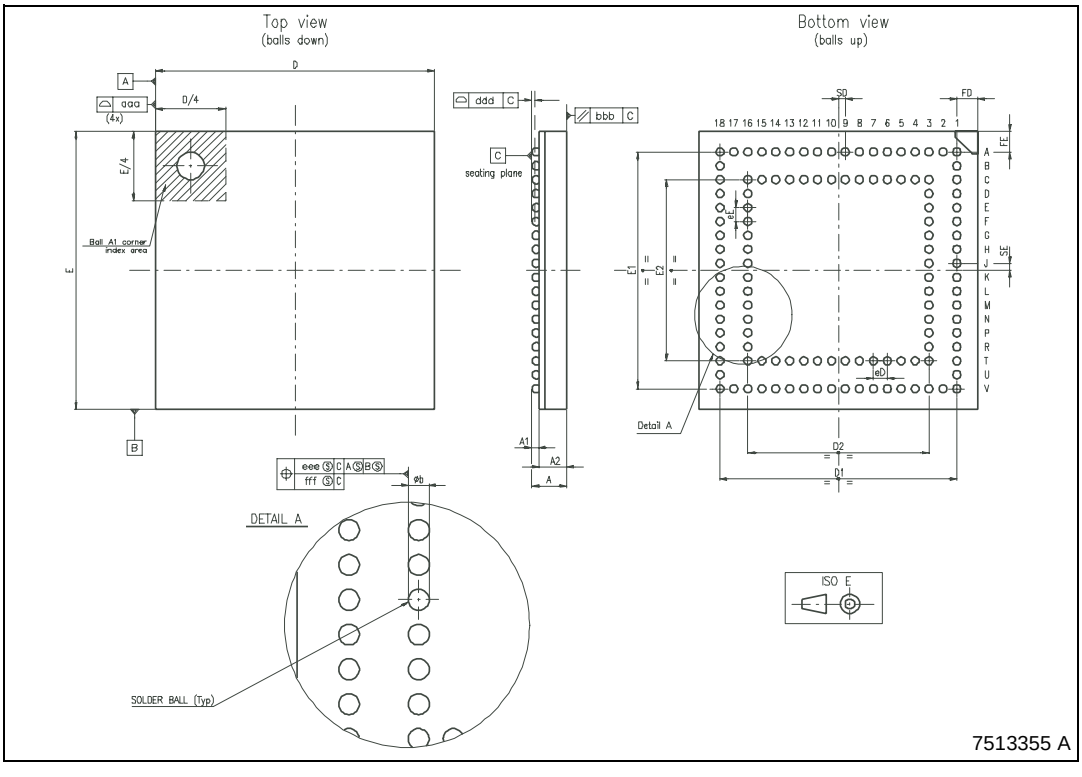


Table 13. Revision History

Date	Revision	Description of Changes
August 2004	1.1	First Issue in EDOCS DMS.
September 2004	2	Editorial corrections. Clock support added in section 1. Section 2 corrected. Modified the figures 2 and 3. Modified the tables 5, 7 and 8. 'To be connected' added in table 9. Section 5.3.1 modified. Section 6.2 corrected. Section 6.5 modified. Section 7.3 updated and figure removed.