



STS9NH3LL

N-channel 30V - 0.018Ω - 9A - SO-8
Low gate charge STripFET™ III Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STS9NH3LL	30V	0.022Ω	9A

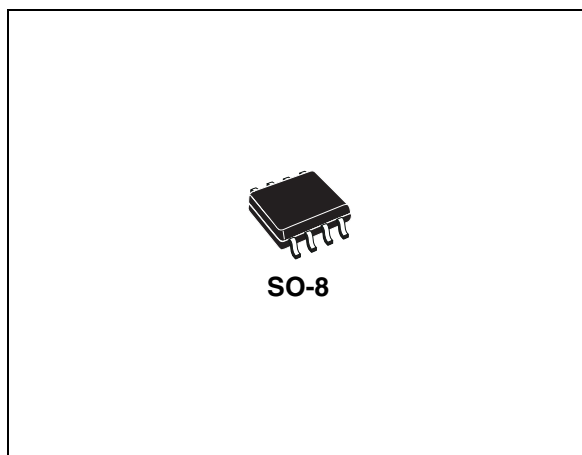
- Optimal R_{DS(on)} x Q_g trade-off @ 4.5V
- Conduction losses reduced
- Switching losses reduced

Description

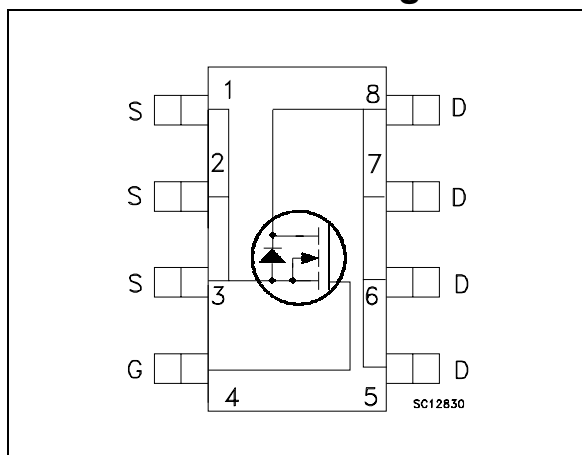
This application specific Power MOSFET is the third generation of STMicroelectronics unique “single feature size™” strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STS9NH3LL	S9NH3LL	SO-8	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate-source voltage	± 16	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	9	A
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	36	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	2.5	W
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4 board, 2oz Cu ($t < 10\text{sec.}$)

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating @ } 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 16V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 4.5A$ $V_{GS} = 4.5V, I_D = 4.5A$		0.018 0.020	0.022 0.025	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10V, I_D = 4.5A$		8.5		S
C_{iss}	Input capacitance	$V_{DS} = 25V, f = 1MHz, V_{GS} = 0$		857		pF
C_{oss}	Output capacitance			147		pF
C_{rss}	Reverse transfer capacitance			20		pF
Q_g	Total gate charge	$V_{DD} = 15V, I_D = 9A$		7.0	10	nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5V,$		2.5		nC
Q_{gd}	Gate-drain charge	(see Figure 14)		2.3		nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=15V$, $I_D=4.5A$, $R_G=4.7\Omega$, $V_{GS}=4.5V$ (see Figure 13)		12 14.5		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=15V$, $I_D=4.5A$, $R_G=4.7\Omega$, $V_{GS}=4.5V$ (see Figure 13)		23 8		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				9 36	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=4.5A$, $V_{GS}=0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=9A$, $di/dt=100A/\mu s$, $V_{DD}=15V$, $T_j=150^\circ C$ (see Figure 18)		15 5.7 0.76		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

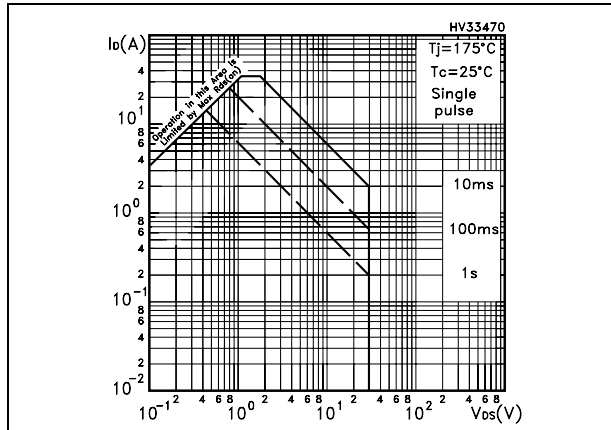


Figure 2. Thermal impedance

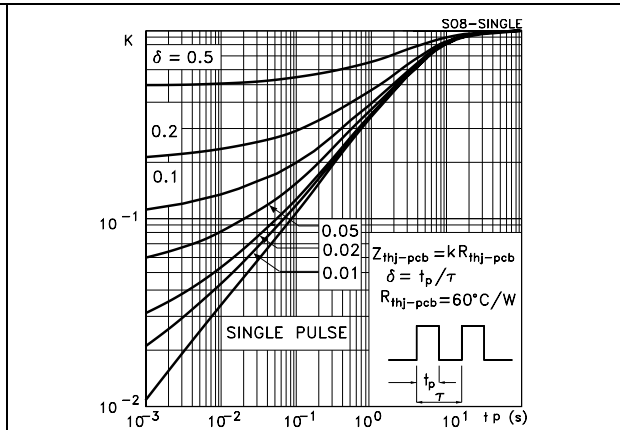


Figure 3. Output characteristics

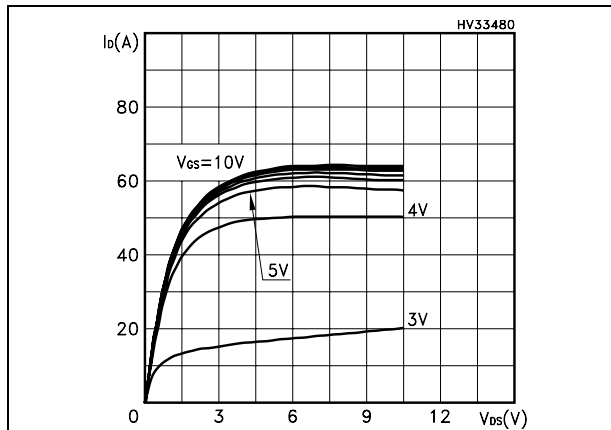


Figure 4. Transfer characteristics

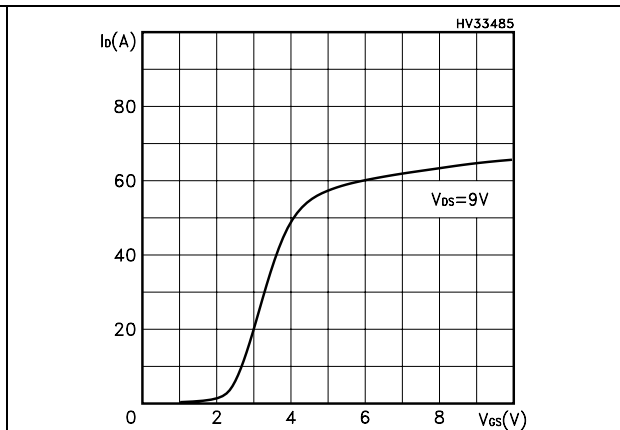


Figure 5. Transconductance

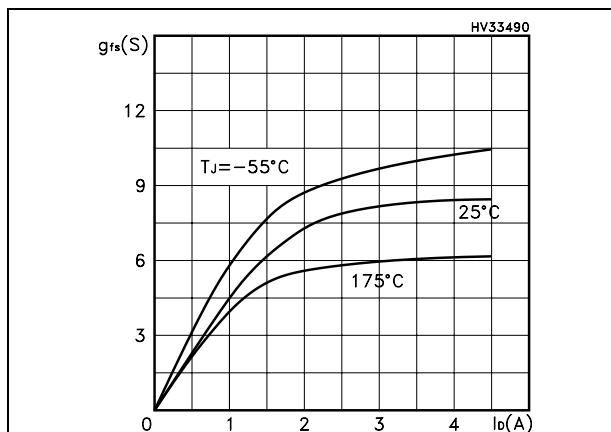


Figure 6. Static drain-source on resistance

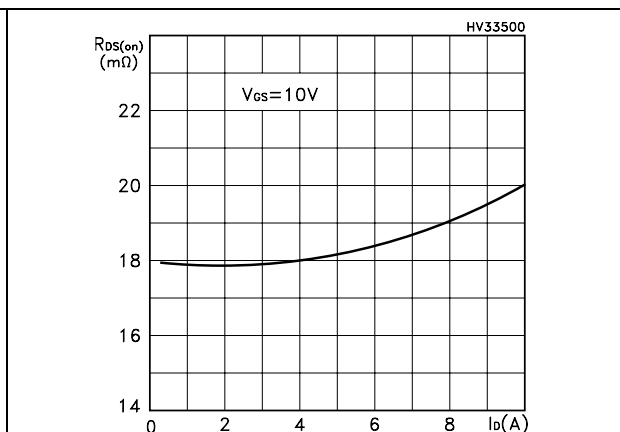


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

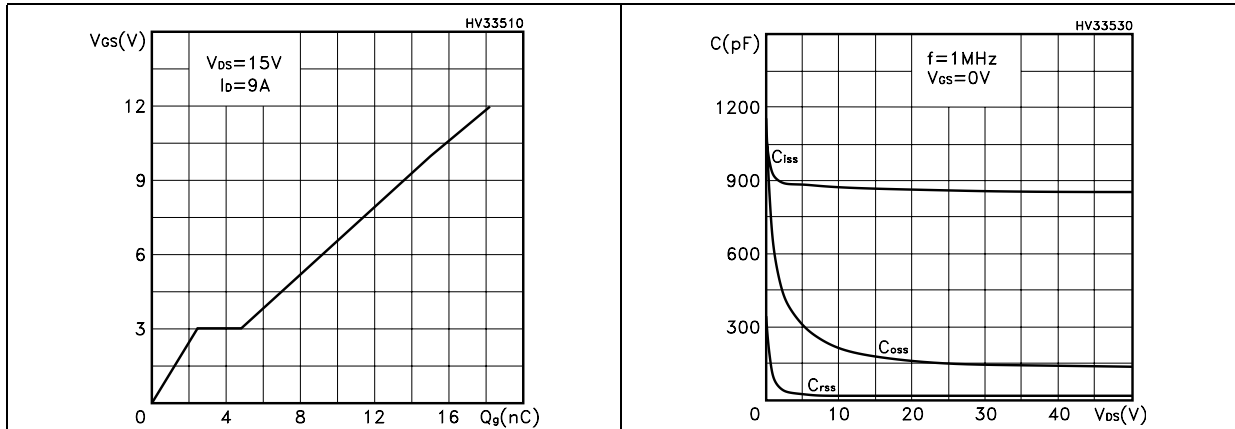


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

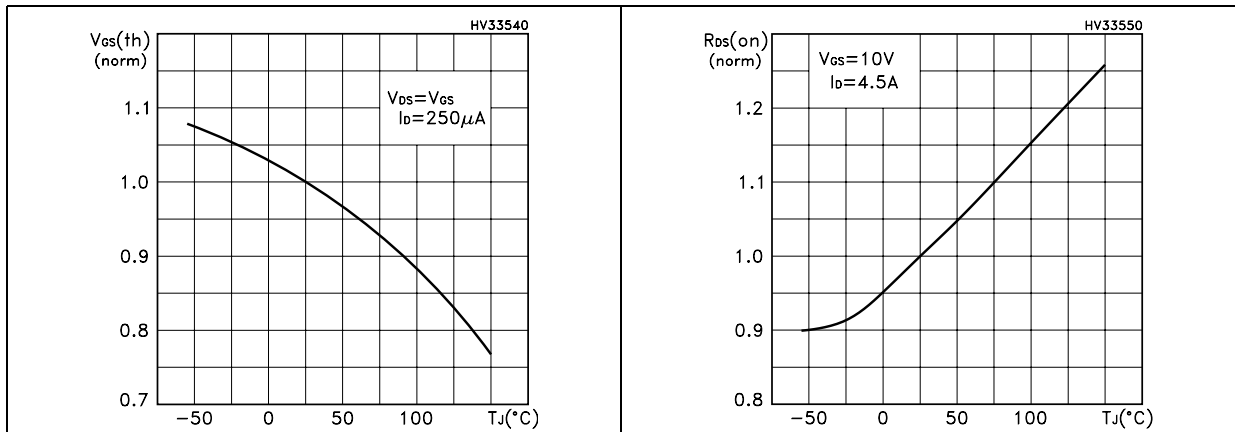
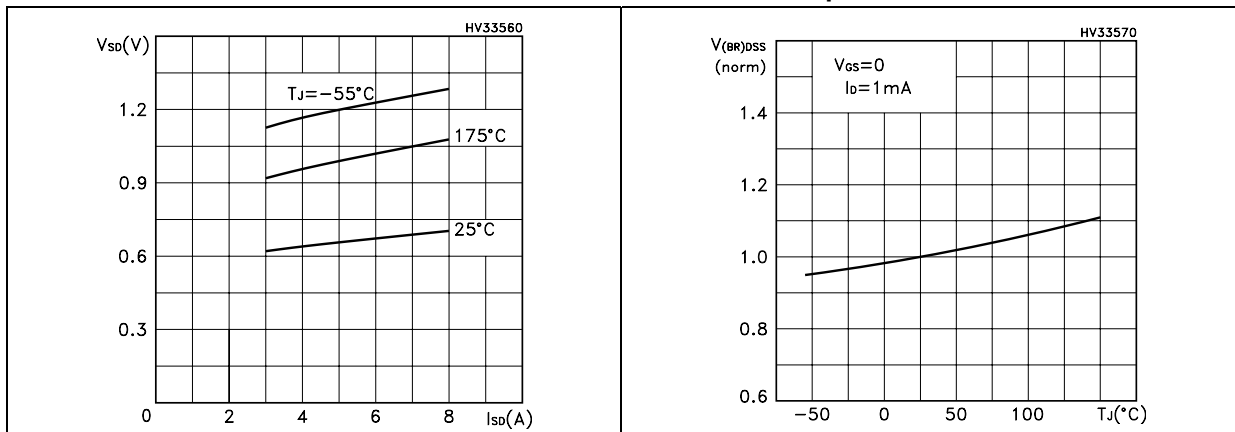


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized breakdown voltage vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

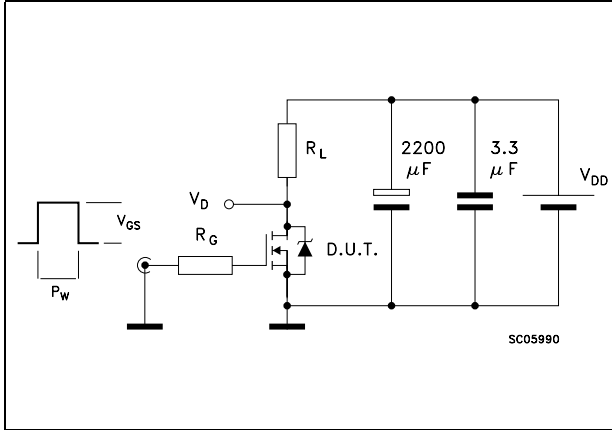


Figure 14. Gate charge test circuit

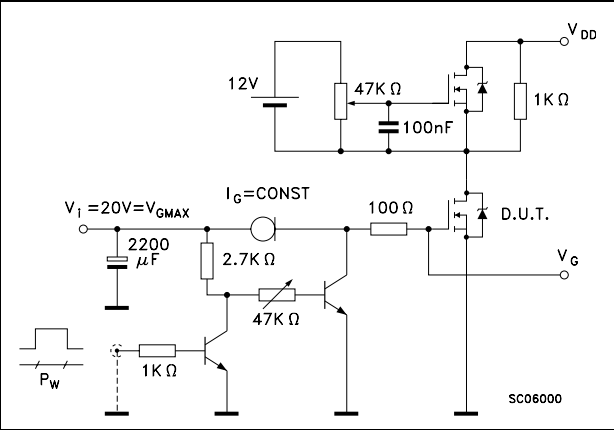


Figure 15. Test circuit for inductive load switching and diode recovery times

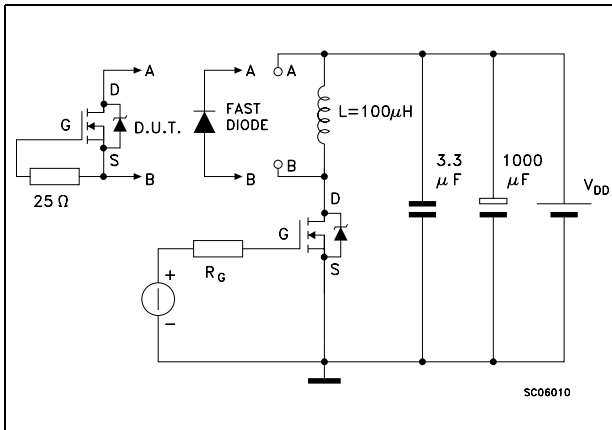


Figure 16. Unclamped inductive load test circuit

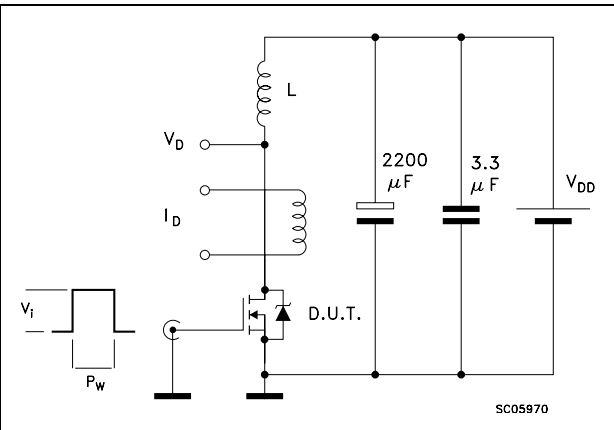


Figure 17. Unclamped inductive waveform

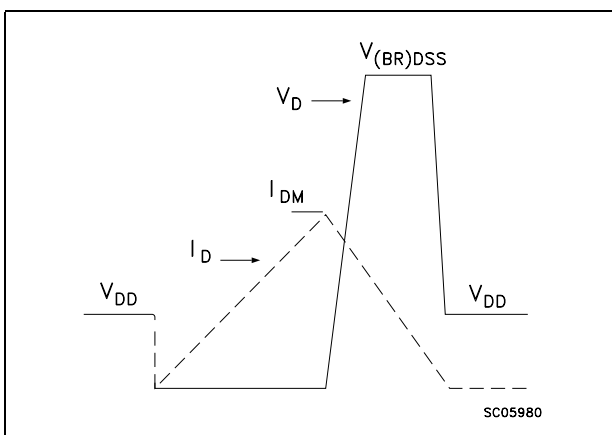
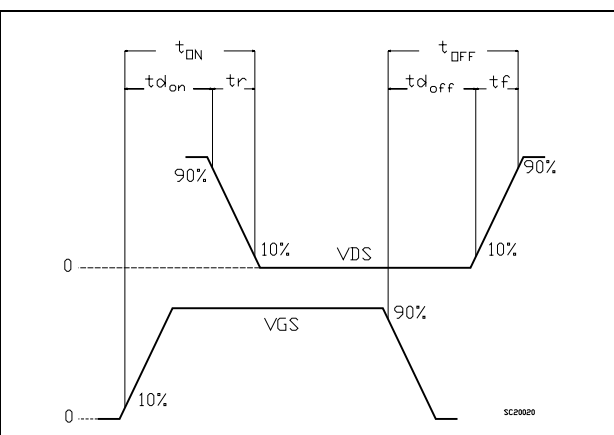


Figure 18. Switching time waveform

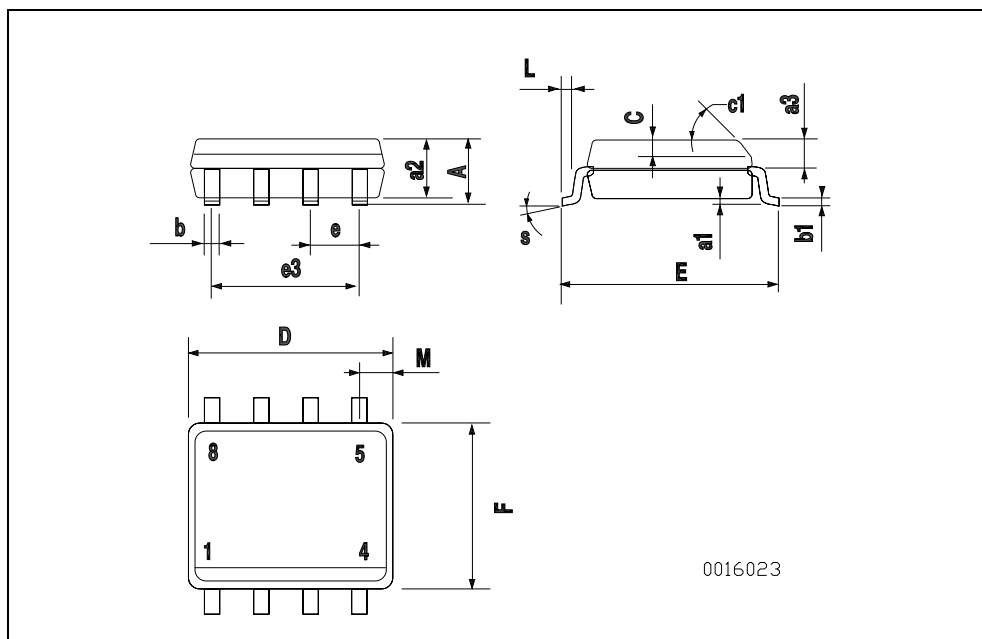


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : www.st.com

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 7. Revision history

Date	Revision	Changes
24-Jul-2006	1	Initial release.

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