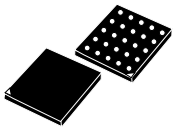
STSMIA832

1.8V/2.8V High speed dual differential line receivers, standard mobile imaging architecture (SMIA) decoder deserializer

Feature summary

- Sub-low voltage differential signaling inputs:
  V_{ID} = 100mV MIN. with R_T = 100Ω, C_L = 10pF
- High signaling rate:
  f_{IN} = 650 Mbps MAX (D+,D-,STRB+,STRB-)
  f_{OUT} = 82 MHz MAX (CLK)
  f_{OUT} = 82 Mbps MAX (for each data line D1-D8)
- Very high speed strobe to clock:
  tp_{LH}~tp_{HL}=5.2ns (TYP) at V_{DD}=2.8V; V_L=1.8V
- Operating voltage range:
  V_{DD}(OPR) = 2.65V to 3.6V
  V_L(OPR) =1.65V to 1.95V
- Symmetrical output impedance (D1-D8, H-SYNC, V-SYNC, CLK):
  $II_{OH}I$=I_{OL}=4mA (MIN) at V_{DD}=2.65V;V_L=1.8V
- Low power dissipation (DISABLED: EN=Gnd):
  I_{SOFF} = I_{DD} + I_L = 10 µA (Max)
- SMIA specification compliant
- CLASS 0 and CLASS 1,2 supported (config by CLASS_SEL)
- CMOS logic input threshold
  (EN, SYNC_SEL, CLASS_SEL):
  V_{IL} = 0.3xV_L; V_L = 1.65V to 1.95V
  V_{IH} = 0.7xVL; V_L = 1.65V to 1.95V
- 3.6V tolerant on inputs
  (EN, SYNC_SEL, CLASS_SEL)
- 32 BIT synchronization codes (SOF, EOF, SOL, EOL)
- Leadfree µTFBGA package
  (RoHS Restriction of hazardous substances)



µTFBGA25

Description

The STSMIA832 receiver converts the subLVDS clock/datastream (up to 650 Mbps throughput bandwidth) back into parallel 8 bits of CMOS/LVTTL. The device recognizes the SMIA 32 bit start of frame (SOF), end of frame (EOF), start of line (SOL) and end of line (EOL) sequences to generate the H-SYNC and V-SYNC signals. Output LVTTL clock (up to 82 MHz) is transmitted in parallel with data. Output data are rising-edge strobes. This chipset is an ideal means to link mobile camera modules to Baseband processors. In order to minimize static current consumption, it is possible to shut down the device when the interface is not being used by a power-down (EN) pin that reduces the Maximum Current Consumption to 10 µA making this device ideal for portable applications like Mobile Phone and Portable Battery Equipment. A configurable input (Class_Sel) is provided to select different CLASS (0 or 1,2) mode inside the SMIA STD specifications.

The STSMIA832 is offered in a µTFBGA package to optimize PCB space. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity from transient excess voltage. The STSMIA832 is characterized for operation over the commercial temperature range -40°C to 85°C.

Order codes

Part number	Temperature Range	Package	Packaging
STSMIA832TBR	-40 to 85 °C	µTFBGA25 3x3mm (TAPE & REEL)	3000 parts per reel

Contents

1 Schematic diagram

Figure 1. Simplified application block diagram

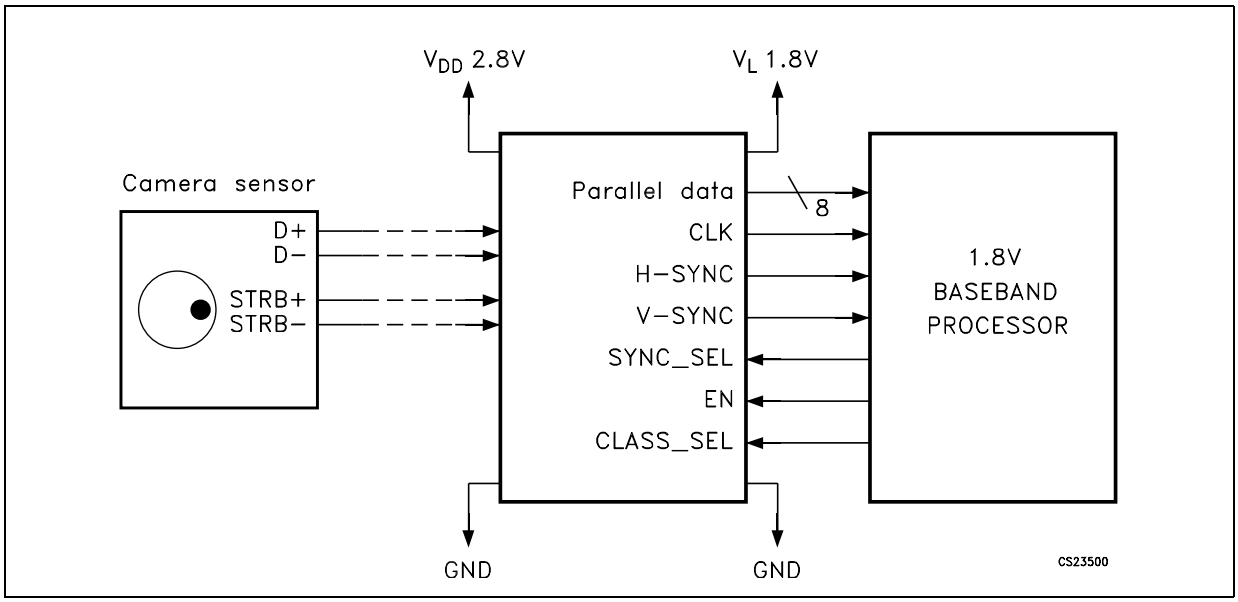
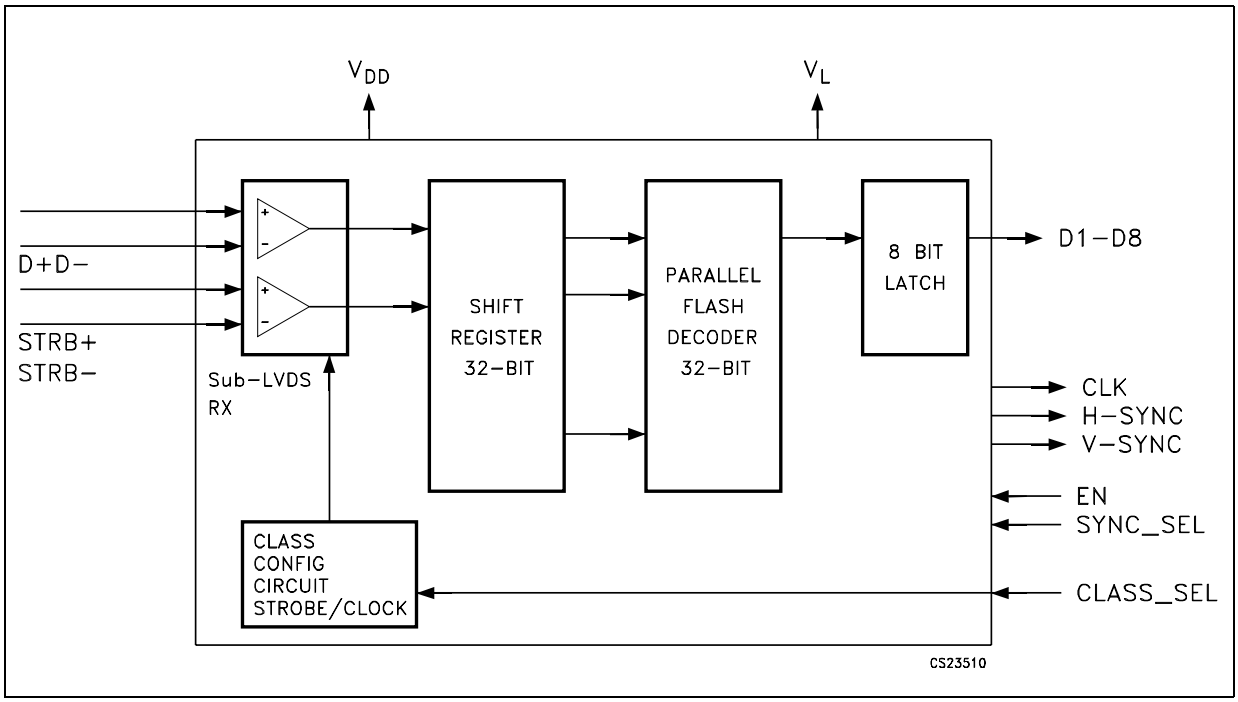


Figure 2. Block diagram



2 Pin configuration

Figure 3. Pin connections (top through view - bumps are on the other side)

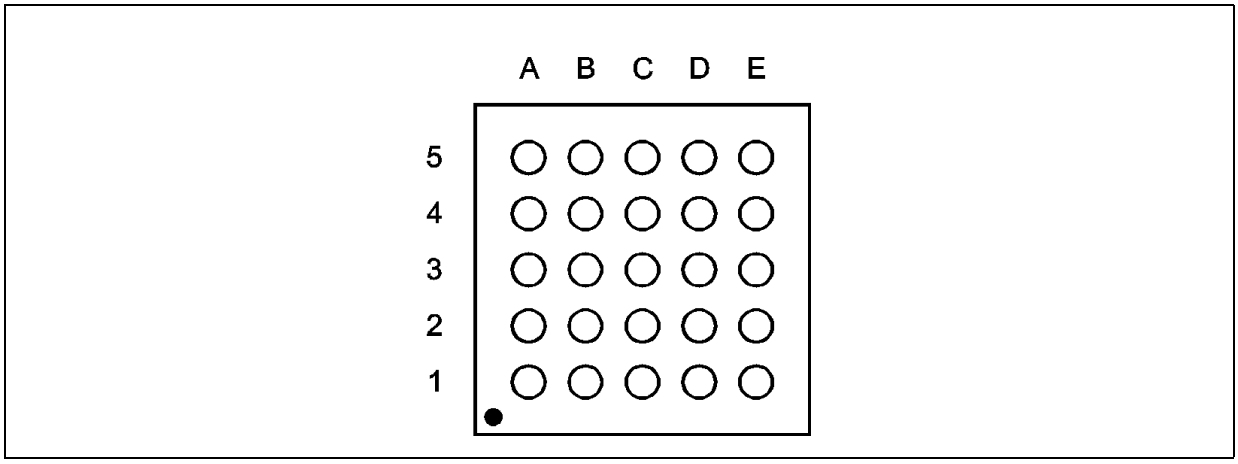


Table 1. Pin description

PIN N°	SYMBOL	NAME AND FUNCTION
D5	D1	Decoder output (LSB)
E5	D2	Decoder output
D4	D3	Decoder output
D3	D4	Decoder output
D2	D5	Decoder output
D1	D6	Decoder output
E1	D7	Decoder output
C3	D8	Decoder output (MSB)
A2, A1	D+, D-	Differential data receiver inputs
A5, A4	STRB+, STRB-	Differential strobe receiver inputs (Class_Sel = VL) Differential clock receiver inputs (Class_Sel = GND)
B3	EN	Receivers enable input
E3	CLK	Clock output
C2	H-SYNC	Horizontal sync output
B2	V-SYNC	Vertical sync output
E2, E4	GND	Ground (Digital I/O reference)
A3, B1	GND	Ground (Analog subLVDS part)
B5	V_{DD}	Core supply voltage
C1, C5	V_L	Digital I/O supply voltage
B4	SYNC_SEL	Select sync input
C4	CLASS_SEL	Select CLASS input

2.1 Pin descriptions for reference:

(D+, D-, STRB+, STRB-)

Differential subLVDS data and strobe inputs to the receiver from the camera sensor interface. The signals operate at 150mV typical differential voltage levels and a common mode voltage of 900mV. The operating data rate is 650Mbps maximum. Depending on the CLASS_SEL pin selection mode, Data/Clock signaling or Data/Strobe signaling modes are activated.

D1-D8, CLK

STSMIA832 output data and clock lines. Parallel 8 bits of CMOS/LVTTL data is output at a maximum data rate of 82Mbps per line. Output LVTTL clock is transmitted in parallel with the data at 82MHz Max.

SYNC-SEL

The Horizontal Sync and Vertical Sync signals are extracted from the data stream before transmitting data on the parallel output D1-D8 if the device is working in ENABLED SYNC mode (SYNC_SEL = V_L). If the device is working in DISABLED SYNC mode (SYNC_SEL = GND) the sync codes are not extracted from the data stream and the embedded Sync codes are transmitted along with the data on the parallel output. This allows for two modes of functioning, formatted and unformatted transmission of data on the data lines based on the selection by the Baseband processor. The main function table lists the functions for various combinations of SYNC_SEL pin and EN pin.

CLASS-SEL

The device embeds all functions forecast inside the SMIA Standard. STRB+ and STRB- signals are considered STROBE Signals when the device is working in HIGH CLASS mode (CLASS_SEL = V_L). If the device is working in LOW CLASS mode (CLASS_SEL = GND) the STRB+ and STRB- inputs change their strobe functionality to CLOCK in order to be compliant with SMIA CLASS 0. In Class 0 mode of operation, data is read on the rising edge only. This allows for two modes of functioning, Clocked and Strobed transmission according to different applications and provides high flexibility to configure the final application in different Baseband processors.

H-SYNC, V-SYNC

In the ENABLED SYNC mode, the parallel data on D1-D8 is accompanied by the Horizontal and Vertical Sync signals on the H-SYNC and V-SYNC pins and together they are used to reconstruct the image frame.

The H-SYNC and V-SYNC are generated by extracting the SMIA 32-bit Synchronization codes (SOF, EOF, SOL, EOL) on the serial input data stream.

EN

Enable pin is to enable the Power-Down Mode. This mode enables the shutting down of the device when the interface is not in use. The maximum current consumption can be reduced to 10 µA. This provision makes this device suitable for portable applications like Mobile phones or Portable Battery Equipment.

V_{DD}, V_L

Both the Camera Sensor module and the Baseband processor interface operate at V_L = 1.8V. The subLVDS receiver core operating voltage is V_{DD} = 2.8V typical.

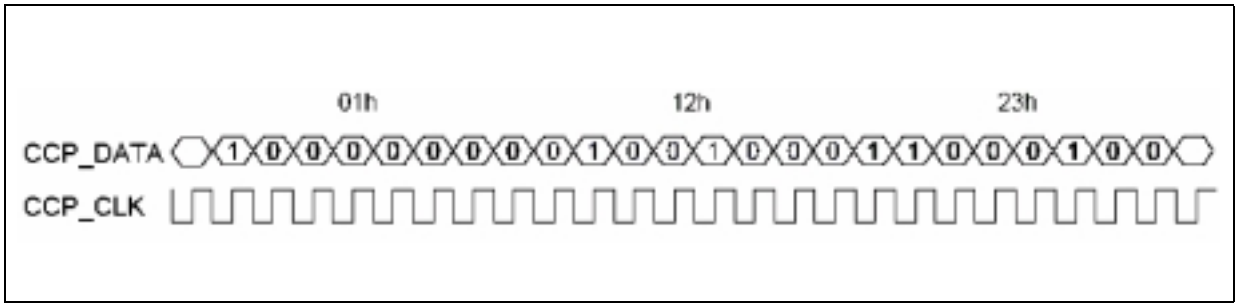
2.2 Supplementary notes: SMIA specification

The Standard Mobile Imaging Architecture (SMIA) specification defines an interface between the digital camera module and mobile phone engine. It defines a standard data transmission and control interface between transmitter (camera module) and receiver (mobile phone engine). The data transmission interface (referred to as CCP2) is a unidirectional differential serial interface with data and clock/strobe signals. The physical layer of CCP2 is based on signaling scheme called SubLVDS, which is current mode differential low voltage signaling method modified from the IEEE 1596.3 LVDS standard for reduced power consumption. STSMIA832 operates in a data/strobe signaling mode. The use of data-strobe coding together with SubLVDS enables the use of high data rates with low EMI.

Data/Clock signaling

Data is a differential output from camera module. Data format is in most of cases bytewise (i.e. on 8-bit boundary) least significant bit (LSB) first. When nothing is being transferred, the DATA lines remain high, except in power shutdown. Figure illustrates the bytewise LSB first transmission..

Figure 4. Data clock signaling



Clock is a differential signal, output from camera module. The receiver reads the data on rising edge of the CCP_CLK. The clock signal may be free running or gated. For most cases free running clock is preferred due to simpler implementation in the transmitting end. However, in some cases gated clock may be better solution. If gated transmission clock is used, clock remains high when nothing is being transferred, except in power shutdown.

Data/Strobe signaling

The data-strobe coding consists of two parallel signals, data and strobe. The data signal carries the bit-serial data while the strobe signal state toggles whenever data signal does not change state. Thus, either the data signal or the strobe signal changes between two data bits. If both signals change simultaneously it is interpreted as an error. The signaling method is presented in the figure 2 below.

The benefit of using data-strobe signaling is that there is no need for transferring continuous clock over the CCP2 bus. The frequency of the bus is also divided by two. The clock is reconstructed at the receiving end from the data and strobe signals. This simplifies the EMC design and in addition, EMI is reduced compared to normal data/clock signaling.

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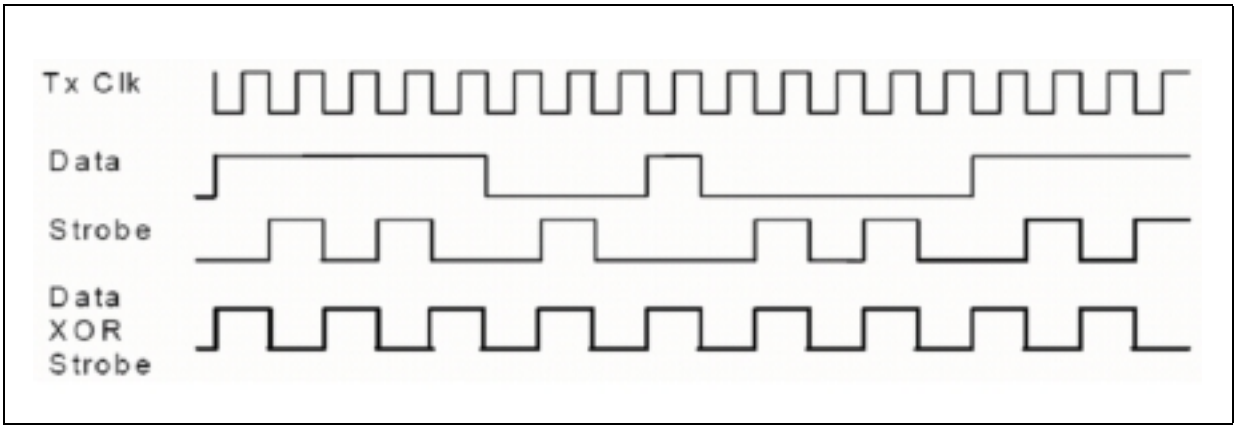
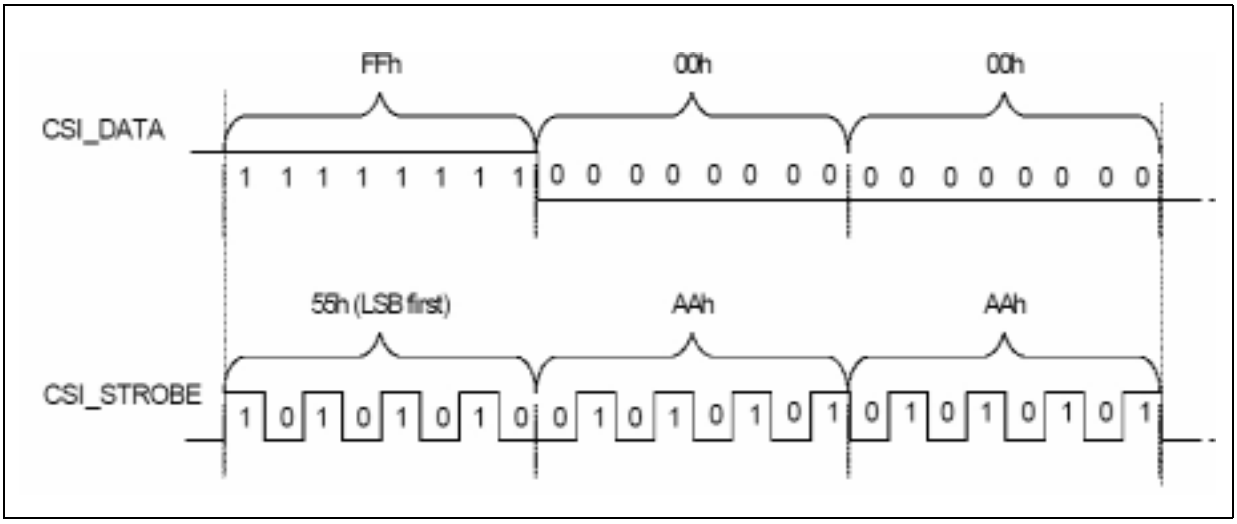
Figure 5. Data-Strobe signaling



Data is sent byte-wise LSB first. The state of the data and strobe signals at the beginning of transmission are fixed i.e. the state of data is logic high and the state of strobe is logic low. The number of clock cycles between synchronization codes has to be even, both between SOL (or SOF) – EOL (or EOF) and EOL (or EOF) – SOL (or SOF). This ensures synchronization is possible with minimum complexity to achieve the fastest possible implementation. The strobe signal can be gated when using the data/strobe signaling, but only if the number of clock cycles is even between synchronization codes.

If the number of transmission clock cycles between synchronization codes is even, it ensures that for each synchronization code sequence FF0000h there will be corresponding strobe sequence of 55AAAAh as illustrated in the Figure 3 below.

Figure 6. Data-Strobe phase relationship

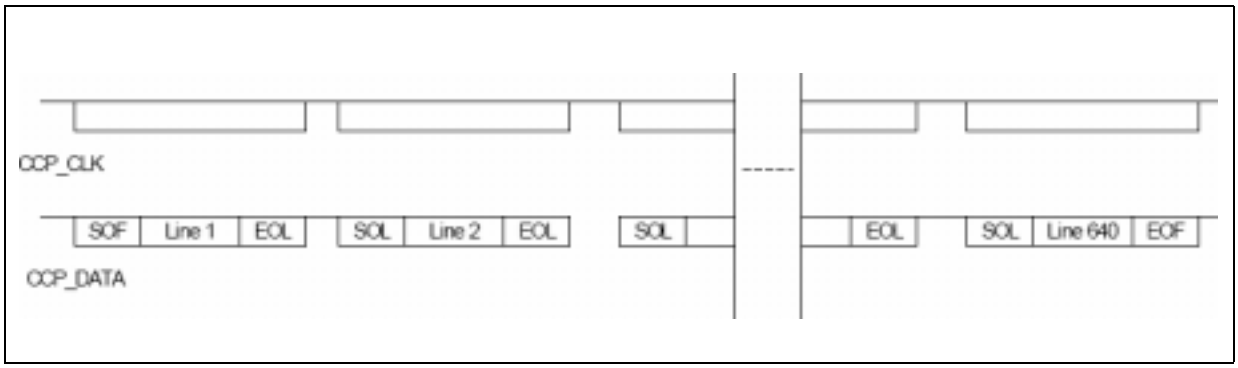


Frame synchronization

Each image frame begins with frame start synchronization code (SOF) and ends with frame end synchronization code (EOF). Each line inside the frame begins with line start synchronization code (SOL) and ends with line end synchronization code (EOL). The period between EOL code and new SOL code is called line blanking period. Similarly, the time between EOF code and new SOF code is called frame blanking period. The total size of one image frame shall be a multiple of 128 bits.

In the beginning of frame and in the end of frame, line synchronization codes are replaced by the frame synchronization codes. Synchronization signal usage is shown in Figure 4 below. Bit order of the synchronization codes is the same as for data, byte-wise LSB first.

Figure 7. CCP2 Synchronization codes



The purpose of logical channels is to separate different data flows, which are interleaved in the data stream.

The DMA channel identifier number is directly encoded in the 4-byte CCP embedded sync codes. The CCP receiver will monitor the DMA channel identifier and de-multiplex the interleaved video streams to their appropriate DMA channel. A maximum of 8 data streams is supported. Valid channel identifiers are 0 to 7.

Table 2. Synchronization codes as per SMIA specifications

Name	Synchronization Codes	Notes
SOL	FFH 00H 00H X0H	Line Start Code
EOL	FFH 00H 00H X1H	Line End Code
SOF	FFH 00H 00H X2H	Frame Start Code
EOF	FFH 00H 00H X3H	Frame End Code
Logical Channels	FFH 00H 00H 0XH (to) FFH 00H 00H 7XH	DMA Channel Identifier from Channel 0 to 7

X = channel number 0 to 7.

3 Application information

3.1 Inputs

Technological advancements in deeper submicron processes have lowered the supply voltage levels of semiconductor devices, creating a design environment where system board devices may potentially use many different supply voltages, which can ultimately lead to voltage conflicts. However, STSMIA832 device has been designed to work with a 3.6V input tolerance. This implies that all input pins (differential inputs and control inputs) can be connected to 3.6V logic or bus even when power to the device is only 1.8V. The device would not be damaged.

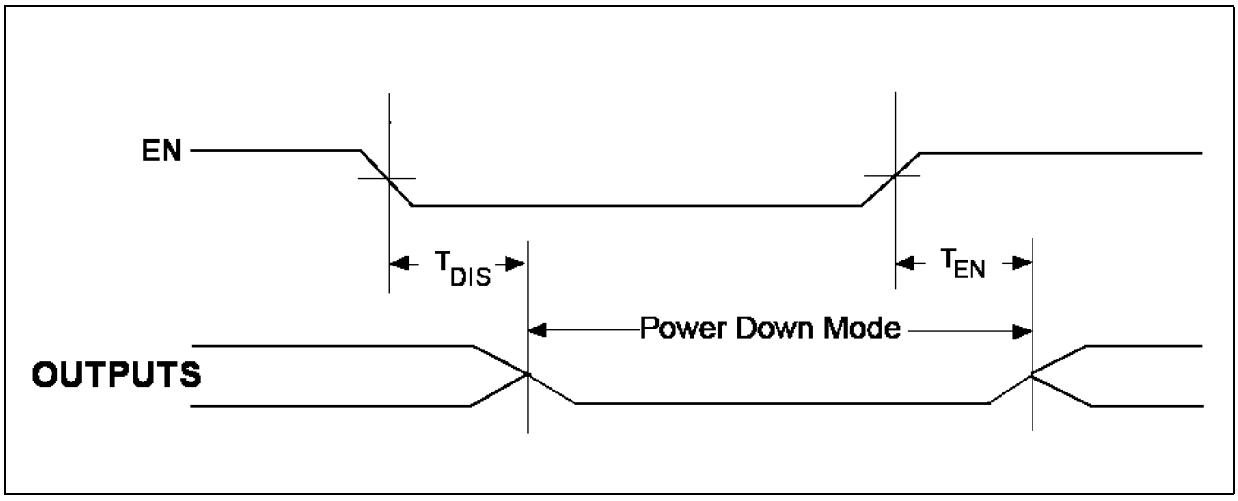
3.2 Power down mode

STSMIA832 comes equipped with a Power Down mode that permits an exceptionally low level of power consumption (I_{SOFF} = 10 µA maximum), making the device ideal for portable battery-powered applications as well as for designs with tight thermal budgets.

The low quiescent supply current possible with Power Down mode is especially useful for products that must use power as efficiently as possible. Low power offers additional benefits such as low operating temperature, low cost packages and high device reliability. The device saves significant quiescent power while internal functions are temporarily suspended.

The activation and de-activation of the power down mode is controlled by the EN pin. The mode becomes active once a low-level pulse is applied to the EN pin. The maximum quiescent supply current gets reduced to I_{SOFF} = 10 µA maximum. Power Down mode is initiated by applying a low-level pulse to the EN input of STSMIA832 device. The device remains in a DC state, drawing minimal power, until EN goes High, at which point it returns to full operation.

Figure 8. STSMIA832 Power down mode



The power saving in the Power Down Mode is obtained by employing the following techniques:

3.3 Power saving at the inputs

All internal blocks of the input circuitry are shutdown by turning off the bias currents for the subLVDS Receivers. This eliminates the power associated with any dynamic activity on the input pins. With no pull-up and pull-down resistors, any remaining current drawn by an input is known as leakage current (I_L), which ranges from 1 µA to 4 µA typical. But care should be taken that the driving circuit for the inputs is also switched to a known state and that there are no transitions on the inputs when the device is in Power Down Mode.

3.4 Switching off digital blocks

To save power, all signals within the device are prevented from switching by resetting all the digital blocks in the internal circuits. In many designs, a major portion of the total dynamic power is due to its clock tree, which consists of all the inter-connects that distributes the clock signal internally. Power drawn varies according to how extensive the tree is. Pulling the clock input to a static logic level (LOW in this case) is an important way to save power, especially as the clock frequency is high

3.5 Disabling the outputs

In the power down mode, to save the power due to transition on output flip flops, the Clock Enable (CE) signal for all the flip-flops is used in the design. All the clock transitions are ignored when the CE signal is inactive and so the output flip flops do not toggle. The CE signal is activated once again when the registered outputs need to be operating under normal conditions. All the outputs (including D1-D8) are driven LOW in the power down state. This reset state is held as long as the device remains in Power Down mode.

Once having exited the mode, normal operation recommences from the reset state.

3.6 Load capacitance

Power dissipation is proportional to capacitance. The capacitance consists both of internal and external capacitance. The lumped internal capacitance is associated with the power dissipated internally by the device and depends on the device characteristics (in STSMIA832, C_{IN} is 4pF). The external capacitance is associated with power dissipated outside the device and it is a function of PCB traces loading and other IC loads.

In high frequency operation, it is essential to have equal trace lengths for all the output lines in order to minimize the skew. A reduced external capacitance leads to reduced current consumption and also reduced rise time and fall time. The parallel output driving capacitance in STSMIA832 is 10pF and the rise time and fall times for the LVTTL parallel outputs are 2.2ns maximum.

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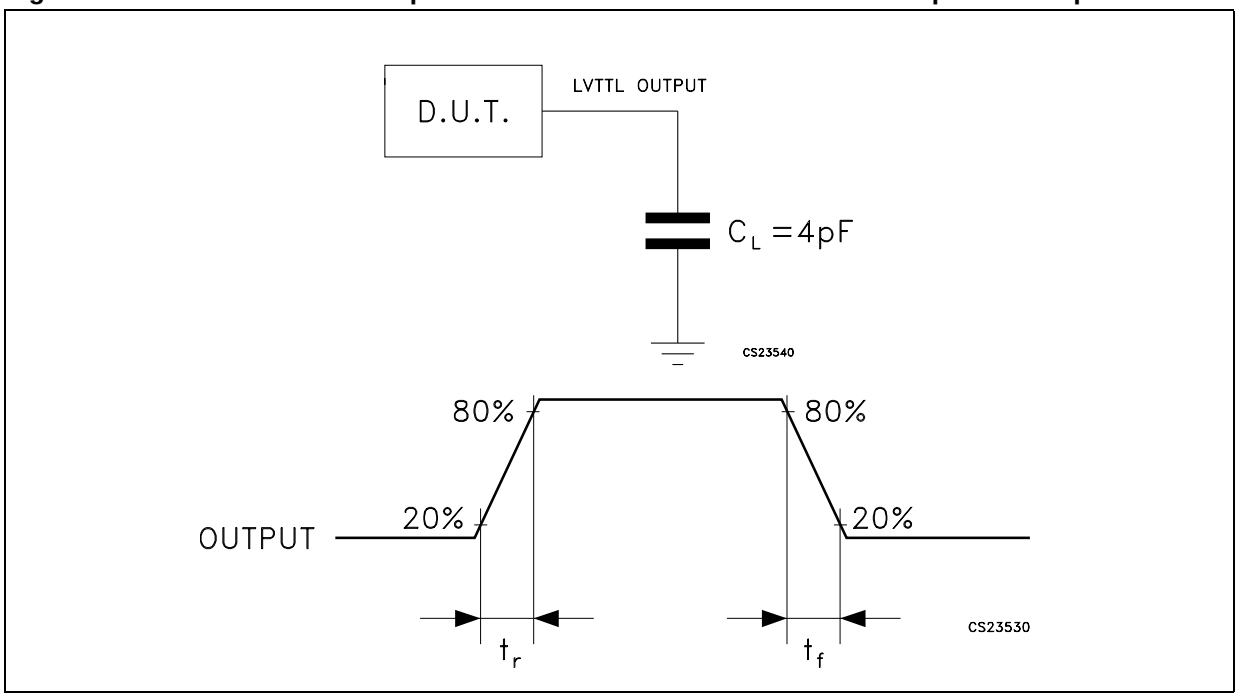
Figure 9. STSMIA832 Load capacitance and rise and fall time of LVTTL parallel outputs



3.7 Board layout

To obtain the maximum benefit from the noise and EMI reductions of subLVDS, attention should be paid to the layout of differential lines. Lines of a differential pair should always be adjacent to eliminate noise interference from other signals and take full advantage of the noise canceling of the differential signals. Equal length should be maintained on signal traces for a given differential pair. As with any high-speed design, the impedance discontinuities should be limited (reduce the numbers of vias and no 90 degree angles on traces). Any discontinuities which do occur on one signal line should be mirrored in the other line of the differential pair. Care should be taken to ensure that the differential trace impedance match the differential impedance of the selected physical media (this impedance should also match the value of the termination resistor (100 ohms) that is connected across the differential pair at the receiver's input). Surface mount resistors are recommended to avoid the additional inductance that accompanies leaded resistors.

These resistors should be placed as close as possible to the receiver input pins to reduce stubs and effectively terminate the differential lines. All of these considerations will limit reflections and crosstalk which adversely effect high frequency performance and EMI.

3.8 Decoupling capacitors

Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. For a conservative approach three parallel-connected decoupling capacitors (Multi-Layered Ceramic capacitors in surface mount form factor) between each V_{CC} and the ground plane(s) are recommended. An example is shown in the figure below. Wide traces for power and ground should be used and it should be ensured each capacitor has its own via to the ground plane.

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Figure 10. Bypass decoupling capacitors

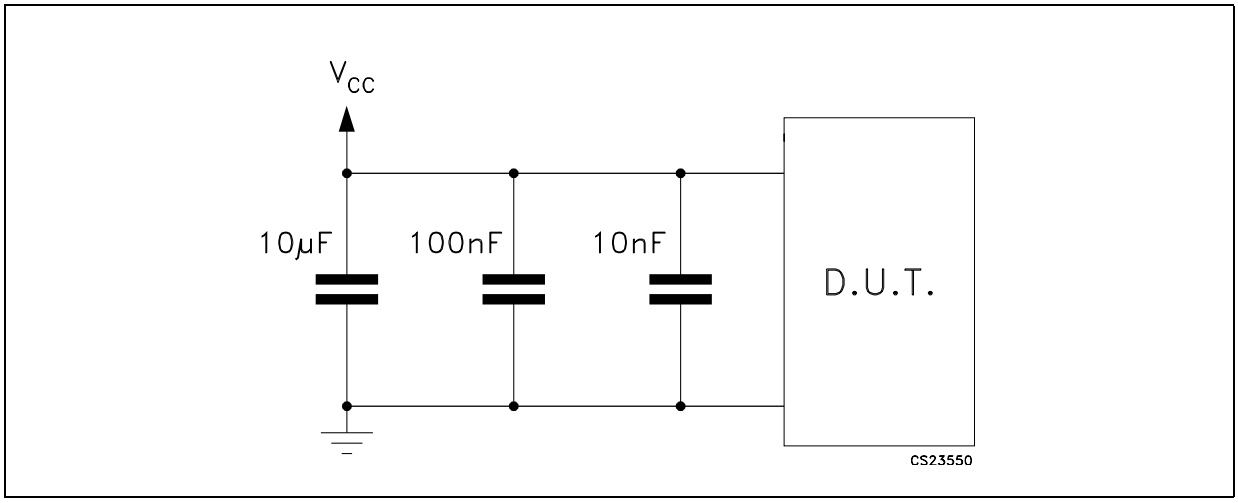


Table 3. Synchronization codes as per SMIA specifications

INPUT						OUTPUT				FUNCTION
EN	SYNC_SEL	D+	D-	STRB+	STRB-	V-SYNC	H-SYNC	D1-D8	CLK	
L	X	X	X	X	X	L	L	L	L	SMIA disabled
H	H	SOF (FF_H 00_H 00_H 02_H)				H	H	See Detailed Timing Diagram		Start of Frame
H	H	EOF(FF_H 00_H 00_H 03_H)				L	L			End of Frame
H	H	SOL(FF_H 00_H 00_H 00_H)				No Change	H			Start of Line
H	H	EOL(FF_H 00_H 00_H 01_H)				No Change	L			End of Line
H	L	X	X	X	X	L	L	D+, D- data in parallel mode	See Detailed Timing Diagram	DisabledSync (D1-D8 will get out data, including Sync Code)

X = Don't care

Table 4. Class function table (CSI Classification)

CLASS	Data Transfer Capacity (Sustained Data Rate)	Signaling Method	CLASS_SEL
Class 0	<208 Mbps	Data/Clock	GND
Class 1	208-416 Mbps	Data/Strobe	V_L
Class 2	416-650 Mbps	Data/Strobe	V_L

4 Maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Main Supply Voltage	-0.5 to 4.6	V
V_L	Secondary Supply Voltage	-0.5 to (V_{DD} + 0.5)	V
V_D	SubLVDS Data Bus Input Voltage (D+, D-)	-0.5 to 4.6	V
V_{STRB}	SubLVDS Clock Bus Input Voltage (STRB+, STRB-)	-0.5 to 4.6	V
V_I	DC Input Voltage (SYNC_SEL, CLASS_SEL, EN)	-0.5 to 4.6	V
V_O	DC Output Voltage (D1-D8, H-SYNC, V-SYNC, CLK)	-0.5 to (V_L + 0.5)	V
T_{stg}	Storage Temperature Range	-65 to +150	°C
ESD	Electrostatic Discharge Protection HBM Human Body Model (All Pins)	±2	kV

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 6. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Main Supply Voltage	2.65	2.8	3.6	V
V_L	Secondary Supply Voltage	1.65	1.8	1.95	V
V_{ID}	Differential Level Input Voltage (D+, D-, STRB+, STRB-)	0.1		0.4	V
V_{CM}	Common Level Input Voltage (D+, D-, STRB+, STRB-)	0.5	0.9	1.3	V
V_{IC}	Level Input Voltage (SYNC_SEL, CLASS_SEL, EN)	1.65	1.8	3.6	V
R_T	Termination Resistance (per pair differential input line)	80	100	120	Ω
C_L	Termination Capacitance (per line vs Gnd Pin)		10		pF
T_A	Operating Ambient Temperature Range	-40		85	°C
T_J	Operating Junction Temperature Range	-40		125	°C
t_R, t_F	Rise and Fall Time (SYNC_SEL, CLASS_SEL, EN; 10% to 90%; 90% to 10%)			10	ns

5 Characteristics

Table 7. Electrical characteristics
(Over recommended operating conditions unless otherwise noted. All typical values are at T_A = 25°C, and V_{DD} = 2.8V, V_L = 1.8V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CM}	Common Mode Input Voltage	R_T = 100Ω ± 1%	0.5	0.9	1.3	V
V_{THL}	Receiver Input Low Threshold (1)	R_T = 100Ω ± 1%	-25			mV
V_{THH}	Receiver Input High Threshold (1)	R_T = 100Ω ± 1%			+25	mV
I_I	Input Leakage Current (D+, D-, STRB+, STRB-)	V_I = 0.4V			±10	µA
		V_I = 1.4V			±10	µA
I_S	Supply Current (I_L + I_{DD})	EN=V_{DD}, D+, STRB+ = Gnd or V_{DD}, D-, STRB- = V_{DD} or Gnd		3.5	9.0	mA
I_{SOFF}	Shutdown Supply Current (I_L+ I_{DD})	EN=Gnd, V_{DD}=2.65V to 3.6V V_L=1.65V to 1.95V			10	µA
V_{IH}	HIGH Level Input Voltage (SYNC_SEL, CLASS_SEL, EN)	V_{DD} = 2.65V to 3.6V V_L = 1.65V to 1.95V	0.7xV_L		3.6V	V
V_{IL}	LOW Level Input Voltage (SYNC_SEL, CLASS_SEL, EN)	V_{DD} = 2.65V to 3.6V V_L = 1.65V to 1.95V	0		0.3xV_L	V
I_{IH}	HIGH Level Input Current (SYNC_SEL, CLASS_SEL, EN)	V_{IH} = 0.7xV_L			±10	µA
I_{IL}	LOW Level Input Current (SYNC_SEL, CLASS_SEL, EN)	V_{IL}= 0.3xV_L			±10	µA
V_{OH}	HIGH Level Output Voltage (D1-D8, H-SYNC, V-SYNC, CLK)	I_{OH} = -4mA	1.25			V
V_{OL}	LOW Level Output Voltage (D1-D8, H-SYNC, V-SYNC, CLK)	I_{OL} = +4mA			0.30	V

1. Guaranteed by design

Table 8. Capacitive characteristics

Symbol	Parameter	Test Conditions		Value			Unit
		V_{DD} (V)		T_A = 25°C			
				Min.	Typ.	Max.	
C_{IN}	Input Capacitance (SYNC_SEL, CLASS_SEL, EN)	2.65 to 3.6	V_L = 1.65V to 1.95V, V_I = GND or V_L		4		pF

Table 9. Switching characteristics

(R_T = 100Ω ± 1%, C_L = 10pF, over recommended operating conditions unless otherwise noted. Typical values are referred to T_A = 25°C and V_{DD} = 2.8V, V_L = 1.8V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_r	Rise Time LVTTL Output Voltage (10% to 90%)			1.9	2.5	ns
t_f	Fall Time LVTTL Output Voltage (90% to 10%)			1.6	2.5	ns
t_{pLH}	Propagation Delay Time (STRB to V-SYNC, H-SYNC) Low to High	Strobed Transmission CLASS_SEL=V_L		6.3	8.5	ns
t_{pHL}	Propagation Delay Time (STRB to V-SYNC, H-SYNC) High to Low			6.9	8.5	ns
t_{pLH}	Propagation Delay Time (STRB to CLK) Low to High	Strobed Transmission CLASS_SEL=V_L		5.2	6.5	ns
t_{pHL}	Propagation Delay Time (STRB to CLK) High to Low			5.2	6.5	ns
t_{pLH}	Propagation Delay (STRB to D1-D8) Low to High	Strobed Transmission CLASS_SEL=V_L		6.8	8.5	ns
t_{pHL}	Propagation Delay (STRB to D1-D8) High to Low			6.4	8.5	ns
t_{pLH}	Propagation Delay Time (STRB to V-SYNC, H-SYNC) Low to High	Clocked Transmission CLASS_SEL= Gnd		6.0	7.0	ns
t_{pHL}	Propagation Delay Time (STRB to V-SYNC, H-SYNC) High to Low			6.0	7.0	ns
t_{pLH}	Propagation Delay Time (STRB to CLK) Low to High	Clocked Transmission CLASS_SEL= Gnd		4.7	6.0	ns
t_{pHL}	Propagation Delay Time (STRB to CLK) High to Low			4.7	6.0	ns
t_{pLH}	Propagation Delay (STRB to D1-D8) Low to High	Clocked Transmission CLASS_SEL= Gnd		6.0	7.5	ns
t_{pHL}	Propagation Delay (STRB to D1-D8) High to Low			5.4	7.5	ns
t_{EN}	Enable Delay Time (EN to V-SYNC, H-SYNC)	t_{rEN} = 2.0ns (10% to 90%) t_{fEN} = 2.0ns (90% to 10%)			20	µs
t_{DIS}	Disable Delay Time (EN to V-SYNC, H-SYNC)	t_{rEN} = 2.0ns (10% to 90%) t_{fEN} = 2.0ns (90% to 10%)			100	ns
DR_{MAX}	Max Usable Data Rate	CLASS_SEL=V_L			650	Mbps
T_{STRB}	Strobe Target Period	CLASS_SEL=V_L	1538			ps
t_{DS}	Minimum Data/Strobe Edge Separation	CLASS_SEL=V_L	780			ps

6 Frame structure.

Figure 11. Frame structure in VGA case (allowed synchronization codes sequence)

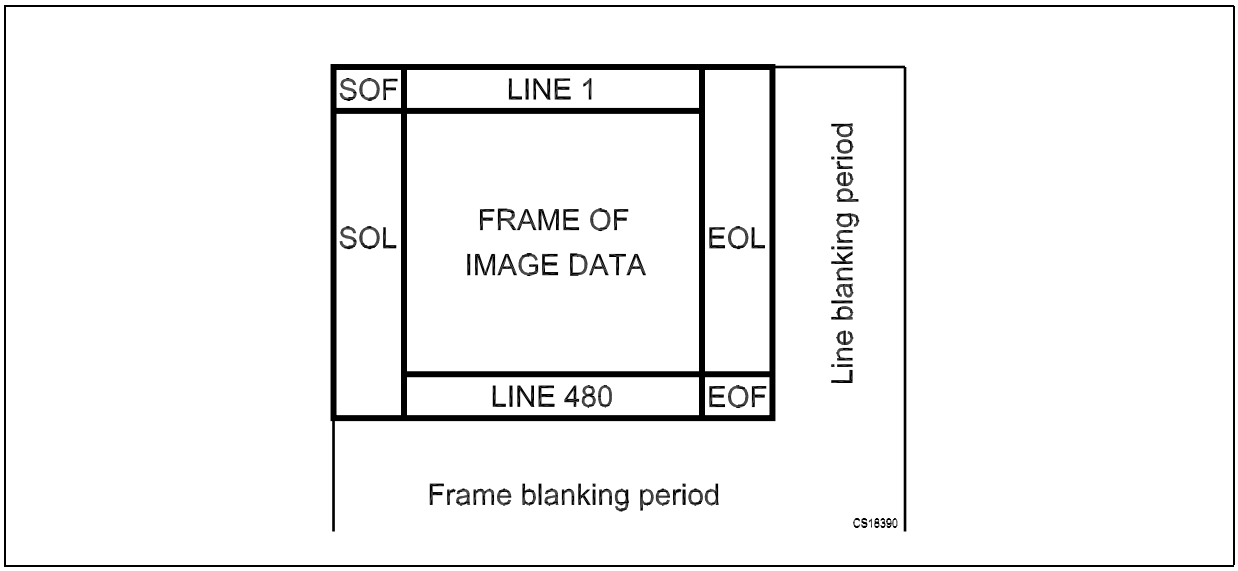
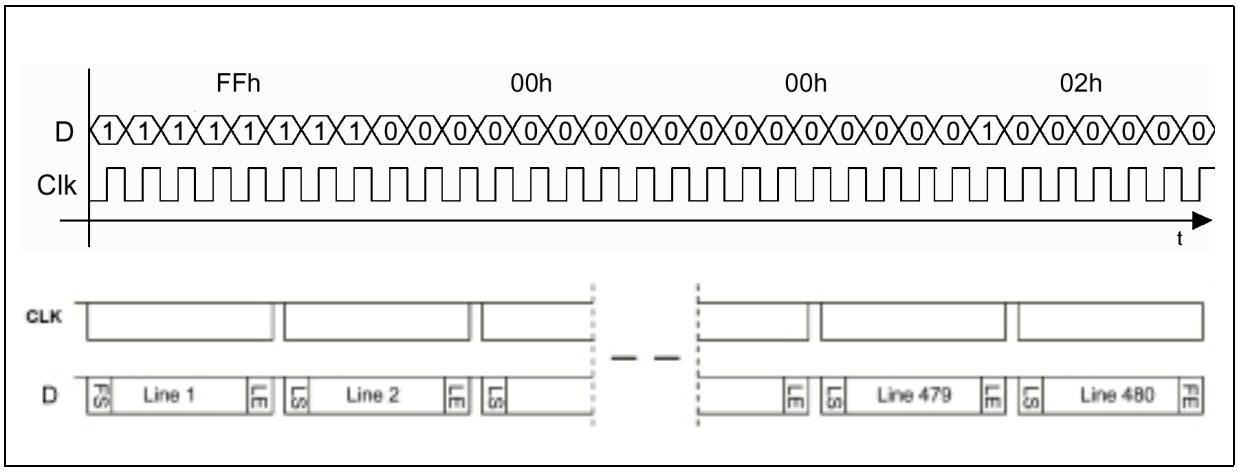


Figure 12. Bit order in synchronization codes and data, LSB first (example start of frame), image frame structure

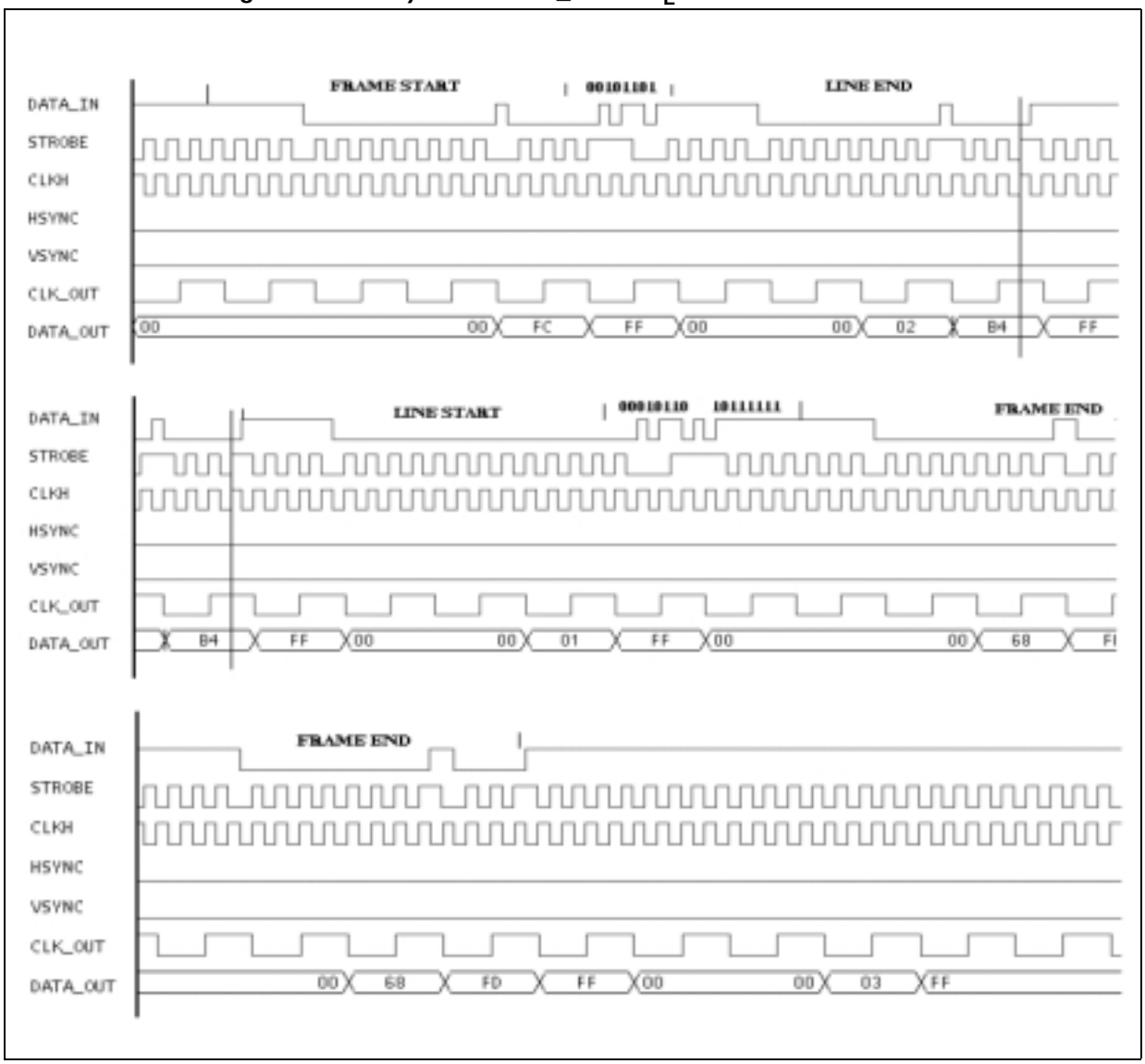


1. LSB (bytewise Least Significant Bit first)

7 Timing diagram

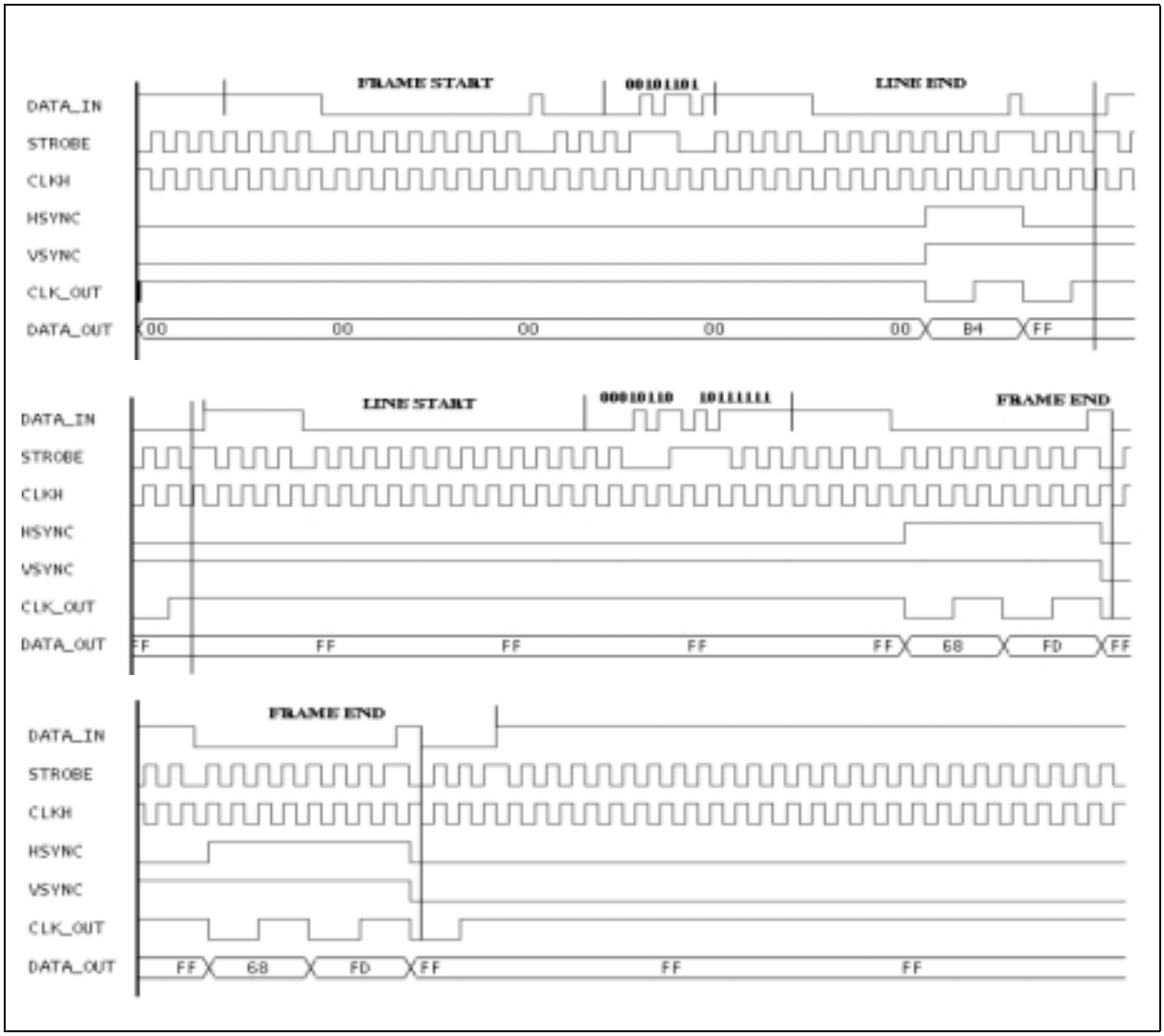
(unless otherwise specified T_A = 25°C)

Figure 13. Disabled Sync Mode (SYNC_SEL = GND) (D1-D8 will transmit the input data DIN, including SYNC CODE) and CLASS_SEL = V_L



1. Note: DATA_IN and STROBE are the input signals, CLKH is an internal signal i.e internal extracted clock having half frequency respect to the external clock. All others are output signals.

Figure 14. Enabled sync mode (SYNC_SEL = VDD) (D1-D8 will transmit the input data DIN, excluding SYNC CODE) and CLASS_SEL = V_L



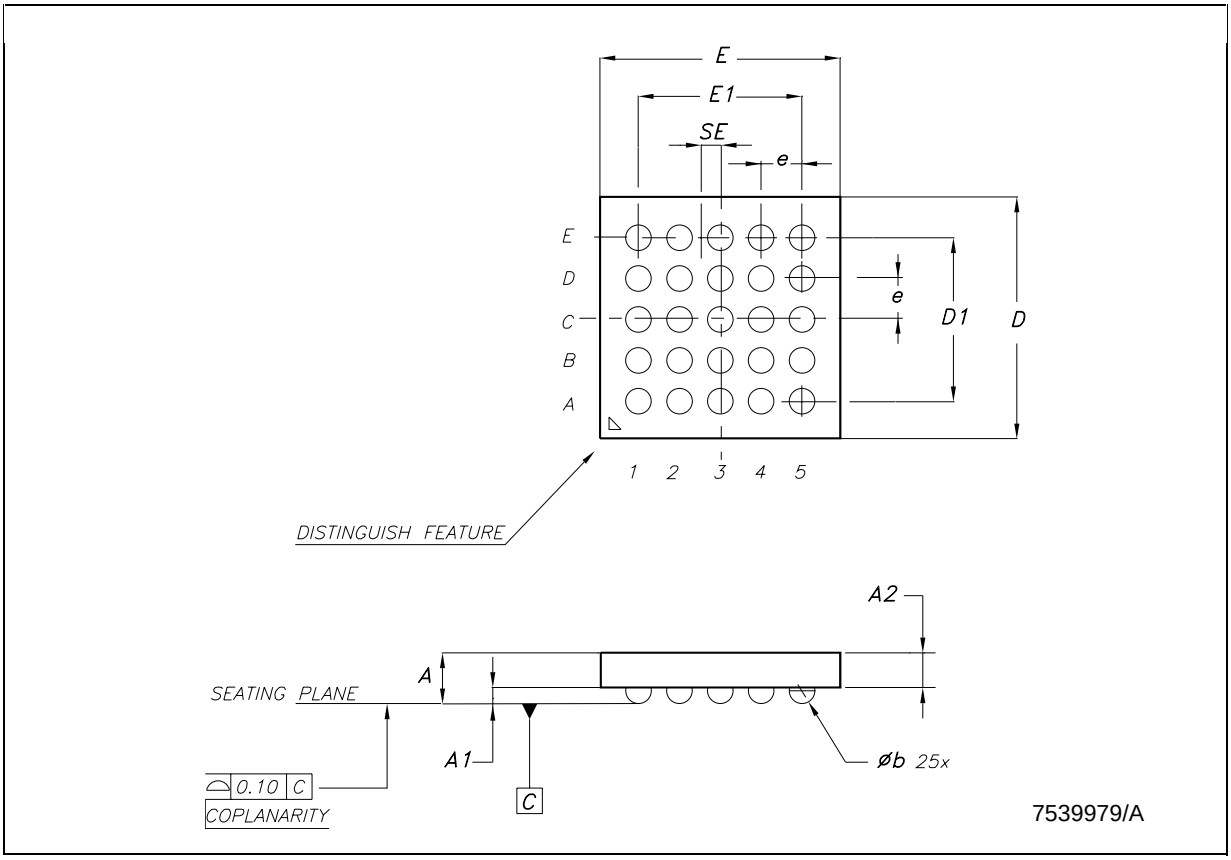
1. Note: DATA_IN and STROBE are the input signals, CLKH is an internal signal i.e internal extracted clock having half frequency respect to the external clock. All others are output signals.

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

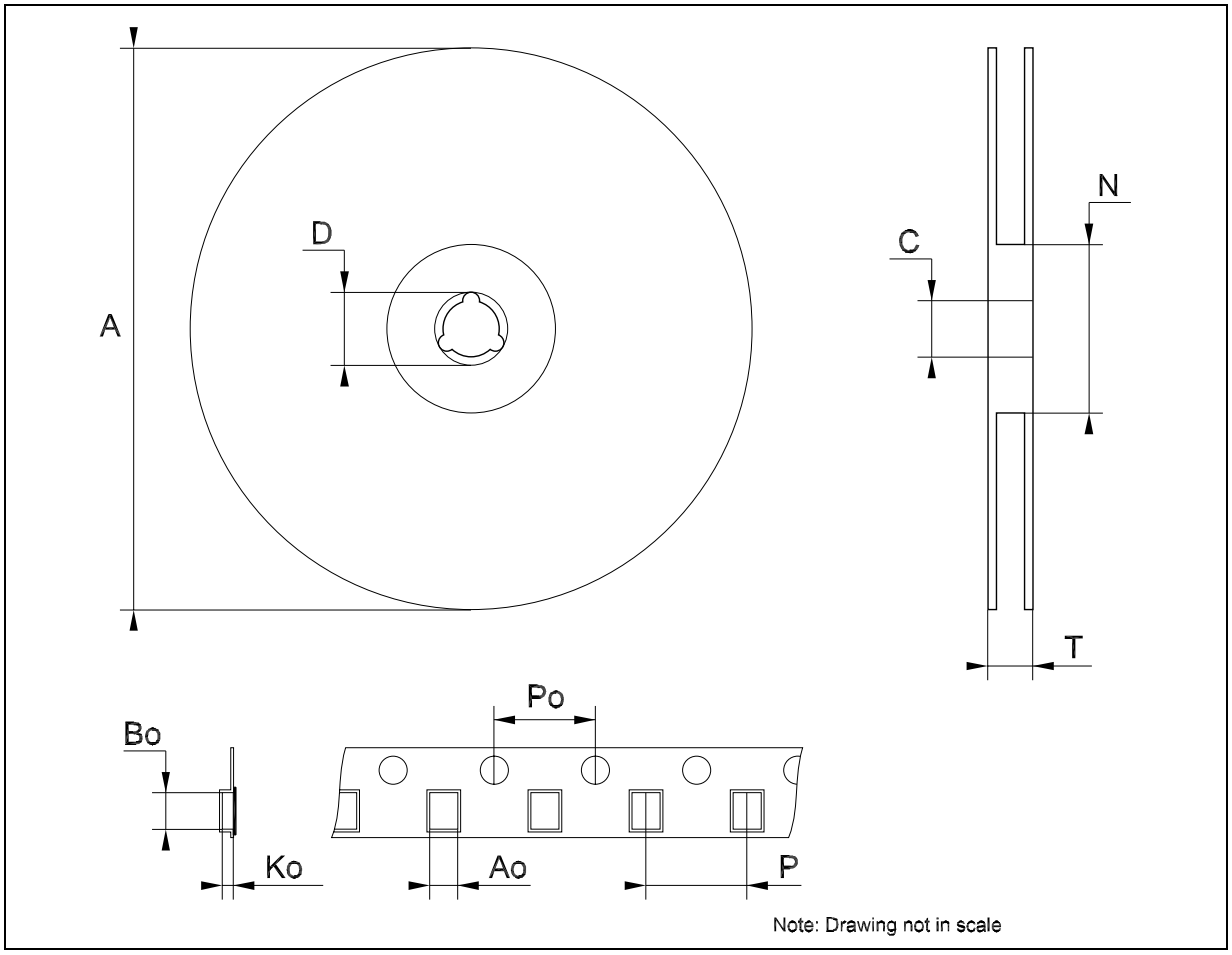
µTFBGA25 MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.0	1.1	1.16	39.4	43.3	45.7
A1			0.25			9.8
A2	0.78		0.86	30.7		33.9
b	0.25	0.30	0.35	9.8	11.8	13.8
D	2.9	3.0	3.1	114.2	118.1	122.0
D1		2			78.8	
E	2.9	3.0	3.1	114.2	118.1	122.0
E1		2			78.8	
e		0.5			19.7	
SE		0.25			9.8	



Tape & Reel TFBGA25 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.60			0.063	
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

9 Revision history

Table 10. Revision history

Date	Revision	Changes
13-Mar-2006	1	Initial release.
3-May-2006	2	Mistake on table 3 - Output.

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