STV0502

CCD SENSORS ANALOG PROCESSOR IC

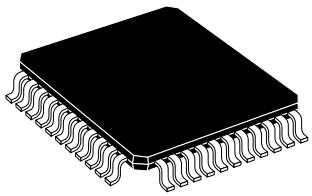
- SERIAL BUS CONTROL

VIDEO

- CORRELATED DOUBLE SAMPLING OF THE CCD SIGNAL
- DIGITALLY CONTROLLED VARIABLE AMPLIFIER AND BLACK CLAMP LEVEL
- 8 BITS PIXEL RATE ADC

AUDIO

- MICROPHONE PREAMP WITH SWITCHABLE AGC (RANGE 34dB - 60dB) OR FIXED GAIN



TQFP44 Full (10 x 10 x 1.40mm)
(Plastic Quad Flat Pack)

ORDER CODE : STV0502

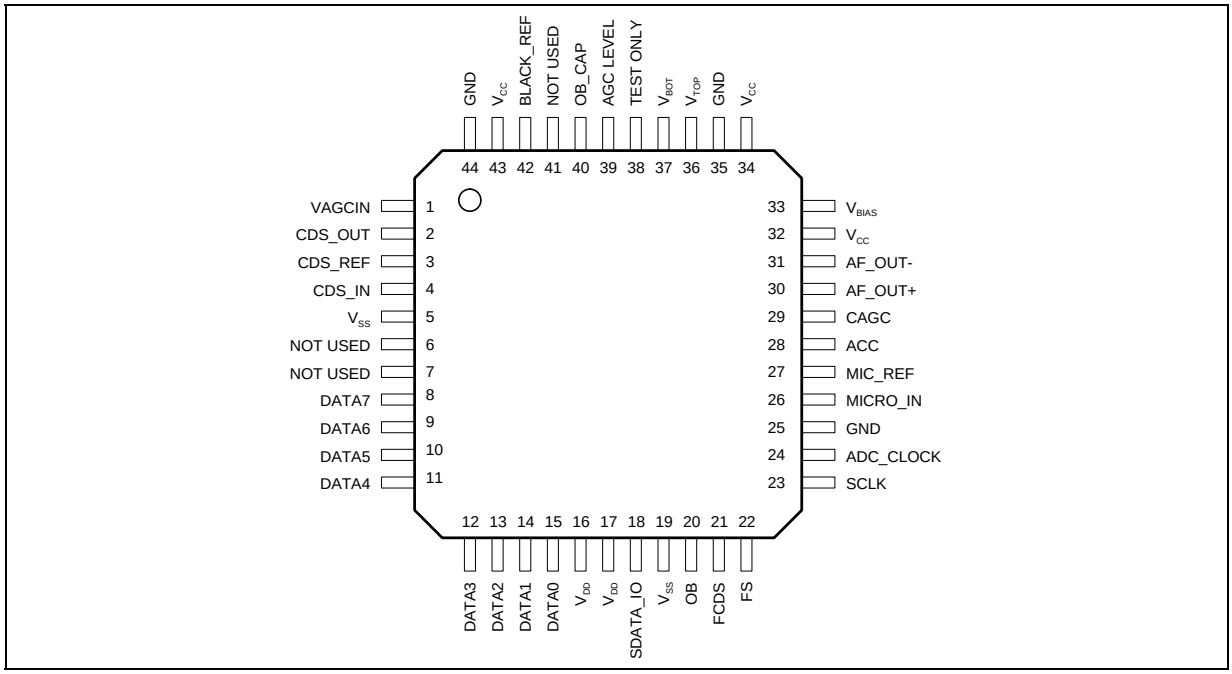
DESCRIPTION

The chip integrates the analog functions needed in a CCD Video Camera, more particularly for video-conferencing purpose.

The CCD signal is sampled, amplified to a useful level and digitized by an 8 bits ADC. The gain of the amplifier and the black level clamp can be adjusted by a serial bus.

The audio microphone preamplifier allows a microphone to be connected to the chip, which outputs a differential audio line level signal ready for digital conversion or straight amplification. The preamplifier incorporates an AGC to adapt to the income signal level. The AGC is switchable ON/OFF by the serial interface.

PIN CONNECTIONS



PINOUT DESCRIPTION

Pin	Signal	Ana./Dig.	Type	Description
1	VAGCIN	Analog	I	Video Variable Gain Input
2	CDS_OUT	Analog	O	CDS Output
3	CDS_REF	Analog	-	CDS Reference
4	CDS_IN	Analog	I	CDS Input
5	V_{SS}	Digital	-	ADC Data Ground
8	DATA[7]	Digital	O	ADC Output - MSB
9	DATA[6]	Digital	O	ADC Output
10	DATA[5]	Digital	O	ADC Output
11	DATA[4]	Digital	O	ADC Output
12	DATA[3]	Digital	O	ADC Output
13	DATA[2]	Digital	O	ADC Output
14	DATA[1]	Digital	O	ADC Output
15	DATA[0]	Digital	O	ADC Output - LSB
16	V_{DD}	Digital	-	ADC Data Supply
17	V_{DD}	Digital	-	Digital Supply
18	SDATA_IO	Digital	I/O	Serial Interface Data Wire
19	V_{SS}	Digital	-	Digital Ground
20	OB	Digital	I	OB Pulse
21	FCDS	Digital	I	FCDS Pulse
22	FS	Digital	I	FS Pulse
23	SCLK	Digital	I	Serial Bus Clock Wire
24	ADC_CLOCK	Digital	I	ADC Clock Input Pulse
25	GND	Analog	-	Microphone Ground
26	MICRO_IN	Analog	-	Microphone Input
27	MICRO-REF	Analog	-	Microphone Internal Reference
28	ACC	Analog	-	Microphone Preamplifier DC Level Capacitor
29	CAGC	Analog	-	Microphone Preamplifier AGC Capacitor
30	AF_OUT+	Analog	O	Microphone Preamplifier Output (diff. +)
31	AF_OUT-	Analog	O	Microphone Preamplifier Output (diff. -)
32	V_{CC}	Analog	-	Microphone Preamplifier Supply
33	V_{BIAS}	Analog	-	Microphone Internal Supply (regulated)
34	V_{CC}	Analog	-	ADC Supply
35	GND	Analog	-	ADC Ground
36	VTOP	Analog	-	ADC Top Reference
37	VBOT	Analog	-	ADC Bottom Reference
38	TEST ONLY	Analog	-	Test only (AGCOUT/ADCIN)
39	AGCLEVEL	Analog	-	Audio AGC Threshold Configuring Pin
40	OB_CAP	Analog	-	Black Clamp DC Loop Capacitor
42	BLACK_REF	Analog	-	Video Voltage Reference
43	V_{CC}	Analog	-	Video Supply
44	GND	Analog	-	Video Ground
6-7 41	NC NC	- -	- -	Not to be connected Not to be connected

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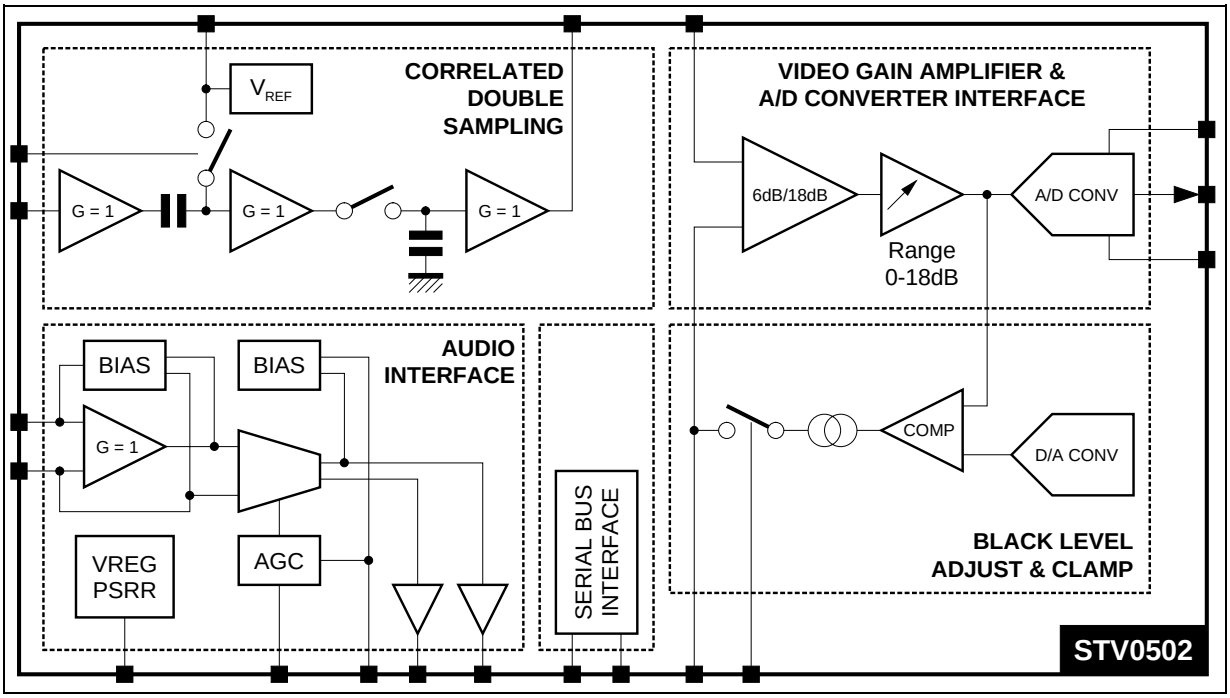
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

1 - Video Section

A CCD signal is provided to the STV0502, via a coupling capacitor, as well as the pulses FS/FCDS. The CDS (Correlated Double Sampling) is performing a clamp of the CCD signal during the FCDS pulse. The signal obtained is then sampled during the FS pulse, and held the rest of the period. The resulting signal is then the difference between the useful pixel level, and the pixel level corresponding to no charge which can vary from one pixel to another. Therefore, the parasitic level offset from one pixel to another is removed.

This signal is DC coupled to the ACG, amplified by a variable gain amplifier, bus controlled (0.07dB step), which gain is in the range +6dB to +23.7dB (17.7dB range). Typically, the amplifier is controlled in order to keep the signal at an optimum level (AGC) to be digitized. An extra 12dB can be added up via a bit of the serial interface. In this case the gain range becomes +18dB up to + 36dB.

At this point, the signal is clamped to a Black level during the OB pulse. The black level is 5 bits bus controlled, and its range corresponds to [0 LSB ; 31 LSB] of the ADC. The black level is made with a 5 bits DC frequency DAC, using the same V_{BOTTOM} and V_{TOP} voltage references than the ADC for matching purposes. The clamp is made out of a OB pulse sampled comparator between the DAC output voltage (Black) and the ADC input signal. The comparator has a symetrical current output charging a capacitor. The obtained voltage is buffered and used as a feedback to the AGC input stage. This clamp makes sure that ADCin is matched to the DAC black setting during the OB pulse, disregarding any offset in the AGC path.

Then the signal is digitized by a fast ADC, clocked at the pixel rate. The output of the chip is then an 8-bit pixel DATA, ready for digital post-processing.

2 - Audio Section

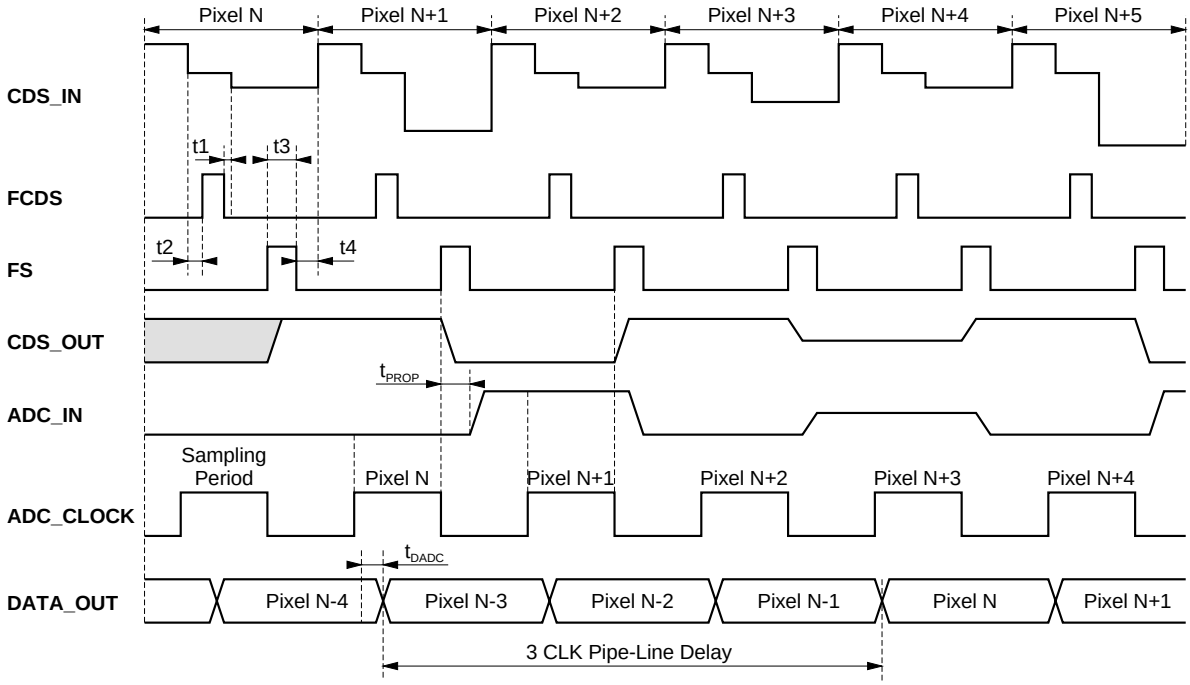
The chip integrates a high gain audio amplifier, in order to process low signals coming from a speech microphone, and provide on its output a line level, differential audio signal, for digital conversion, or power amplification. Two modes can be selected : fixed gain mode or AGC mode. In case of AGC mode, a peak detection of the signal is performed in order to regulate the output signal on a defined level of $1.5V_{PP}$ or $1V_{PP}$ (non-diff). This regulated level can be chosen at $1.5V_{PP}$ or $1V_{PP}$ thanks to a pin at respectively ground or supply voltage (a pull-up resistor to supply is already included on chip), for compatibility purposes between the 502 and various back-end chips.

The system includes a Low-Noise fixed amplifier (26dB), and a bias circuitry at the front.

FUNCTIONAL DESCRIPTION (continued)

It is followed by a Voltage Controlled Amplifier (range 8dB - 34dB), that can be switched into a fixed 26dB gain amplifier.
The VCA output is differential and 2 buffers are driving the two output pins, with a load impedance down to 5kΩ.
A bias circuitry and an external capacitor (ACC) form a DC feedback loop on the VCA DC bias, in order to correct any DC offset on the VCA output.
Finally, a peak detector (double alternance) is used to compare the output signal with the reference threshold, to be regulated at. An external capacitor (CAGC) is used for the AGC time constants. If the signal goes above the threshold, a 500µA current is charging the capacitor with a fast reponse time(attack). In case of very big signals, a second charge cureent of about 5mA is given, in order to reduce the period during which the output signal is saturated. Otherwise, a constant 1µA current discharges the capacitor with a slow response time (decay). The capacitor voltage controls the VCA gain. This constitues the AGC loop.

Figure 1



Notation : - t1 is the delay between the falling edge of FCDS and the beginning of the active pixel level from the CCD.
- t2 is the delay between the falling edge of FS and the end of the active pixel level from the CCD.

t1, t2, t3 and t4 must be kept > 0 in the Application.

- t_{PROP} is the propagation delay between CDS_OUT and ADC_IN signals (within the AGC block).
- t_{DADC} is the delay on the ADC outputs between the rising edge of the clock and data output.

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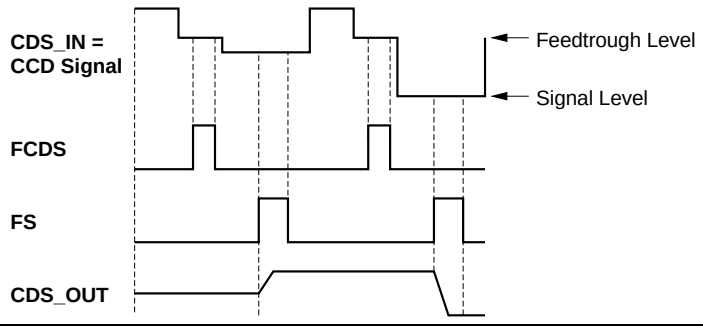
Figure 2



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FUNCTIONAL DESCRIPTION (continued)

3 - Serial Bus Specification

It is a 2-wires (data and clock) serial bus, used as a slave.

Clock line is monodirectional (input) and allways sent by the master to the chip, whereas Data line is bidirectional (I/O).

There are 3 registers (8 bits), both writable/readable.

Each register can be addressed by a 4 bits address word, followed by a R/W bit, and an 8 bits word Data (read/write).

2 main patterns can be sent : Reset Pattern and Read/Write pattern.

3.1 -Timings and Protocol

The data bit is taken into account when the clock is rising.

- Reset Pattern : resets all the registers to their default (Power On) values :
  format = 16 * (data=1) | 2 * (data=0)
  (total = 18 clocks)
- Read/Write Pattern :
  format = 4 addr bits | R/W bit | 8 data bits
  (total = 13 clocks)

Please note that :

1/ On power On conditions, SDATA line is in Write (Input) Mode.

2/ In case of a read pattern, the SDATA line is automatically set to Read (Output mode) during 8 clock cycles (Data D7 - D0) after R/W bit has been sent, and comes back in Write (Input mode) after the 13th clock cycle.

3/ There is no timing restriction between two consecutive patterns (a pattern being defined as one of the two above).

3.2 - Register Summary

Register	Address (A3-A0)	Data Format (D7-D0)
Video Amplifier Gain	0000	DDDD.DDDD
Black Level Adjust	0001	XXXD.DDDD
Video High Gain Select	0001	XXDX.XXXX
Test Mode	0001	DDXX.XXXX
Microphone AGC	0010	XXXX.XXXD

X : unused bits
D : means useful bits

Please note that 3 different functions are merged in register address 01.

Figure 3

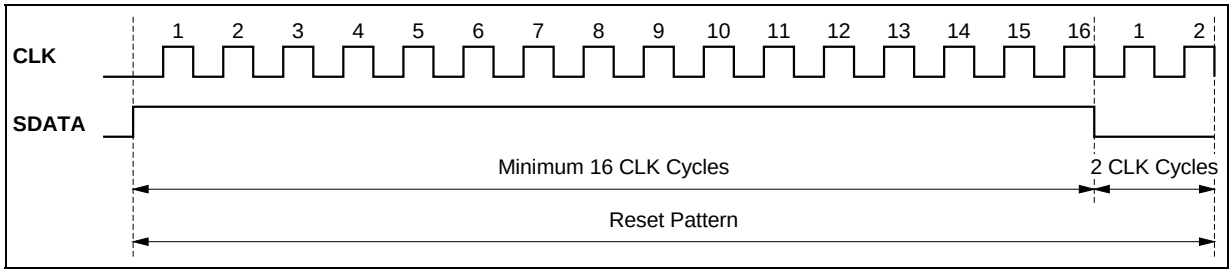
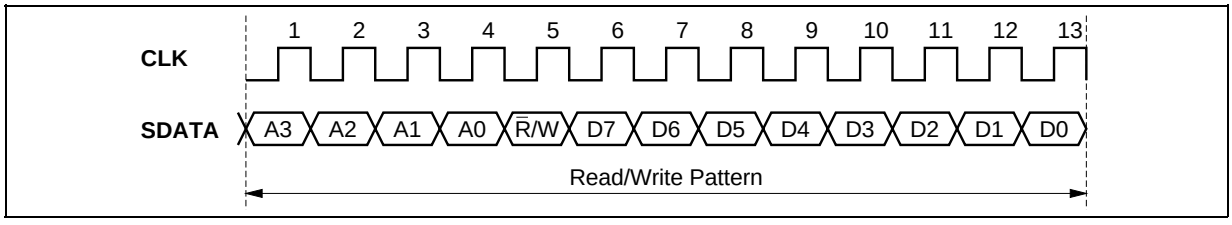


Figure 4



FUNCTIONAL DESCRIPTION (continued)

3.3 - Control Data

Video Amplifier Gain Control *(8 bits used)*

Address : 0000
POR value : 0000.0000 ---> 6dB

Gain is expressed from CDSoutput to ADC input (ADC range 1.55V_{PP})
- 0.07dB / LSB step
- Overall range (256 steps) : 17.7dB

Video Gain (dB)	Data
6	0000.0000
6.07	0000.0001
6.14	0000.0010
...	...
7.12	0001.0000
7.19	0001.0001
...	...
23.63	1111.1110
23.7	1111.1111

Black Level Adjustment Control *(5 bits used)*

Address : 0001
POR Value : 0001.0000 ---> 16LSB

The adjustment is controlling the black reference voltage. However, it is preferred to express the Black level adjustment in terms of the ADC output code variation (in ADC LSBs, compared to the nominal default setting) depending on the Black setting.

Typically, 16 LSBs black level is recommended.
- 1 ADC LSBs / LSB step
- Overall range : 31 ADC LSBs

Black Level (ADC Ouput Variation)	Data
0 LSBs	XXX0.0000
1 LSBs	XXX0.0001
...	...
30 LSBs	XXX1.1110
31 LSBs	XXX1.1111

Video High Gain Select *(1 bit used)*

Address : 0001
POR Value : 0 ---> Nominal gain

This bit controls an extra 12dB gain in the video path (adding to gain described in previous page).

Video High Gain Select	Data
Nominal Gain	XX0X.XXXX
Extra 12dB Gain	XX1X.XXXX

Video AGCOUT Test Signal ON/OFF *(2 bits used)*

Address : 0001
POR Value : 00 ---> High Z pad

A pin is reserved to output the ADC input signal, or input the ADC input signal for test and evaluation purpose.

Those bits control the state of the output buffer. To limit Xtalk and pollutions, the buffer is in High impedance mode during normal operation.

VAGCOUT PIn State	Data
Normal Operation (High Z Pin)	00XX.XXXX
AGC Output Test	10XX.XXXX
ADC Input Test	11XX.XXXX

Microphone AGC Switch *(1 bit used)*

Address : 0010
POR value : 0000.0000 ---> AGC OFF

The switch is controlling the state of the AGC : ON or OFF.

In OFF mode, the Micro Preamp. is set at a fixed nominal gain of 52dB.

In ON mode, the AGC is operating in a gain range [34dB ; 60dB] (see further in this document for details).

Microphone AGC	Data
OFF	0000.0000
ON	0000.0001

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}, V_{CC}	Supply Voltage	-0.5, 7	V
V_I	Digital Input Pin Voltage	-0.5, V_{DD} + 0.5	V
I_I	Digital Input Pin Current	1.6	mA
T_{stg}	Storage Temperature	+80	°C
T_{oper}	Operating Temperature	0, +70	°C
T_{lead}	Lead Temperature (10s Max.)	+260	°C

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ESD : The STV0502 withstands 2kV in Human Body Model and 100V in Machine Model for all Pins versus V_{DD} and V_{SS}.

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-ambient Thermal Resistance	Max.	65	°C/W

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ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C, V_{DD} = V_{CC} = 5V, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_{CC}, V_{DD}	All Supplies		4.5	5	5.5	V
I_{SUP}	Total Current Consumption	V_{CC} = V_{DD} = 5V	40	55	70	mA
CMOS DIGITAL INPUTS						
V_{IL} V_{IH}	Low Level Input Voltage High Level Input Voltage		 0.7 V_{DD}		0.3 V_{DD}	V V
I_{IL} I_{IH}	Low Level Input Current High Level Input Current				-1.0 1.0	µA µA
CMOS DIGITAL OUTPUTS (4mA drivers)						
V_{OL} V_{OH}	Low Level Output Voltage High Level Output Voltage		 2.4		0.4	V V
I_{OL} I_{OH}	Low Level Output Current High Level Output Current				4.0 -4.0	mA mA
SERIAL INTERFACE						
Slevel	SDATA, SCLK Levels		CMOS			V
f_{CLK}	Bus Clock Frequency			0.5	1	MHz
DutyC	Clock Duty Cycle	SCLK	40	50	60	%
t_{DR}	Delay between CLK Rising Edge and Data Out	Read Mode, see Figure 5	300	500	700	ns
t_{DW}	Delay between CLK Rising Edge and Data In	Write Mode, see Figure 5	300	500	700	ns
t_R	Clock Rise Time	SCLK			200	ns
t_F	Clock Fall Time	SCLK			200	ns

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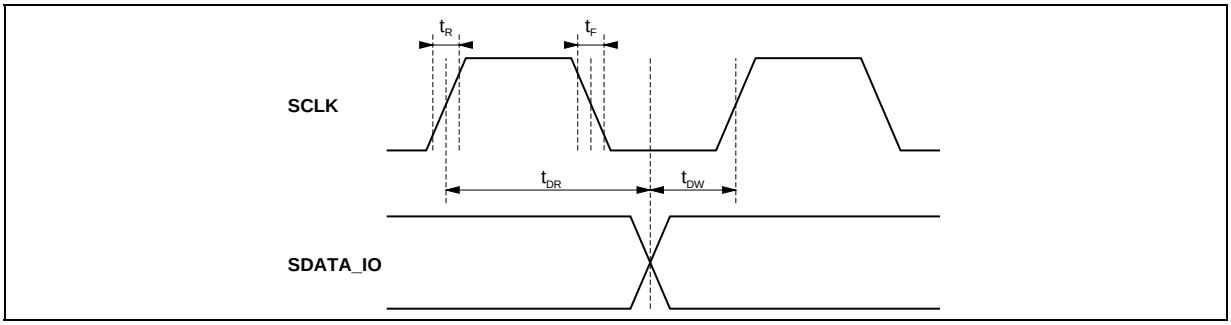
Figure 5



0502-07.EPS

ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C, V_{DD} = V_{CC} = 5V, unless otherwise specified (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VIDEO CDS						
R_{IN}	Input Resistance	Pin 4	8	11	14	kΩ
C_{IN}	Input Capacitance	Pin 4		6		pF
INDyn	Input Dynamic Range	Pin 4, before output clipping	0.6	0.7		V_{PP}
CDS_SR	S/H Slew Rate	Pin 2, FS high	0.6	0.9		V/15ns
CDS_DR	S/H Droop Rate	Pin 2, FS low	-20		+20	mV/µs
CDS_HM	S/H Hold Mode Feed through	Pin 2, FS low, f_{IN} = 1MHz		-55	-45	dB
CDS_lin	CDS Linearity	Pin 2, 500mV_{PP} (1)		0.3	1.5	%
CDS Gain	Overall Input to Output Gain	Pin 2, normal operation	-2	-1	0	dB
R_{OUT}	CDS Output Impedance	Pin 2, FCDS & FS high			250	Ω
OUTload	CDS Ouput Load		100			Ω
FS	PS Pulse Width	See timings	12			ns
FCDS	FSDS Pulse Width	See timings	12			ns
PIX_FRE	Pixel Rate	Pins 4, 21, 22	6	12		MHz
PSRR	Power Supply Rejection	Measured on Pin 2 (2)		60		dB
VIDEO AMPLIFIER						
R_{IN}	Input Resistance	Pin 1		2		kΩ
C_{IN}	Input Capacitance	Serial bus from H00 to HFF		18		pF
Min. Gain Max. Gain	Minimum Gain Maximum Gain	Serial bus = H00/no extra gain Serial bus = HFF/no extra gain	 23.2	6 23.7	6.5	dB dB
Min. Gain Max. Gain	Minimum Gain Maximum Gain	Serial bus = H00/extra gain Serial bus = HFF/extra gain	 35.2	12 35.7	12.5	dB dB
Gset-err	Gain Setting Relative Error	Serial bus from H00 to HFF	-0.5		0.5	dB
Out_Max	Max. Output Signal before clipping	Pin 38, V_{CC} = 4.5V G = 6dB, V_{IN} = 0.8V_{PP} G = 23.7dB, V_{IN} = 0.1V_{PP}		 1.6 1.6		 V_{PP} V_{PP}
t_R	Output Rise Time	Square input		10	15	ns
t_F	Output Fall Time	Square input		10	15	ns
t_{PROP}	AGC Propagation Time	Pin 1 to Pin 38		15	20	ns
PSRR	Power Supply Rejection	Measured on Pin 38 (2)		45		dB
Xtalk	Xtalk from Video to Audio	Measured on Pin 38, compared to Pins 20 and 21 (2)		60		dB

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Notes : 1. Normal operation means FS & FCDS run at specified timings and 12MHz frequency.
2. On a 20Hz to 10MHz frequency range, with 10µF filtering capacitors on all supplies, and well splitted supplies and grounds.

ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C, V_{DD} = V_{CC} = 5V, unless otherwise specified (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
8 BITS ADC & OB CLAMP						
OB_rise	OB High Time Constant	Pin 38, OB 0 to 1	4			mV/µs
OB_decay	OB Low Time Constant	Pin 38, OB 1 to 0			-2	mV/ms
BLK_RAN	Black Level Adjust Range	Pins 8 to 15, OB high, Serial bus from H00 to H1F		31		LSBs
BLK_res	Black Level Adjust Resolution	Pins 8 to 15, per serial bus LSB step		1		LSBs
BLK_LEV	Black Level Adjust	Pins 8 to 15 Bus = H00 Bus = H1F	 29	 0 31	 2 33	 LSBs LSBs
ADC_DN	ADC Input Dynamic Range (output from 0 to 255)	Pin 38 test signal above black clamping level (V_{BOT})	1.4	1.55	1.7	V_{PP}
f_{CLK}	ADC Clock Frequency	Pin 24		12		MHz
t_{PCLK}	Output Pipeline Delay (3)	From a sampling to data out	3		3	CLK cycles
t_{DADC}	Clock to Data Out (4)	CLK positive edge, C_{LOAD} = 20pF		17		ns
R_{LADD}	Ladder Resistance	Between Pins 36 and 37		330		Ω
V_{TOP}	Top Reference Voltage	Pin 36	3.2	3.35	3.5	V
V_{BOT}	Bottom Reference Voltage	Pin 37	1.71	1.8	1.89	V
ADC_lin	ADC Linearity	Data out, input signal between [V_{BOT} + 25mV ; V_{TOP} - 25mV]			1	%

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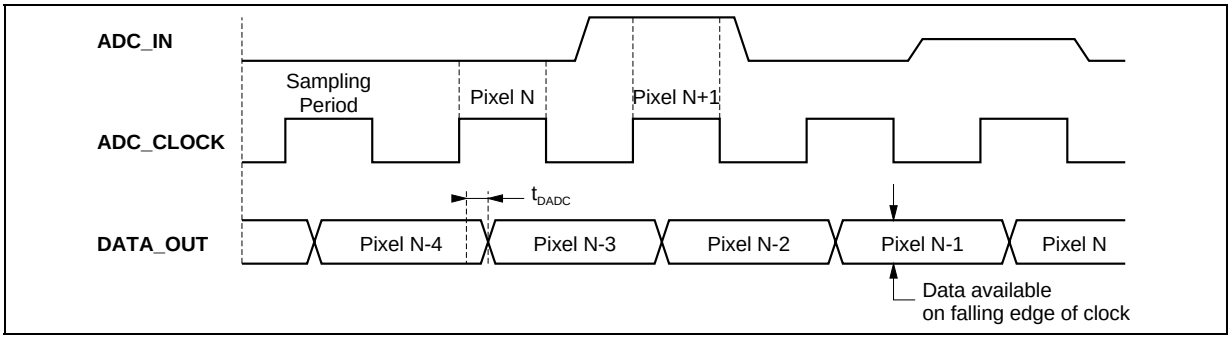
Notes : 3. The signal is being sampled as long as ADC_CLK is high.
4. See Figure 6 for data reading timing constraint.

Figure 6



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Due to t_{DADC}, and to make sure the data are read when they are stable, please read the data on the falling edge of the ADC clock.

ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C, V_{DD} = V_{CC} = 5V, unless otherwise specified (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
MICROPHONE PREAMPLIFIER						
V_{BIAS}	Bias Audio Voltage	Pin 26		3.8		V
IN_ref	Micro Input Voltage	Pin 33		2		V
R_{IN}	Input Impedance	Pin 33		50		kΩ
G_{FIX}	Overall Gain	AGC Mode off	48	50	52	dB
G_{AGC}	Overall Gain	AGC Mode on V_{AGC} = 0.5V V_{AGC} = 4V	54	56 20	58 34	dB dB
ALC1 ALC2	Regulated Output Level	On Pins 30/31, AGC on, Input = [1.5mV_{PP} ; 30mV_{PP}] AGClevel (Pin 39) = 0 AGClevel (Pin 39) = 5	1.1 0.7	1.5 1	1.9 1.3	V_{PP} V_{PP}
Ich	AGC Charge Current	On Pin 29 when signal out above threshold		500		µA
Idis	AGC Discharge Current	All the time with AGC on		-1		µA
t_{ATT}	Output Response Time	Step +6dB, C_{AGC} = 2.2µF		5		ms
t_{DEC}	Output Response Time	Step -6dB, C_{AGC} = 2.2µF		2.5		s
OUT_Max	Output Clipping Level	Pins 30/31 AGC off : V_{IN} = 5mV_{PP} AGC on : V_{IN} > 40mV_{PP}	1.7 1.7	2 2		V_{PP} V_{PP}
OUT_DC	Output DC Voltage	Pins 30/31		2.1		V
OUT_OF	Channel DC Mismatch	Pins 30/31	-350	0	350	mV
R_{OUT}	Output Impedance	Pins 30/31		100		Ω
THD	Overall THD	1V_{PP} out, 1kHz signal, BW 15kHz		0.15	0.4	%
PSRR	PSRR from V_{CC}	f = 1kHz, V_{CC} + sine 100mV_{PP} (2)		60		dB
CMRR	CMRR from V_{CC}	f = 1kHz, V_{CC} + sine 100mV_{PP} (2)		60		dB
LFc	Low Cut-off Frequency	C_{IN} = 2.2µF, C_{ACC} = 10µF			250	Hz
HFc	High Cut-off Frequency	C_{IN} = 2.2µF, C_{ACC} = 10µF	20			kHz
Xtalk	Xtalk from video to audio	Measure on Pins 30/31, compared to Pin 38 (2)		60		dB

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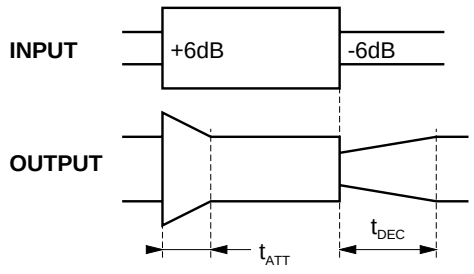
Notes : 2. On a 20Hz to 10MHz frequency range, with 10µF filtering capacitors on all supplies, and well splitted supplies and grounds.

Figure 7



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I/O DIAGRAMS

Figure 8 : VAGCIN

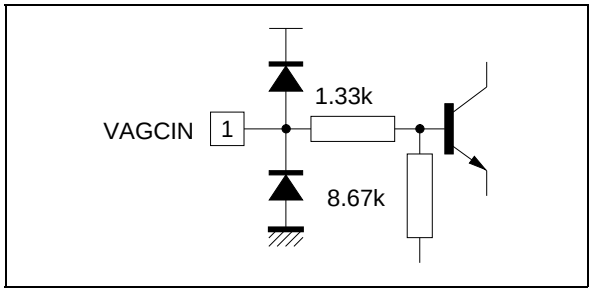


Figure 9 : CDS_OUT

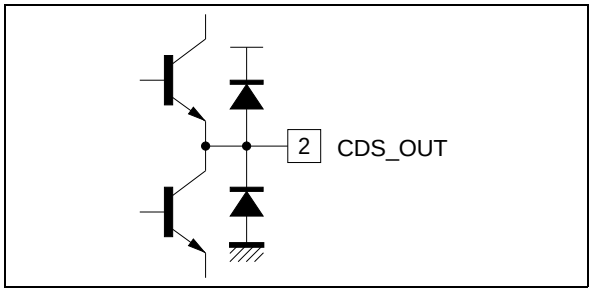


Figure 10 : CDS_REF

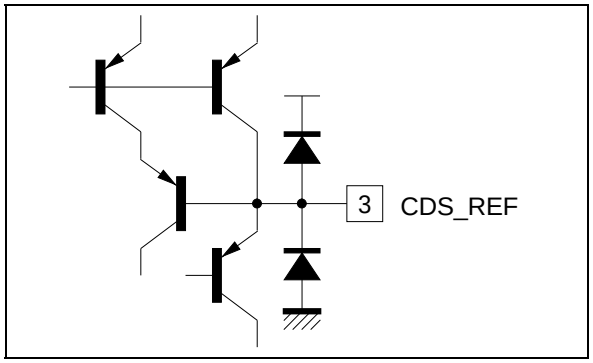


Figure 11 : CDS_IN

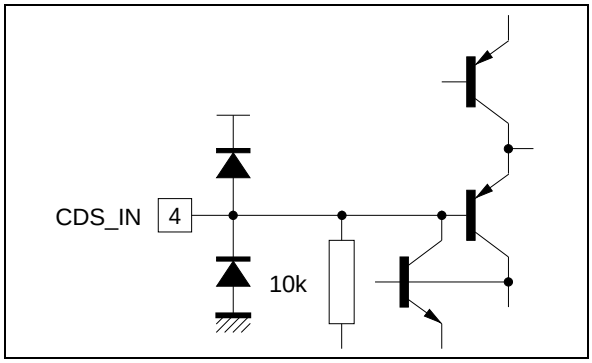


Figure 12 : DATA[7:0]

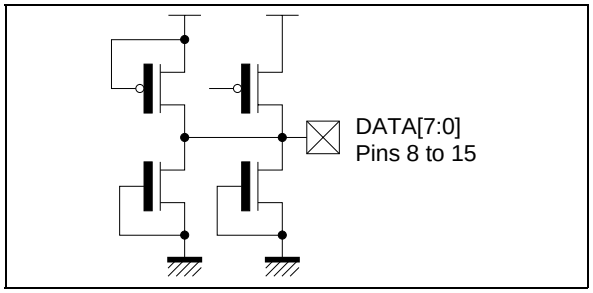


Figure 13 : SDATA_IO

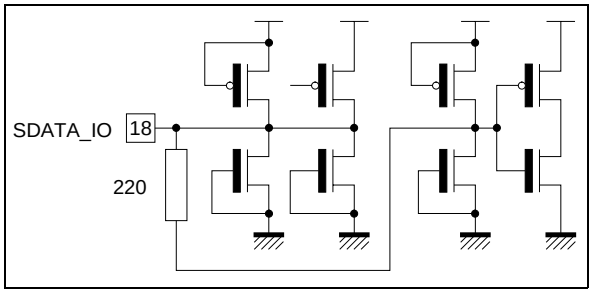


Figure 14 : OB, FCDS, FS, SCLK, ADC_CLOCK

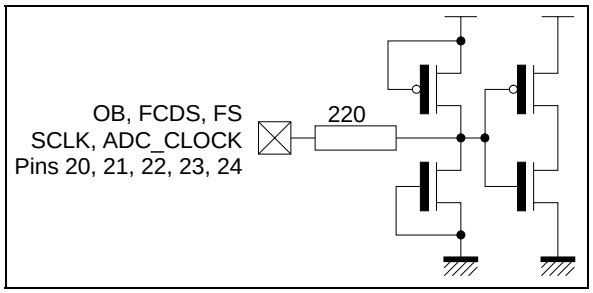
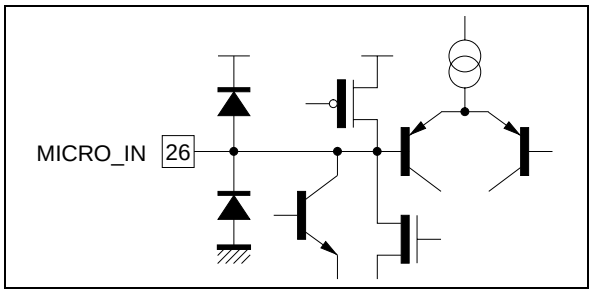


Figure 15 : MICRO_IN



I/O DIAGRAMS (continued)

Figure 16 : MIC_REF

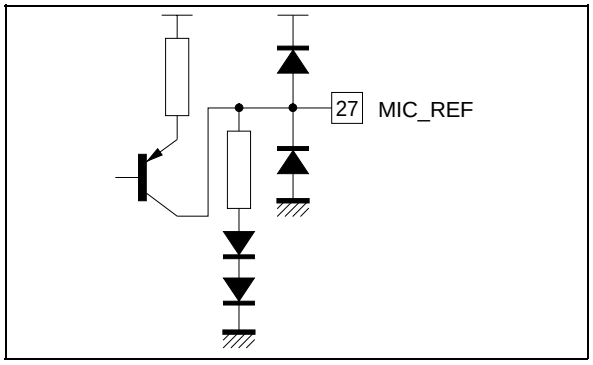


Figure 17 : ACC

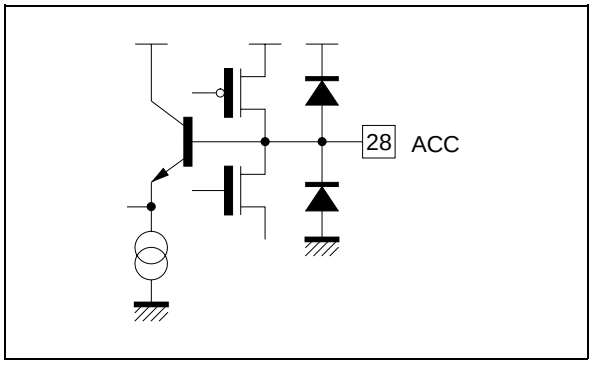


Figure 18 : CAGC

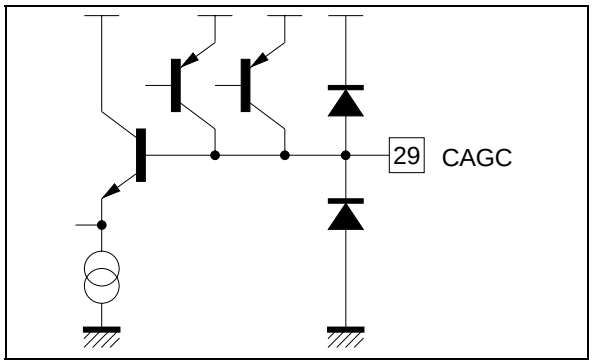


Figure 19 : AF_OUT+, AF_OUT-

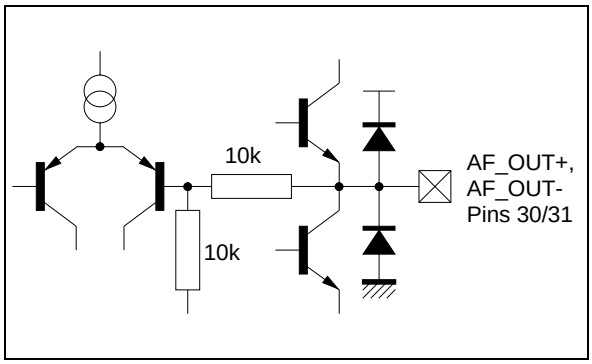


Figure 20 : V_{BIAS}

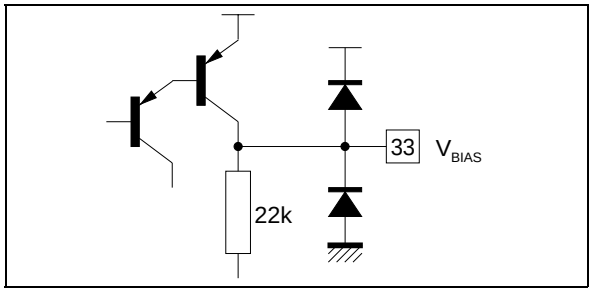


Figure 21 : V_{TOP}

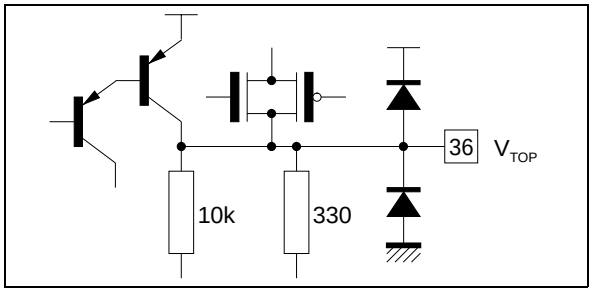


Figure 22 : V_{BOT}

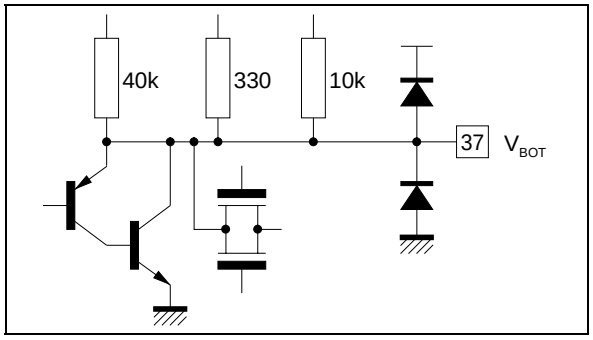
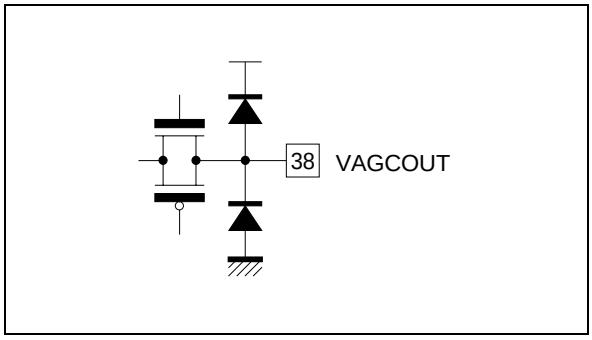


Figure 23 : VAGCOUT



I/O DIAGRAMS (continued)

Figure 24 : AGCLEVEL

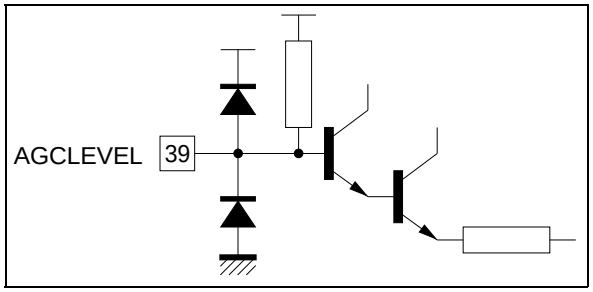


Figure 25 : OB_CAP

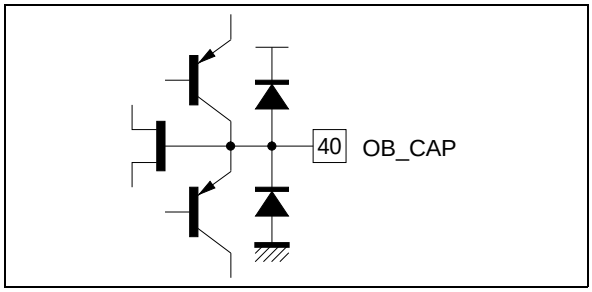
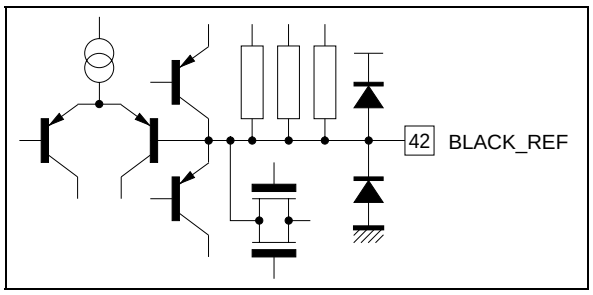
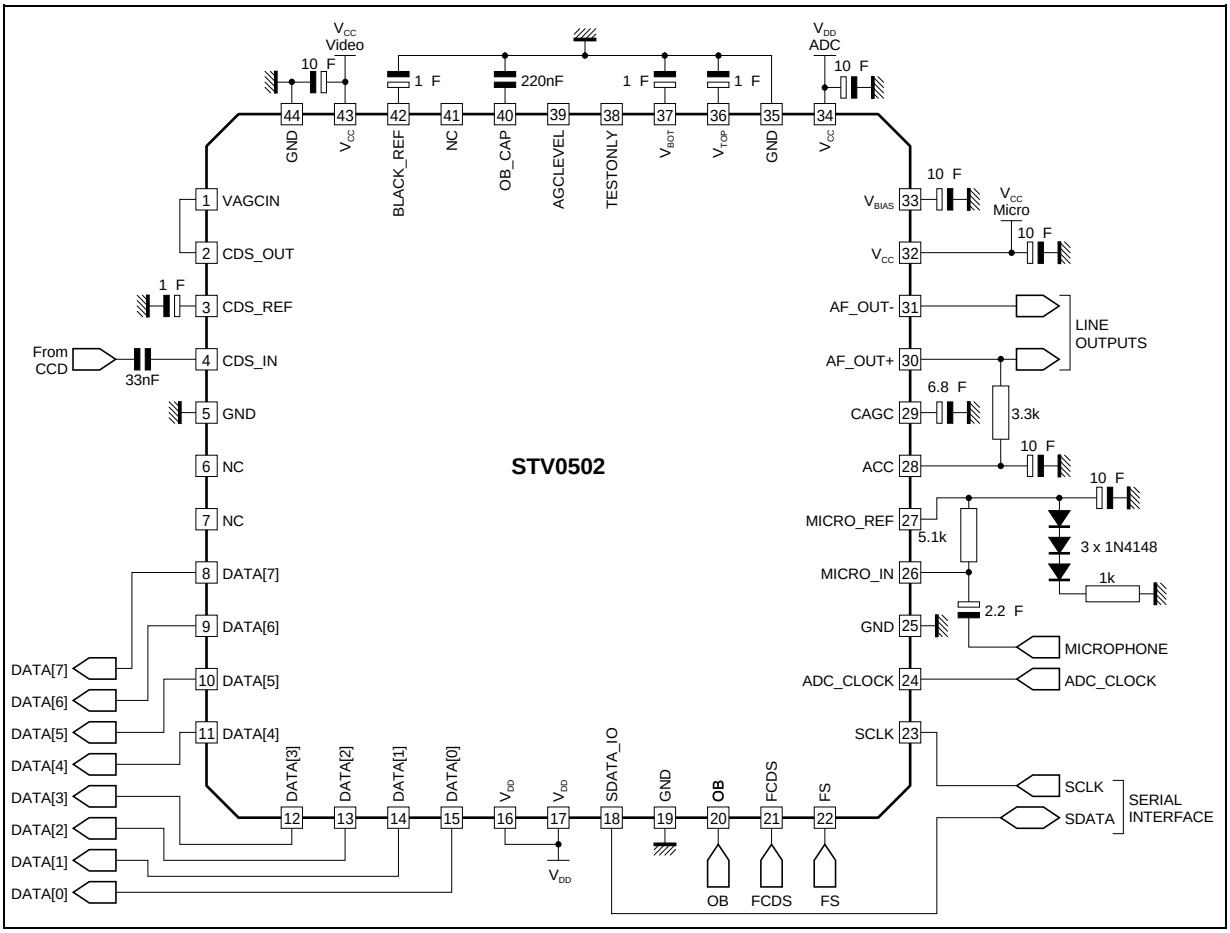


Figure 26 : BLACK_REF

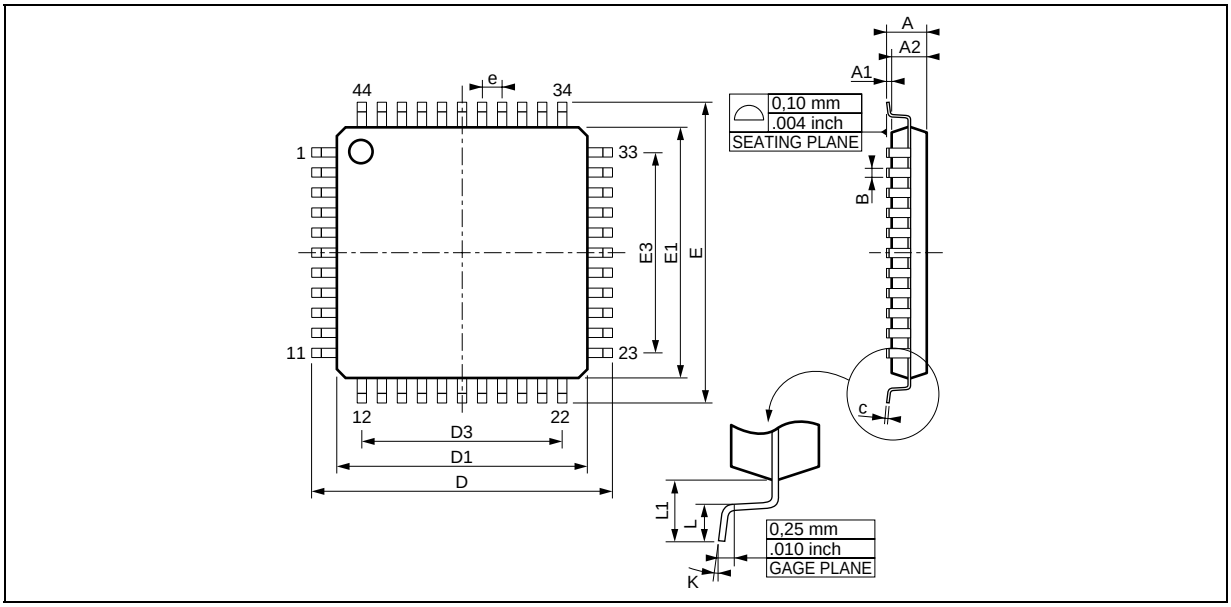


TYPICAL APPLICATION



PACKAGE MECHANICAL DATA

44 PINS - FULL PLASTIC QUAD FLAT PACK (THIN) (TQFP)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.40	0.012	0.015	0.016
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0^o (Min.), 7^o (Max.)					

4Y.TBL