



# STY100NS20FD

## N-CHANNEL 200V - 0.022Ω - 100A Max247 MESH OVERLAY™ Power MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STY100NS20FD	200V	< 0.024Ω	100 A

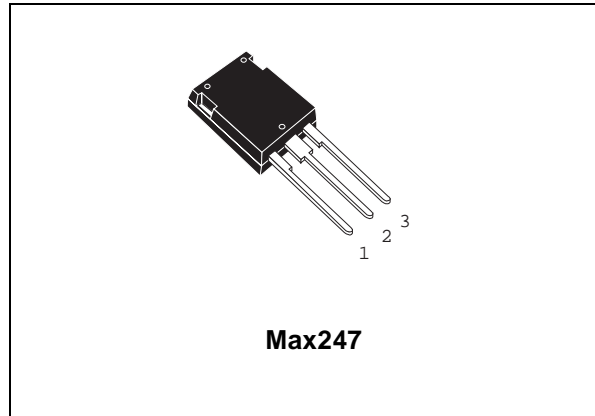
- TYPICAL R<sub>DS(on)</sub> = 0.022Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- ± 20V GATE TO SOURCE VOLTAGE RATING
- LOW INTRINSIC CAPACITANCE
- FAST BODY-DRAIN DIODE: LOW t<sub>rr</sub>, Q<sub>rr</sub>

### DESCRIPTION

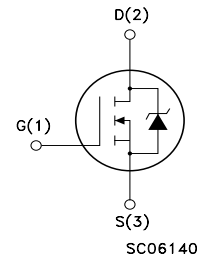
Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patented STrip layout coupled with the Company's proprietary edge termination structure, gives the lowest R<sub>DS(ON)</sub> per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLY (SMPS)
- DC-AC CONVERTER FOR WELDING EQUIPMENT AND UNINTERRUPTABLE POWER SUPPLY AND MOTOR DRIVE



### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	200	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	200	V
V <sub>GS</sub>	Gate- source Voltage	±20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	100	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	63	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	400	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	450	W
	Derating Factor	3.6	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	25	V/ns
T <sub>stg</sub>	Storage Temperature	-65 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area

(1)I<sub>SD</sub> ≤ 100A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>

## STY100NS20FD

### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	0.277	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	30	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose		300	°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	100	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	750	mJ

### ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

#### OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	200			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			10 100	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20V			±100	nA

#### ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3	4	5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 50A		0.022	0.024	Ω

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 50A		30		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		7900		pF
C <sub>OSS</sub>	Output Capacitance			1500		pF
C <sub>rSS</sub>	Reverse Transfer Capacitance			460		pF

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

**ELECTRICAL CHARACTERISTICS (CONTINUED)**  
SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 100V, I_D = 50A$		42		ns
$t_r$	Rise Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		140		ns
$Q_g$	Total Gate Charge	$V_{DD} = 100V, I_D = 100A,$		360		nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = 10V$		35		nC
$Q_{gd}$	Gate-Drain Charge			135		nC

SWITCHING OFF

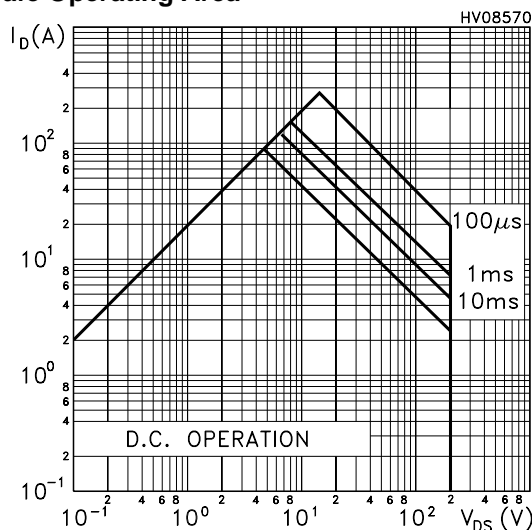
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 100V, I_D = 100A,$		245		ns
$t_f$	Fall Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		140		ns
$t_c$	Cross-over Time			220		ns

SOURCE DRAIN DIODE

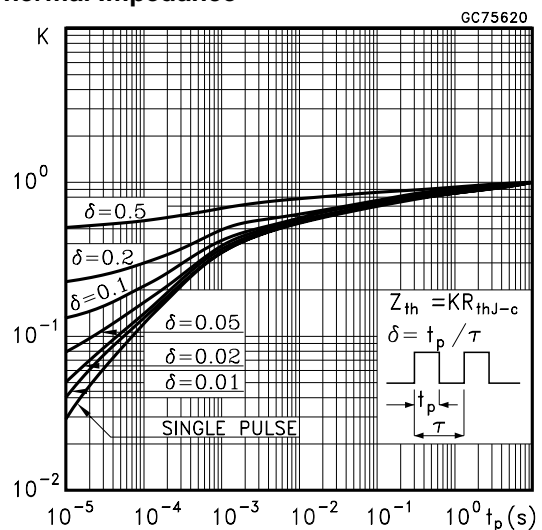
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				100	A
$I_{SDM} (2)$	Source-drain Current (pulsed)				400	A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 100A, V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 100A, di/dt = 100A/\mu s,$		225		ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 160V, T_j = 150^\circ C$ (see test circuit, Figure 5)		1.35		$\mu C$
$I_{RRM}$	Reverse Recovery Current			12		A

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.

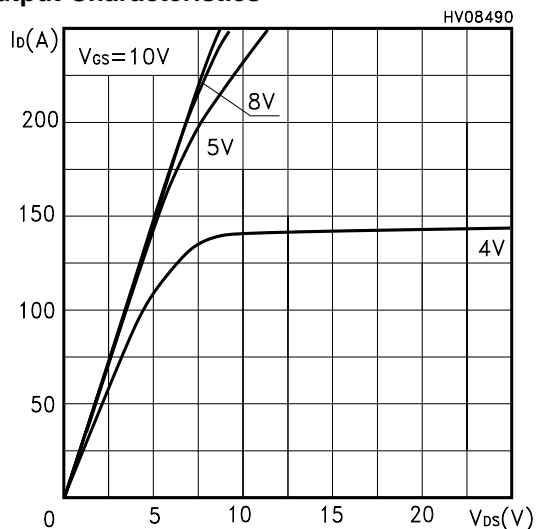
Safe Operating Area



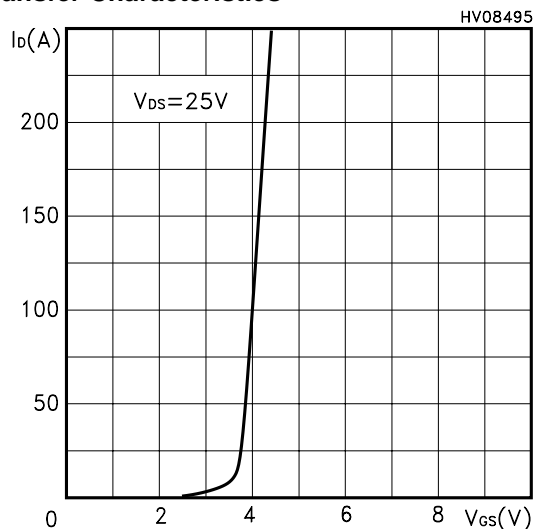
Thermal Impedance



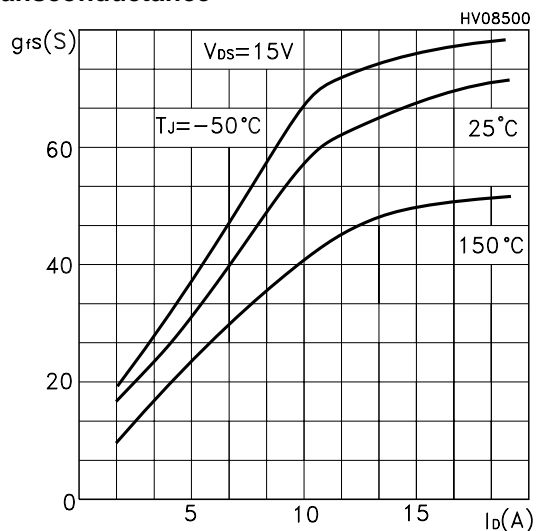
Output Characteristics



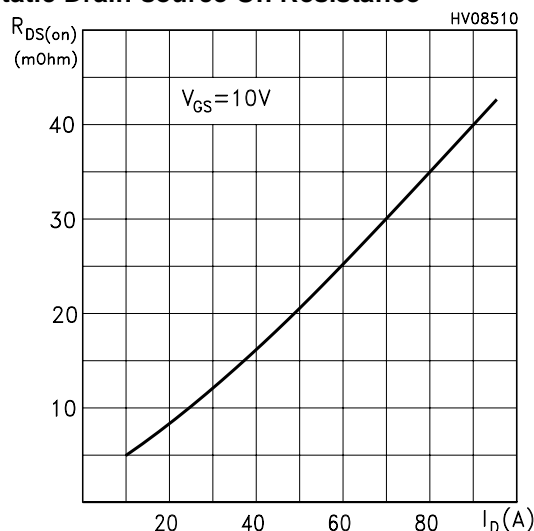
Transfer Characteristics



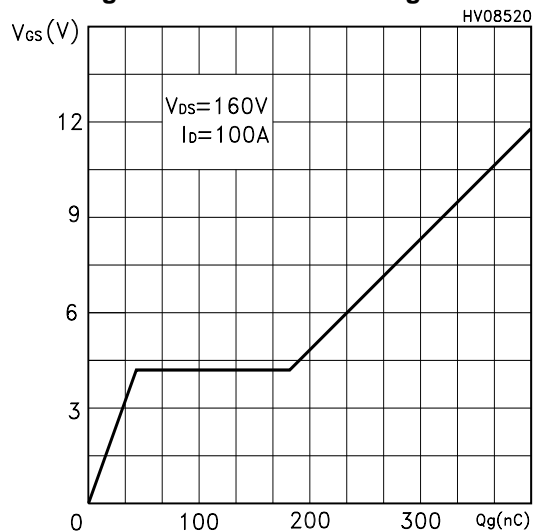
Transconductance



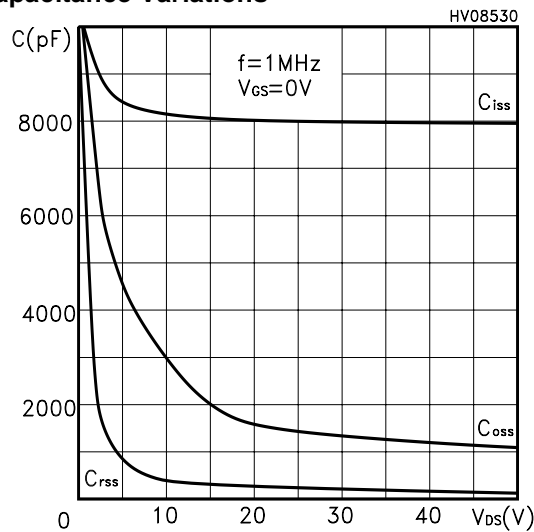
Static Drain-source On Resistance



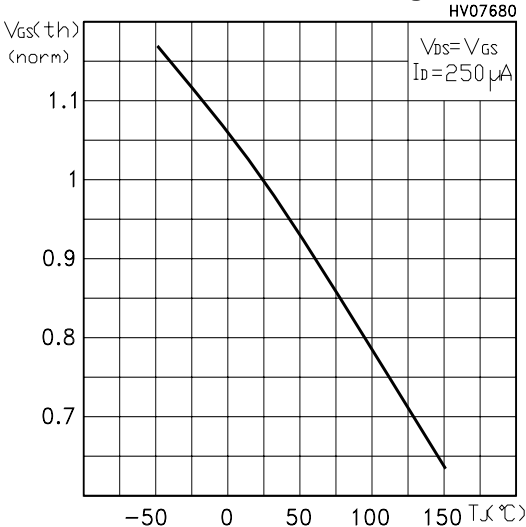
Gate Charge vs Gate-source Voltage



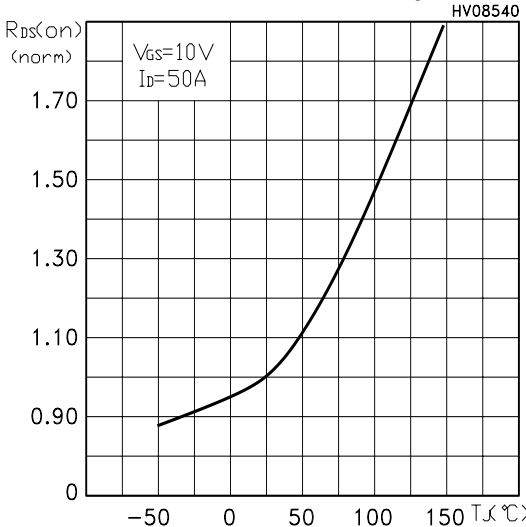
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

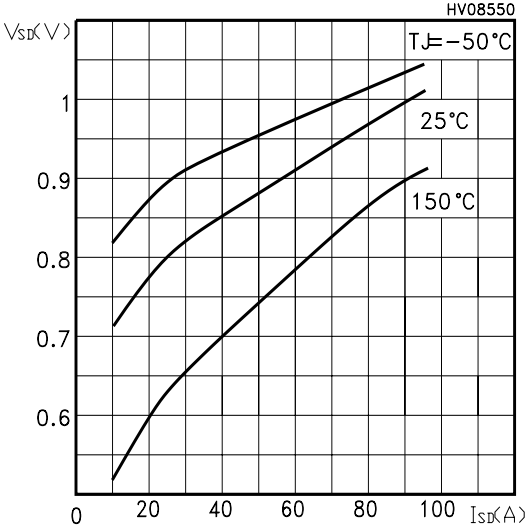


Fig. 1: Unclamped Inductive Load Test Circuit

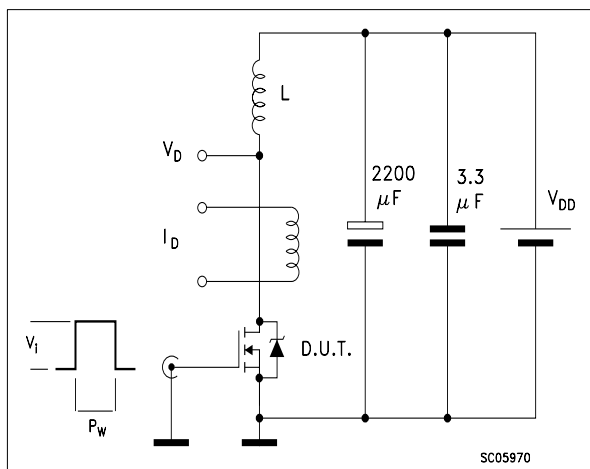


Fig. 2: Unclamped Inductive Waveform



Fig. 3: Switching Times Test Circuit For Resistive Load

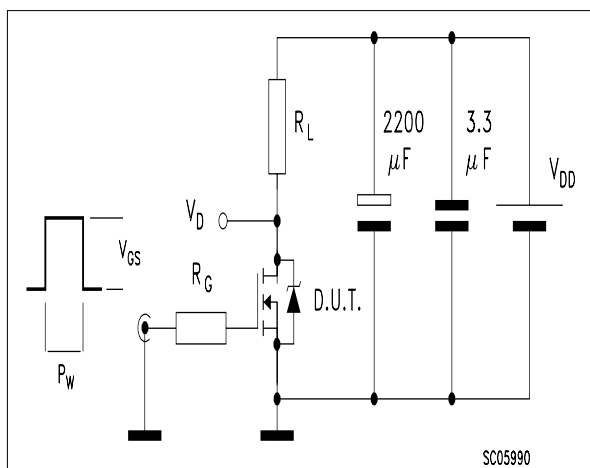
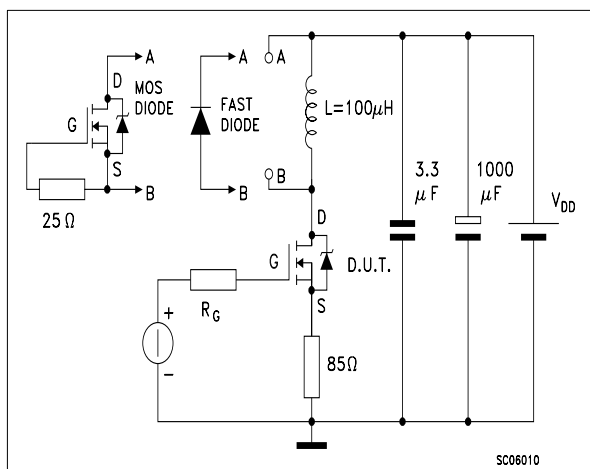


Fig. 4: Gate Charge test Circuit

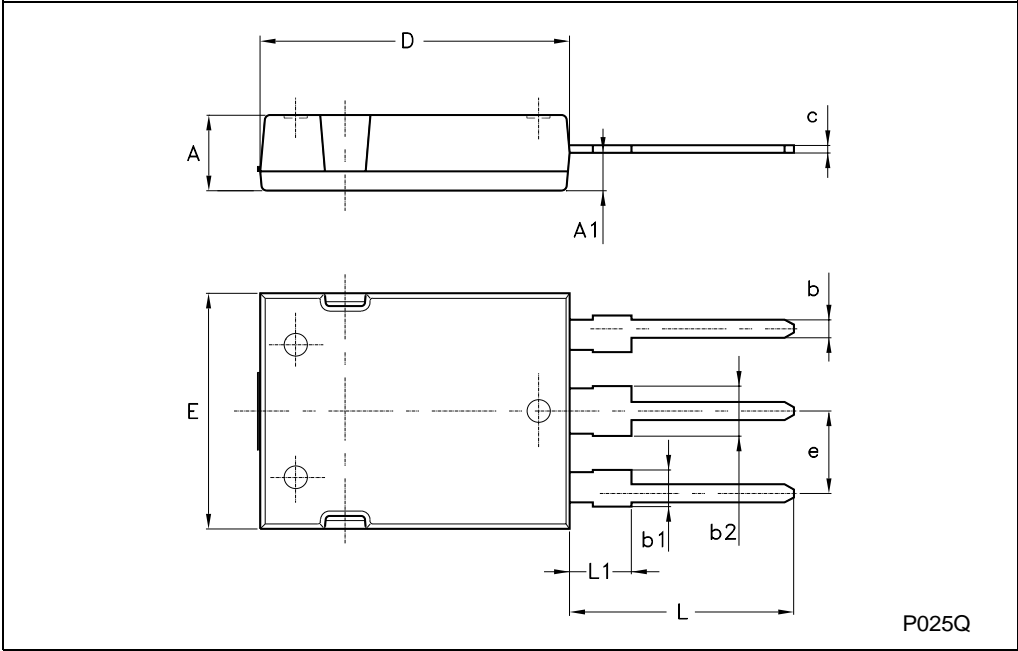


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



**Max247 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.70		5.30			
A1	2.20		2.60			
b	1.00		1.40			
b1	2.00		2.40			
b2	3.00		3.40			
c	0.40		0.80			
D	19.70		20.30			
e	5.35		5.55			
E	15.30		15.90			
L	14.20		15.20			
L1	3.70		4.30			



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2000 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -  
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>