



## N-Channel 20-V (D-S) 175°C MOSFET

PRODUCT SUMMARY			
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ)
20	0.012 @ $V_{GS} = 10$ V	40 <sup>a</sup>	7.5
	0.026 @ $V_{GS} = 4.5$ V	40 <sup>a</sup>	

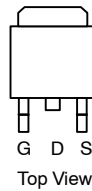
### FEATURES

- TrenchFET® Power MOSFET
- 175°C Junction Temperature
- Optimized for High-Side Synchronous Rectifier
- 100%  $R_g$  Tested

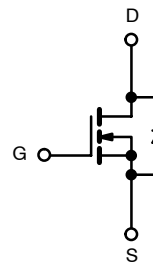
### APPLICATIONS

- Desktop or Server CPU Core
- Game Station

TO-263



DRAIN connected to TAB



N-Channel MOSFET

Ordering Information: SUM40N02-12P  
SUM40N02-12P—E3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175^\circ\text{C}$ )	$I_D$	$T_C = 25^\circ\text{C}$	40 <sup>a</sup>
		$T_C = 100^\circ\text{C}$	40 <sup>a</sup>
Pulsed Drain Current	$I_{DM}$	90	A
Maximum Power Dissipation <sup>b</sup>	$P_D$	$T_C = 25^\circ\text{C}$	83 <sup>c</sup>
		$T_A = 25^\circ\text{C}$ <sup>d</sup>	3.75
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mounted) <sup>d</sup>	$R_{thJA}$	40	$^\circ\text{C/W}$
Junction-to-Case	$R_{thJC}$	1.8	

Notes

- Package limited.
- Duty cycle  $\leq 1\%$ .
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).



SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>DS</sub> = 0 V, I <sub>D</sub> = 250 μA	20			V
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	0.85	2	3	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	90			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0095	0.012	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C			0.0175	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C			0.022	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A		0.021	0.026	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A	10			S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 10 V, f = 1 MHz		1000		pF
Output Capacitance	C <sub>oss</sub>			370		
Reverse Transfer Capacitance	C <sub>rss</sub>			180		
Total Gate Charge <sup>b</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 40 A		7.5	12	nC
Gate-Source Charge <sup>b</sup>	Q <sub>gs</sub>			3.5		
Gate-Drain Charge <sup>b</sup>	Q <sub>gd</sub>			2.6		
Gate Resistance	R <sub>g</sub>		1.5	3.0	5.1	Ω
Turn-On Delay Time <sup>b</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 10 V, R <sub>L</sub> = 0.25 Ω I <sub>D</sub> ≅ 40 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 2.5 Ω		11	20	ns
Rise Time <sup>b</sup>	t <sub>r</sub>			10	15	
Turn-Off Delay Time <sup>b</sup>	t <sub>d(off)</sub>			24	35	
Fall Time <sup>b</sup>	t <sub>f</sub>			9	15	
<b>Source-Drain Diode Ratings and Characteristics (T<sub>C</sub> = 25 °C)<sup>c</sup></b>						
Continuous Current	I <sub>S</sub>				40	A
Pulsed Current	I <sub>SM</sub>				90	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0 V		1.1	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 40 A, di/dt = 100 A/μs		20	40	ns
Peak Reverse Recovery Current	I <sub>RM</sub>			0.7	1.1	A
Reverse Recovery Charge	Q <sub>rr</sub>			0.007	0.022	μC

Notes

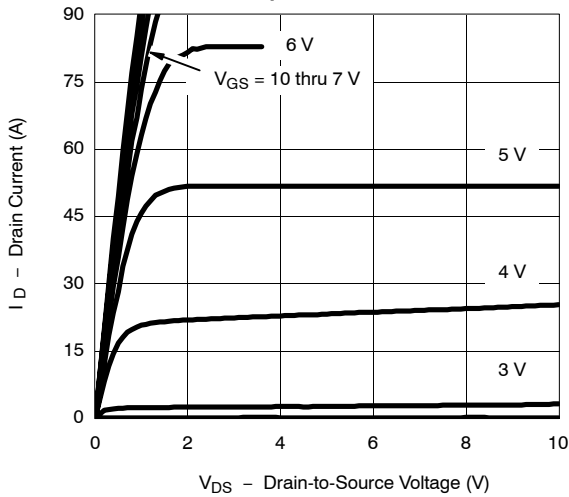
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Independent of operating temperature.
- c. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

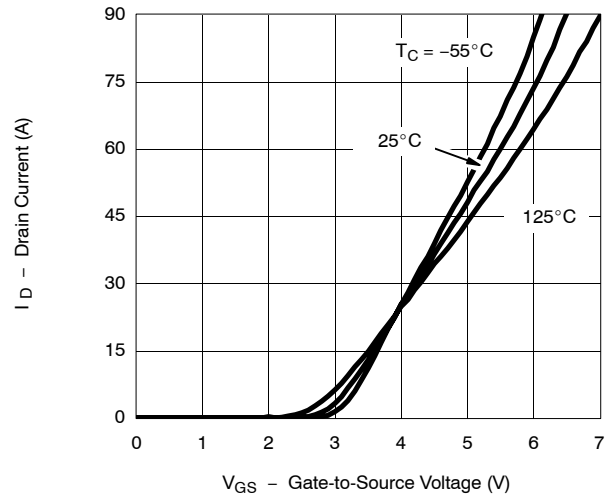


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

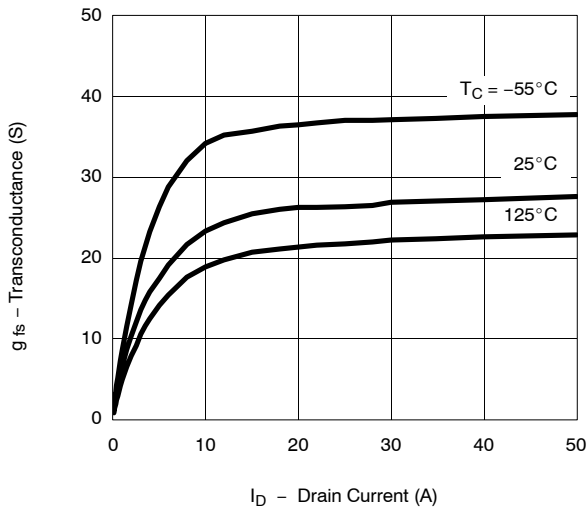
**Output Characteristics**



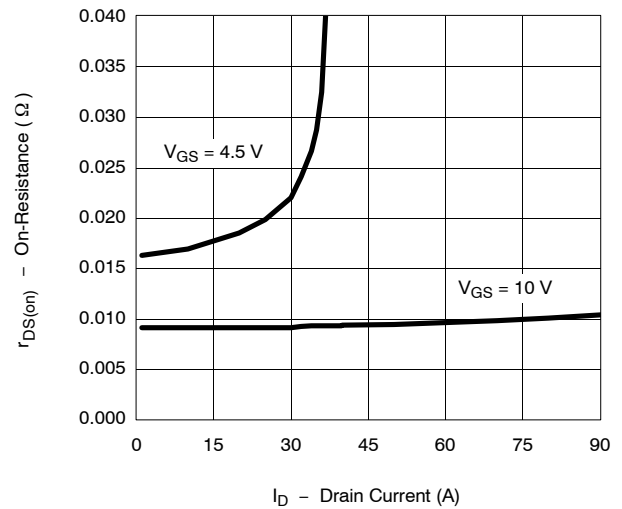
**Transfer Characteristics**



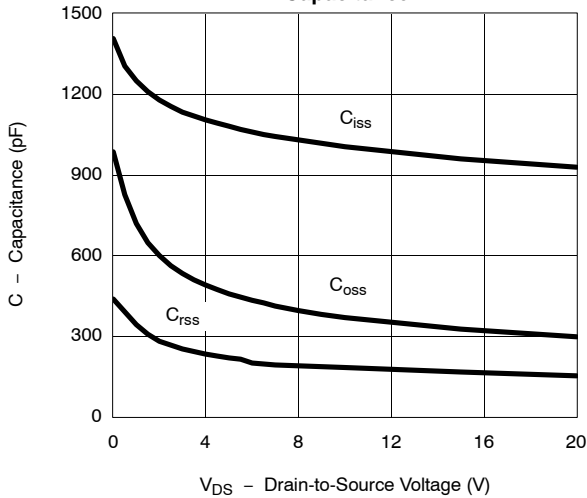
**Transconductance**



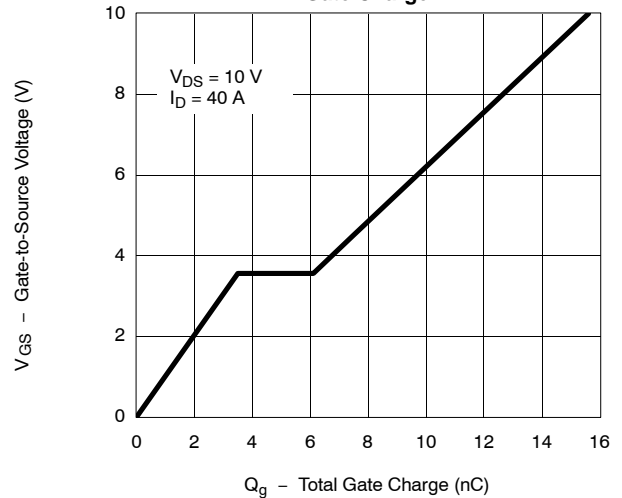
**On-Resistance vs. Drain Current**



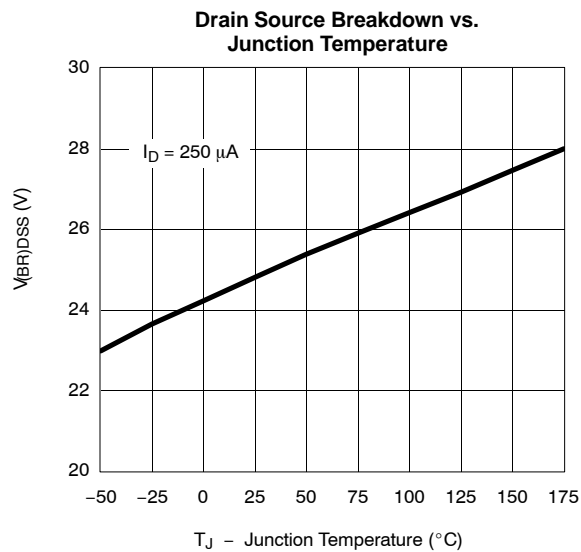
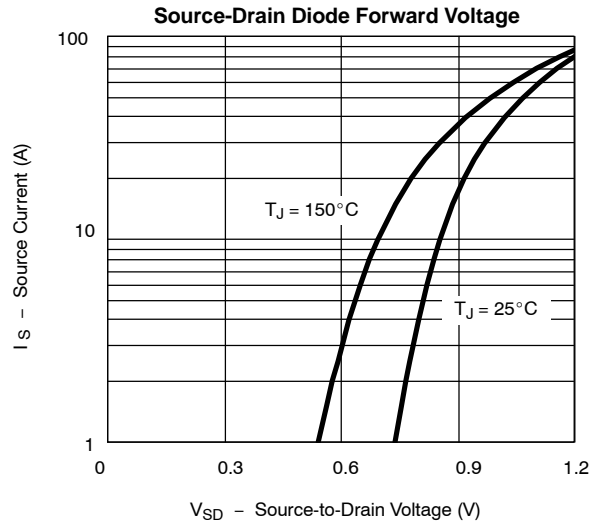
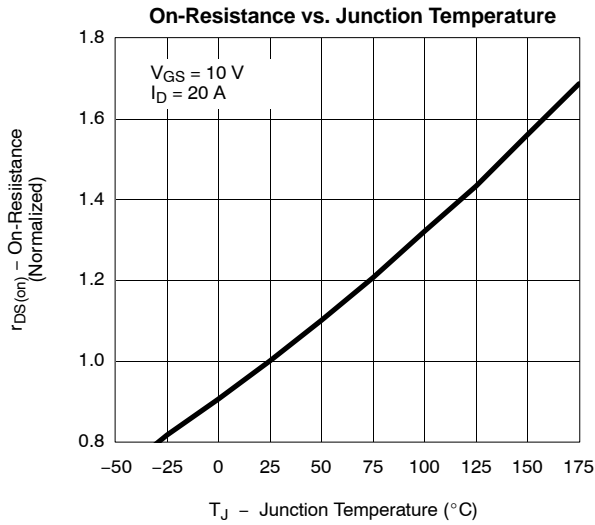
**Capacitance**



**Gate Charge**



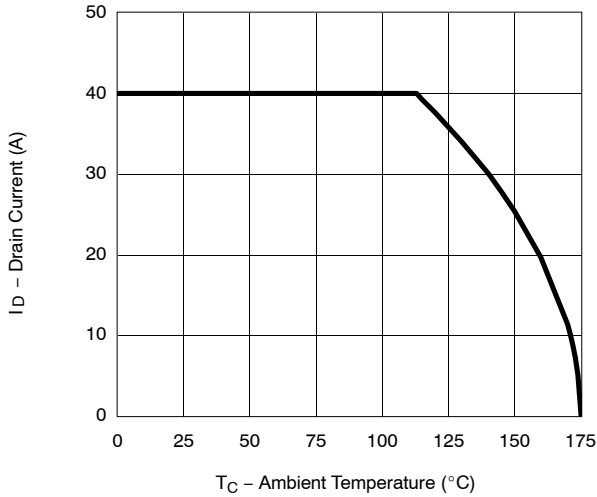
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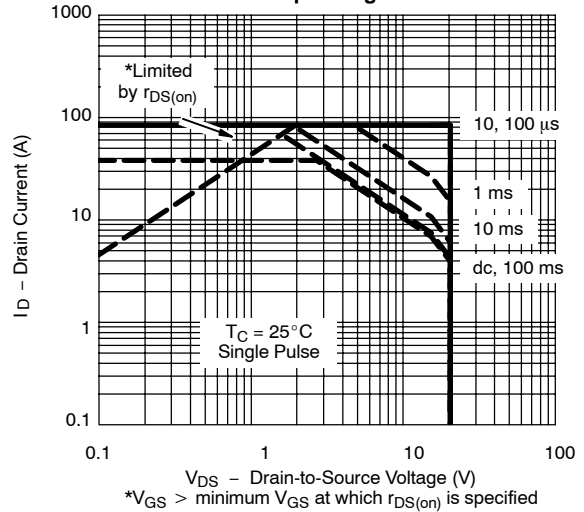


**THERMAL RATINGS**

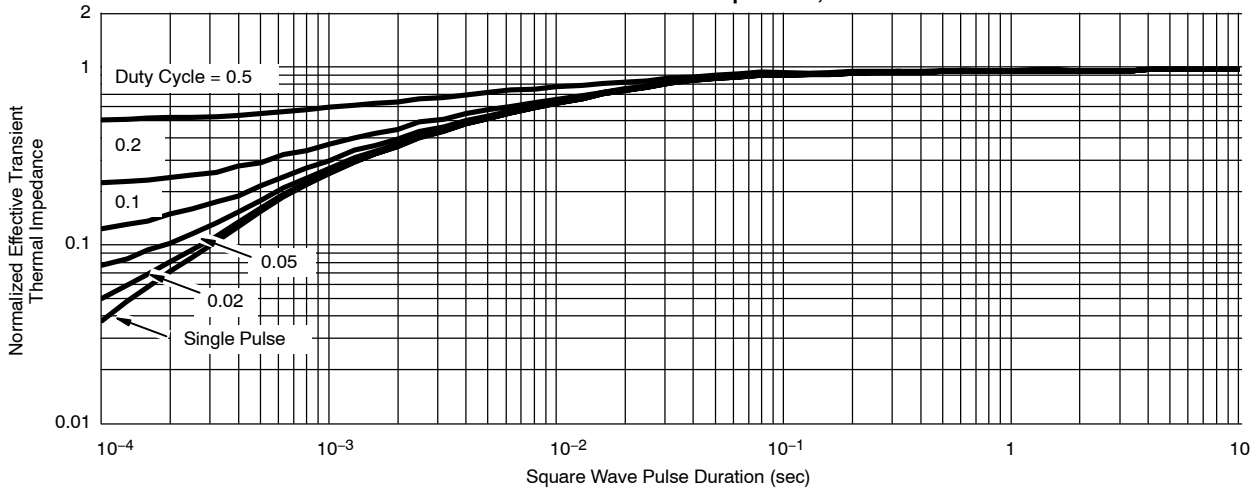
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72111>.