

## FEATURES

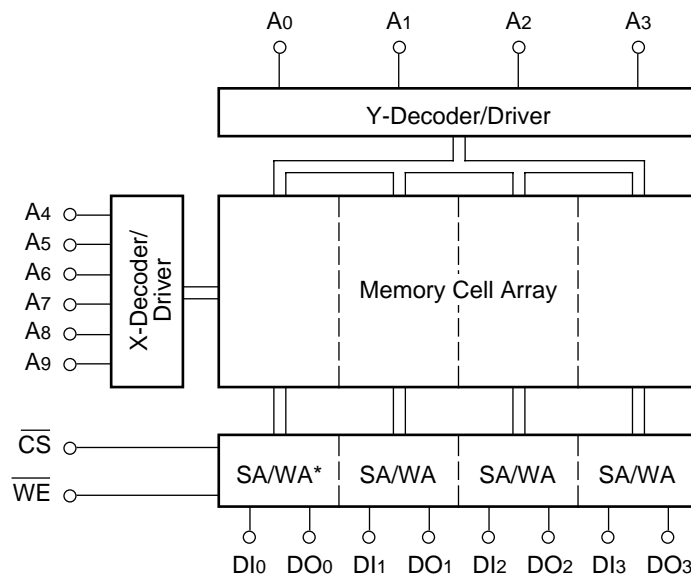
- Address access time,  $t_{AA}$ : 3/4/5/7ns max.
- Chip select access time,  $t_{AC}$ : 2ns max.
- Write pulse width,  $t_{WW}$ : 3ns min.
- Edge rate,  $t_r/t_f$ : 500ps typ.
- Power supply current,  $I_{EE}$ : -300mA, -220mA for -5/7ns
- Superior immunity against alpha particles provides virtually no soft error sensitivity
- Built with advanced ASSET™ technology
- Fully compatible with industry standard 10K/100K ECL I/O levels
- Noise margins improved with on-chip voltage and temperature compensation
- Open emitter output for easy memory expansion
- ESD protection of 2000V
- Available in 24-pin Flatpack and 28-pin PLCC and MLCC packages

## DESCRIPTION

The Synergy SY10/100/101474 are 4096-bit Random Access Memories (RAMs), designed with advanced Emitter Coupled Logic (ECL) circuitry. The devices are organized as 1024-words-by-4-bits and meet the standard 10K/100K family signal levels. The SY100474 is also supply voltage-compatible with 100K ECL, while the SY101474 operates from 10K ECL supply voltage (-5.2V). All feature on-chip voltage and temperature compensation for improved noise margin.

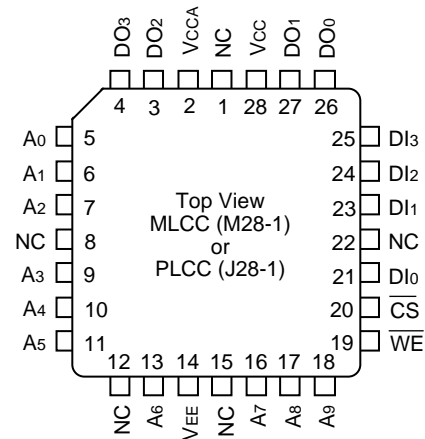
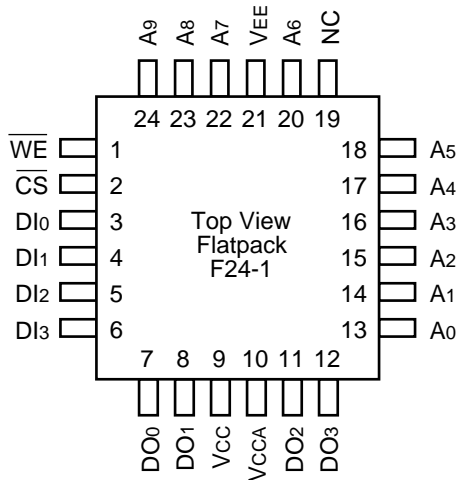
The SY10/100/101474 employ proprietary circuit design techniques and Synergy's proprietary ASSET advanced bipolar technology to achieve extremely fast access, write pulse width and write recovery times. ASSET uses proprietary technology concepts to achieve significant reduction in parasitic capacitance while improving device packing density. Synergy's circuit design techniques, coupled with ASSET, result not only in ultra-fast performance, but also allow device operation with virtually no soft error sensitivity and with outstanding device reliability in volume production.

## BLOCK DIAGRAM



\* SA = Sense Amplifier  
 WA = Write Amplifier

## PIN CONFIGURATIONS



## PIN NAMES

Label	Function
A0 - A9	Address Inputs
CS	Chip Select
WE	Write Enable
DI0 - DI3	Data Input (DIN)
DO0 - DO3	Data Output (DOUT)
Vcc	GND (0V)
VCCA	Output GND (0V)
VEE	Supply Voltage
NC	No Connect

## TRUTH TABLE

Input			Output	Mode
CS	WE	DIN		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	DOUT	Read

**NOTE:**

H = High Voltage Level  
 L = Low Voltage Level  
 X = Don't Care

## FUNCTIONAL DESCRIPTION

The Synergy SY10/100/101474 are 4096-bit RAMs organized as 1024-words-by-4-bits. Memory cell selection is achieved by using the 10 address bits designated as A0 through A9. Each of the  $2^{10}$  possible input address combinations corresponds to a unique word location in memory. The active low Chip Select ( $\overline{CS}$ ) is provided for memory expansion. The active low Write Enable ( $\overline{WE}$ ) controls the read and write operation. Data resident on the  $\overline{DIN}$  inputs ( $\overline{DI0}$  through  $\overline{DI3}$ ) is written into the addressed location only when  $\overline{WE}$  and  $\overline{CS}$  are held low. In order to perform a read operation,  $\overline{WE}$  is held high,  $\overline{CS}$  is held low

and the non-inverted output data at the addressed location is transferred to  $\overline{DOUT}$  ( $\overline{DO0}$  through  $\overline{DO3}$ ) to be read out. Open emitter outputs are provided for maximum flexibility and memory expansion by allowing output wire-OR connections. External termination of  $50\Omega$  to  $-2.0V$  or an equivalent circuit must be used to provide the specified output levels.

The outputs are brought to a logical low level when the RAM is being written into ( $\overline{WE} = \text{LOW}$ ) or when the device is deselected via the active low chip select pin ( $\overline{CS} = \text{HIGH}$ ).

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Value	Unit
V <sub>EE</sub>	V <sub>EE</sub> Pin Potential to V <sub>CC</sub> Pin	+0.5 to -7.0	V
V <sub>IN</sub>	Input Voltage	+0.5 to V <sub>EE</sub>	V
I <sub>OUT</sub>	DC Output Current (Output High)	-30	mA
T <sub>C</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>store</sub>	Storage Temperature	-65 to +150	°C

**NOTE:**

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

## GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Supply Voltage <sup>(1)</sup>	10K	V <sub>EE</sub>	-5.46	-5.2	-4.94	V
		T <sub>C</sub>	0	—	75	°C
Supply Voltage <sup>(1)</sup>	100K	V <sub>EE</sub>	-4.8	-4.5	-4.2	V
		T <sub>C</sub>	0	—	85	°C
Supply Voltage <sup>(1)</sup>	101K	V <sub>EE</sub>	-5.46	-5.2	-4.94	V
		T <sub>C</sub>	0	—	85	°C

**NOTE:**

1. Referenced to V<sub>CC</sub>.

## RISE AND FALL TIME

Parameter	Code <sup>(1)</sup>	Symbol	Min.	Typ.	Max.	Unit
Output Rise Time	F	tr	—	500	—	ps
	S		—	1500	—	
Output Fall Time	F	tf	—	500	—	ps
	S		—	1500	—	

**NOTE:**

1. F = Fast Edge Rate  
S = Standard Edge Rate

## CAPACITANCE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C <sub>IN</sub>	—	4	—	pF
Output Pin Capacitance	C <sub>OUT</sub>	—	5	—	pF

## 10K DC ELECTRICAL CHARACTERISTICS

VCC = 0V; TC = 0°C to +75°C; VEE = -5.2V; Airflow > 2.5m/s; Output Load = 50Ω to -2.0V

Symbol	Parameter	Tc	Min.	Max.	Unit	Condition
VOH	Output High Voltage	0°C +25°C +75°C	-1000 -960 -900	-840 -810 -720	mV	VIN = VIH Max. or VIL Min.
VOL	Output Low Voltage	0°C +25°C +75°C	-1870 -1850 -1830	-1665 -1650 -1625	mV	VIN = VIH Max. or VIL Min.
VOHC	Output High Voltage	0°C +25°C +75°C	-1020 -980 -920	— — —	mV	VIN = VIH Min. or VIL Max.
VOLC	Output Low Voltage	0°C +25°C +75°C	— — —	-1645 -1630 -1605	mV	VIN = VIH Min. or VIL Max.
VIH	Input High Voltage	0°C +25°C +75°C	-1145 -1105 -1045	-840 -810 -720	mV	Guaranteed Input Voltage High for All Inputs
VIL	Input Low Voltage	0°C +25°C +75°C	-1870 -1850 -1830	-1490 -1475 -1450	mV	Guaranteed Input Voltage Low for All Inputs
IiH	Input High Current	0°C to +75°C	0.0	20	μA	VIN = VIH Max.
IiL	Input Low Current	0°C to +75°C	-2	2	μA	VIN = VIL Min.
IiL	$\overline{CS}$ Input Low Current	0°C to +75°C	30	170	μA	VIN = VIL Min.
IiH	$\overline{CS}$ Input High Current	0°C to +75°C	40	220	μA	VIN = VIH Max.
IiL	$\overline{WE}$ Input Low Current	0°C to +75°C	-2	35	μA	VIN = VIL Min.
IiH	$\overline{WE}$ Input High Current	0°C to +75°C	0.0	60	μA	VIN = VIH Max.
IEE	Power Supply Current -3ns, -4ns -5ns, -7ns	0°C to +75°C	-300 -220	—	mA	All Inputs and Outputs Open

## 100K/101K DC ELECTRICAL CHARACTERISTICS

VCCA = 0V  
VCC = 0V

VEE = -4.5V (100K)  
VEE = -5.2V (101K)

TC = 0°C to +85°C

Airflow > 2.5m/s  
Output Load = 50Ω to -2.0V

Symbol	Parameter	Min.	Max.	Unit	Condition
VOH	Output High Voltage	-1025	-880	mV	VIN = VIH Max. or VIL Min.
VOL	Output Low Voltage	-1810	-1620	mV	VIN = VIH Max. or VIL Min.
VOHC	Output High Voltage	-1035	—	mV	VIN = VIH Min. or VIL Max.
VOLC	Output Low Voltage	—	-1610	mV	VIN = VIH Min. or VIL Max.
VIH	Input High Voltage	-1165	-880	mV	Guaranteed Input Voltage High for All Inputs
VIL	Input Low Voltage	-1810	-1475	mV	Guaranteed Input Voltage Low for All Inputs
IiH	Input High Current	0.0	20	μA	VIN = VIH Max.
IiL	Input Low Current	-2	2	μA	VIN = VIL Min.
IiL	$\overline{CS}$ Input Low Current	30	170	μA	VIN = VIL Min.
IiH	$\overline{CS}$ Input High Current	40	220	μA	VIN = VIH Max.
IiL	$\overline{WE}$ Input Low Current	-2	35	μA	VIN = VIL Min.
IiH	$\overline{WE}$ Input High Current	0.0	60	μA	VIN = VIH Max.
IEE	Power Supply Current 3ns, 4ns -5ns, -7ns	-300 -220	—	mA	All Inputs and Outputs Open

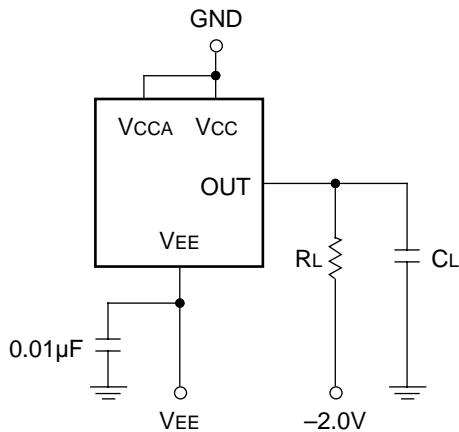
## AC ELECTRICAL CHARACTERISTICS

### AC TEST CONDITIONS

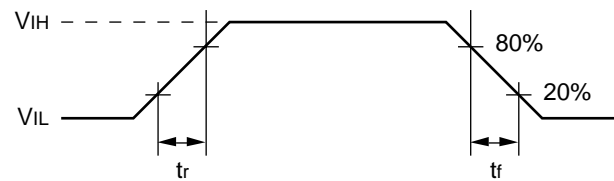
$V_{CC} = V_{CCA} = 0V$       Output Load =  $50\Omega$  to  $-2.0V$   
 $V_{EE} = -5.2V \pm 5\%(10K)$      $T_c = 0^\circ C$  to  $+75^\circ C$  (10K)  
 $V_{EE} = -4.5V \pm 0.3V(100K)$   $T_c = 0^\circ C$  to  $+85^\circ C$  (100K/101K)  
 $V_{EE} = -5.2V \pm 5\%(101K)$     Airflow > 2.5m/s

	$T_c$	$V_{IH}$	$V_{IL}$
10K	$0^\circ C$	-0.933V	-1.733V
	$+25^\circ C$	-0.90V	-1.70V
	$+75^\circ C$	-0.863V	-1.663V
100/101K	$0^\circ C$ to $+85^\circ C$	-0.90V	-1.70V

#### Loading Condition



#### Input Pulse



$t_r = t_f = 1.0ns$  typ.

OUTPUT LOAD:  $R_L = 50\Omega$   
 $C_L = 5pF^*$  (typ.)

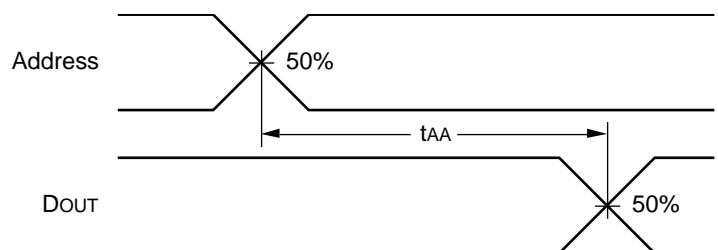
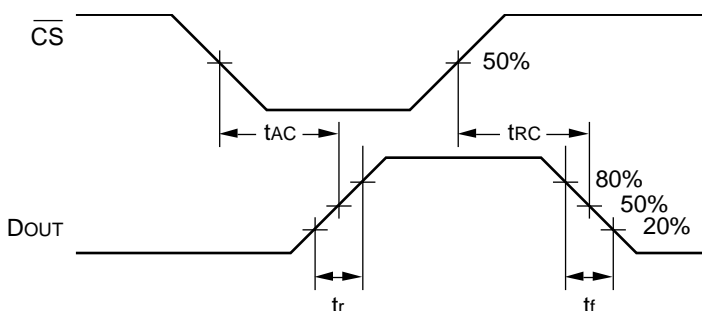
\* (Modeled as  $50\Omega$  transmission line terminated to  $-2V$ .)

**NOTE:** All timing measurements referenced to 50% input levels.

## READ CYCLE

Symbol	Parameter	SY10474-3 SY100474-3 SY101474-3		SY10474-4 SY100474-4 SY101474-4		SY10474-5 SY100474-5 SY101474-5		SY10474-7 SY100474-7 SY101474-7		Unit	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_{AA}$	TAVQV	Address Access Time	—	3	—	4	—	5	—	7	ns
$t_{AC}$	TSLQV	Chip Select Access Time	—	2	—	2	—	3	—	3	ns
$t_{RC}$	TSHQL	Chip Select Recovery Time	—	2	—	2	—	3	—	3	ns

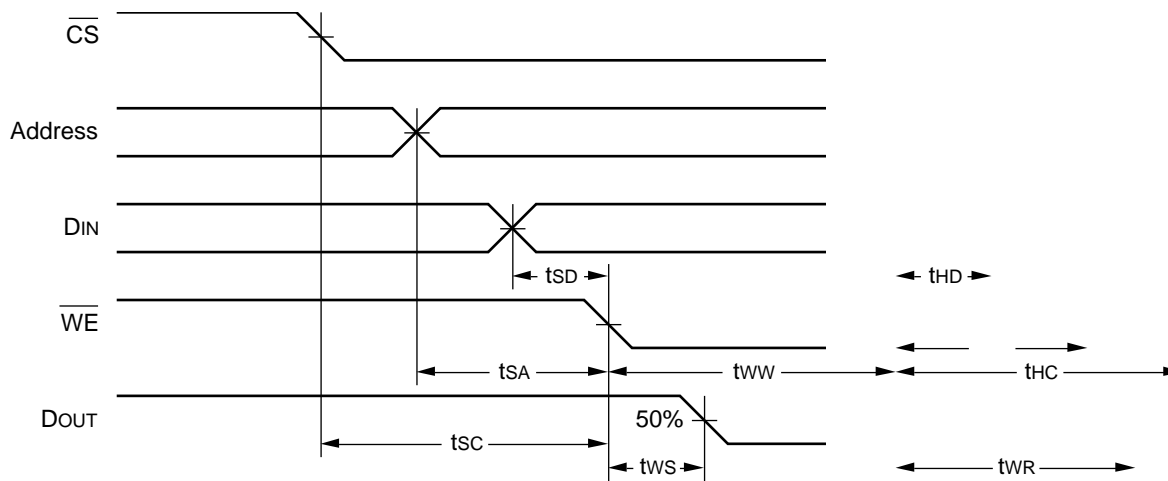
## READ CYCLE TIMING DIAGRAM



## WRITE CYCLE

Symbol		Parameter	SY10474-3 SY100474-3 SY101474-3		SY10474-4 SY100474-4 SY101474-4		SY10474-5 SY100474-5 SY101474-5		SY10474-7 SY100474-7 SY101474-7		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WW</sub>	TWLWH	Write Pulse Width	3	—	4	—	5	—	5	—	ns
t <sub>WS</sub>	TWLQL	Write Disable Time	—	2	—	2	—	3	—	4	ns
t <sub>WR</sub>	TWHQV	Write Recovery Time	—	3	—	4	—	5	—	5	ns
t <sub>SA</sub>	TAVWL	Address Set-up Time	1	—	1	—	1	—	1	—	ns
t <sub>SC</sub>	TSLWL	Chip Select Set-up Time	0	—	0	—	0.5	—	1	—	ns
t <sub>SD</sub>	TDVWL	Data Set-up Time	0	—	0	—	0.5	—	1	—	ns
t <sub>HA</sub>	TWHAX	Address Hold Time	1	—	1	—	1	—	1	—	ns
t <sub>HC</sub>	TWHSX	Chip Select Hold Time	1	—	1	—	1	—	1	—	ns
t <sub>HD</sub>	TWHDX	Data Hold Time	1	—	1	—	1	—	1	—	ns

## WRITE CYCLE TIMING DIAGRAM



## PRODUCT ORDERING CODE

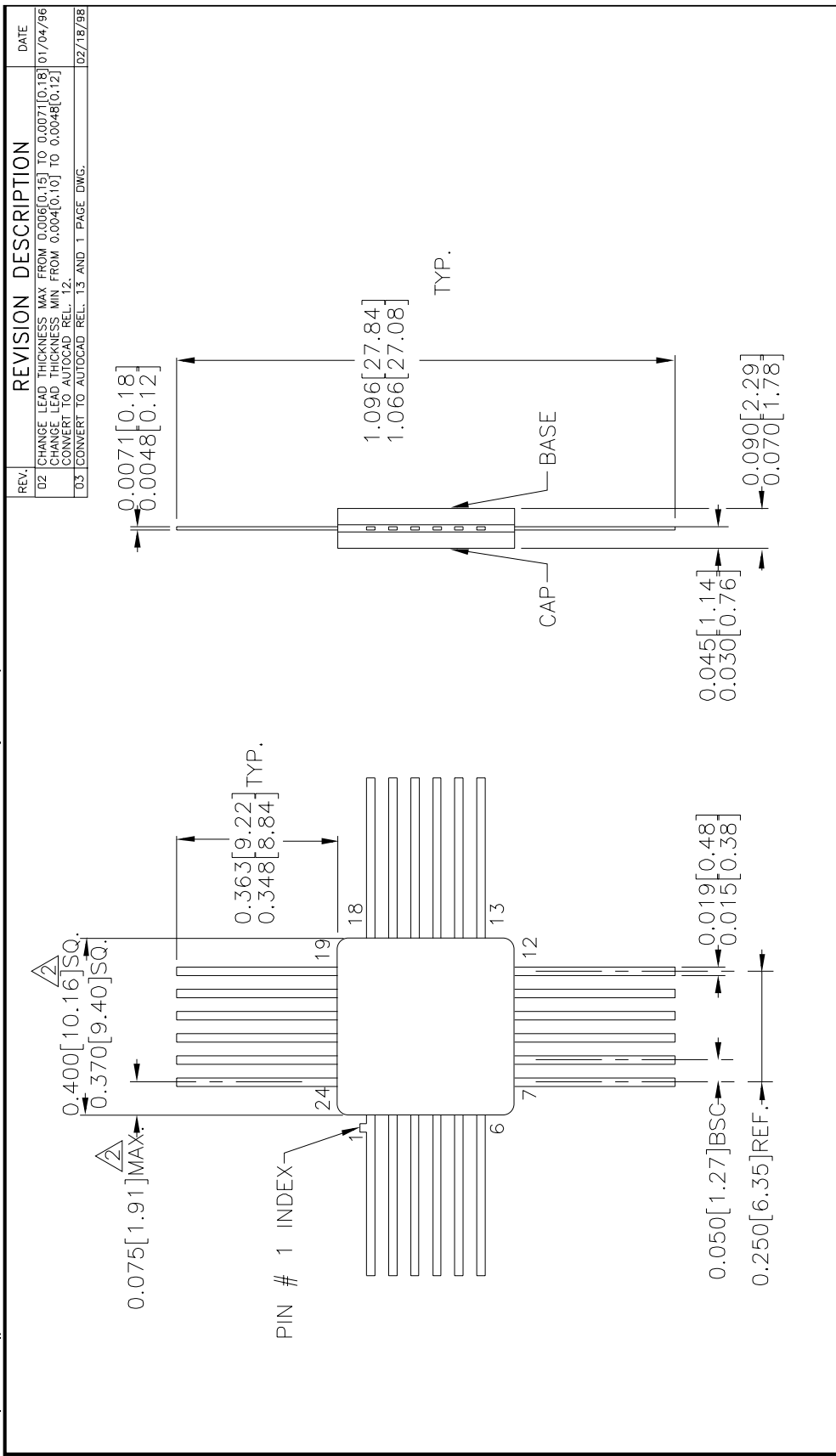
Speed (ns)	Ordering Code	Edge Rate	Package Type	Operating Range
3	SY10/100/101474-3FCF	Fast	F24-1	Commercial
	SY10/100/101474-3MCF	Fast	M28-1	Commercial
4	SY10/100/101474-4FCF	Fast	F24-1	Commercial
	SY10/100/101474-4MCF	Fast	M28-1	Commercial
5	SY10/100/101474-5FCS	Standard	F24-1	Commercial
	SY10/100/101474-5JCS	Standard	J28-1	Commercial
	SY10/100/101474-5JCSTR	Standard	J28-1	Commercial
7	SY10/100/101474-7FCS	Standard	F24-1	Commercial
	SY10/100/101474-7JCS	Standard	J28-1	Commercial
	SY10/100/101474-7JCSTR	Standard	J28-1	Commercial

**24 LEAD CERPACK (F24-1)**

FILE/REV #: PD0006A03

PD/0006/ASCORP

PAGE 1 OF 1



**SYNERGY**  
SEMICONDUCTOR

APPROVALS	DATE	APPROVALS	DATE
ORIGINATOR:	02/23/98	QUALITY:	
CHK'D:		DOCUMENT CONTROL:	
RELEASE DATE:			

3250 SCOTT BOULEVARD  
 SANTA CLARA, CA 95054  
 TEL: 408-980-9191  
 FAX: 408-567-7878

24 LEAD CERPACK  
 PACKAGE OUTLINE

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SCALE	REVISION
N/A	03

**NOTES:**

1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.



**28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)**

FILE/REV #: PD0008A03

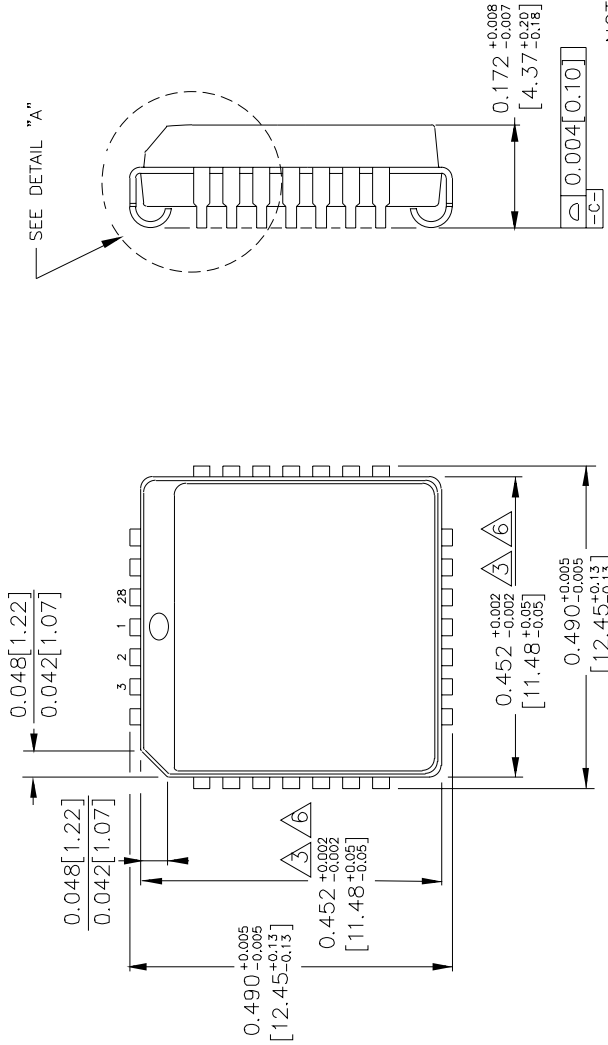
PD/0008/ASCORP

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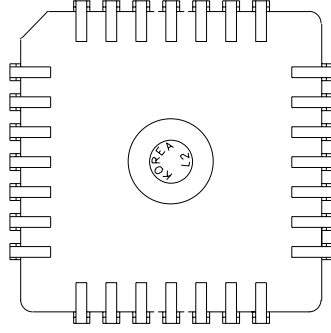
REV.	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450[1.43] TO 0.443[11.25]. TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD. REL. 12. REFERENCE AMKOR DWG. NO. 34855. REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98

SIDE VIEW

TOP VIEW



BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

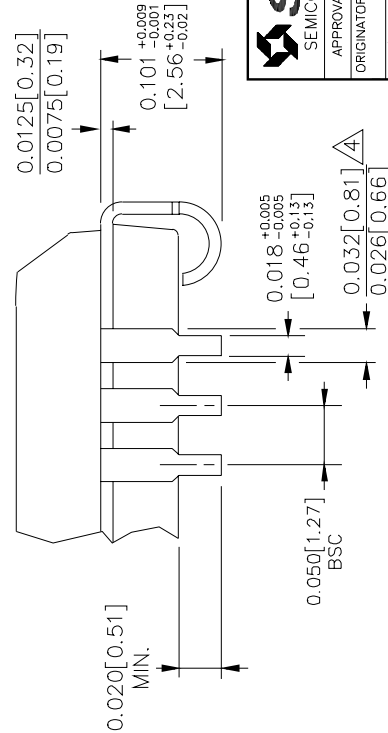


3250 SCOTT BOULEVARD  
SANITA CLARA, CA. 95054  
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FAX: 408-367-7678

APPROVALS	DATE	APPROVALS	DATE	SIZE	28 LEAD PLCC
ORIGINATOR:	02/23/98	QUALITY:		A	PACKAGE OUTLINE
CHK'D:		DOCUMENT CONTROL:			
RELEASE DATE:					

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SCALE: N/A  
REVISION: 03



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