

**FEATURES**

- Max. shift frequency of 600MHz
- Max. Clock to Q delay of 1200ps
- IEE min. of -150mA
- Industry standard 100K ECL levels
- Extended supply voltage option:  
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75KΩ input pull-down resistors
- 70% faster than Fairchild 300K at lower power
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

**DESCRIPTION**

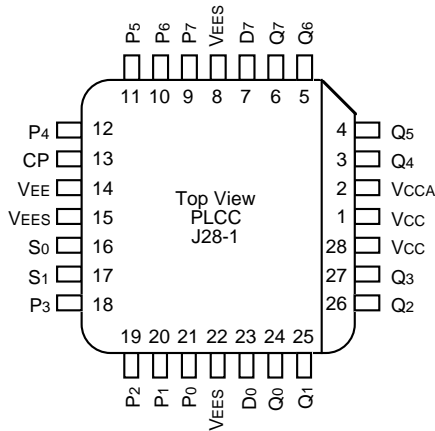
The SY100S341 offer eight D-type, edge-triggered flip-flops with both individual inputs for parallel operation as well as serial inputs for bidirectional shifting, and are designed for use in high-performance ECL systems. Data is clocked into the flip-flops on the rising edge of the clock.

The mode of operation is selected by two Select inputs (S<sub>0</sub>, S<sub>1</sub>) which determine if the device performs a shift, hold or parallel entry function, as described in the Truth Table. The inputs on these devices have 75KΩ pull-down resistors.

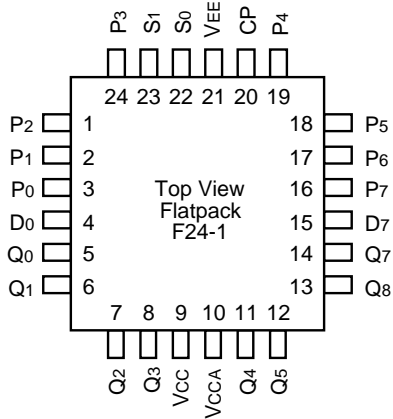
**PIN NAMES**

Label	Function
CP	Clock Pulse Input
S <sub>0</sub> — S <sub>1</sub>	Select Inputs
D <sub>0</sub> — D <sub>7</sub>	Serial Inputs
P <sub>0</sub> — P <sub>7</sub>	Parallel Inputs
Q <sub>0</sub> — Q <sub>7</sub>	Data Outputs
VEES	VEE Substrate
VCCA	Vcco for ECL Outputs

**PACKAGE/ORDERING INFORMATION**



**28-Pin PLCC (J28-1)**



**24-Pin Cerpack (F24-1)**

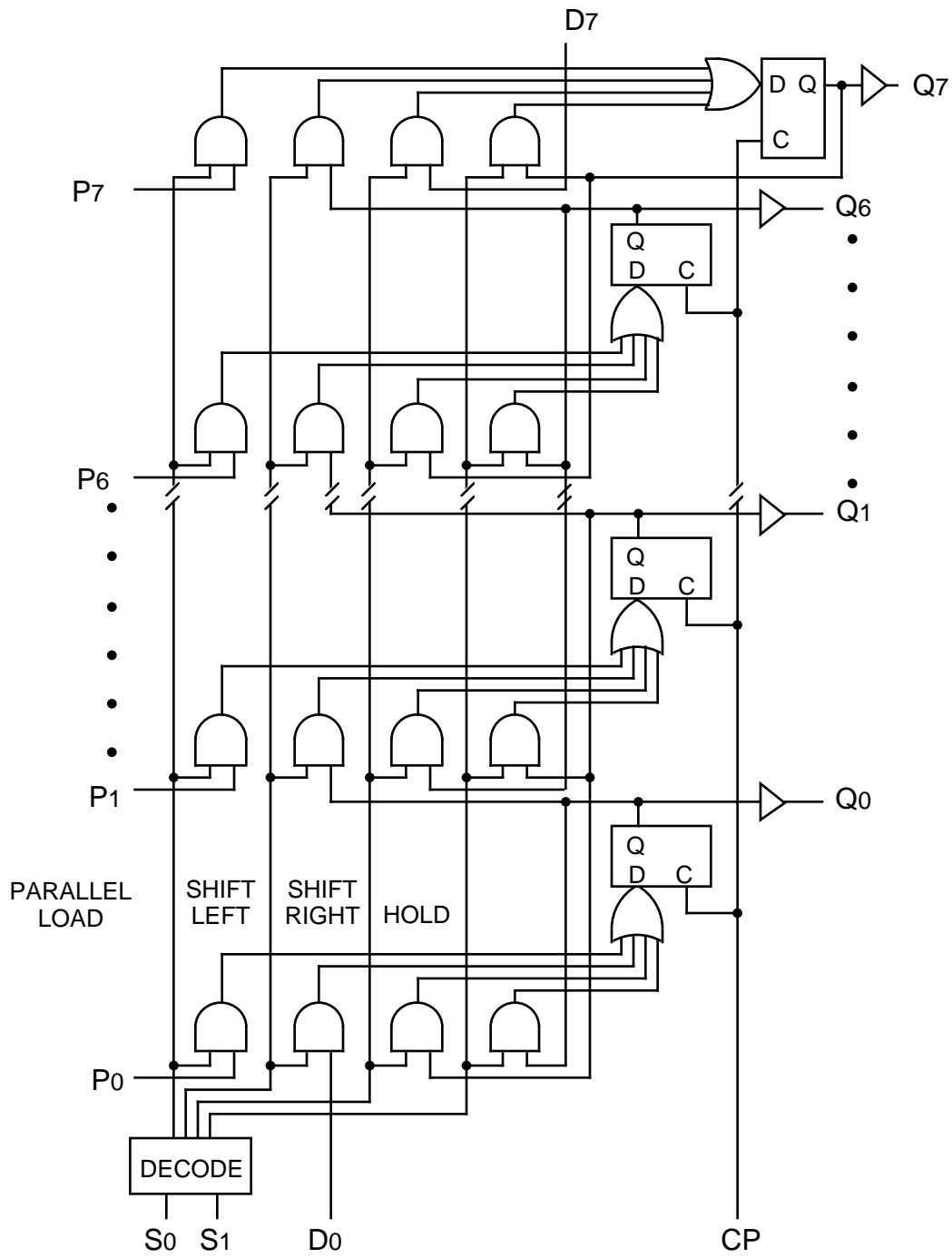
**Ordering Information**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S341FC	F24-1	Commercial	SY100S341FC	Sn-Pb
SY100S341FCTR <sup>(1)</sup>	F24-1	Commercial	SY100S341FC	Sn-Pb
SY100S341JC	J28-1	Commercial	SY100S341JC	Sn-Pb
SY100S341JCTR <sup>(1)</sup>	J28-1	Commercial	SY100S341JC	Sn-Pb
SY100S341JZ <sup>(2)</sup>	J28-1	Commercial	SY100S341JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S341JZTR <sup>(1, 2)</sup>	J28-1	Commercial	SY100S341JZ with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

**BLOCK DIAGRAM**



**TRUTH TABLE**

Function	Inputs					Outputs							
	D7	D0	S1	S0	CP	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Load Register	X	X	L	L	u	P7	P6	P5	P4	P3	P2	P1	P0
Shift Left	X	L	L	H	u	Q6	Q5	Q4	Q3	Q2	Q1	Q0	L
Shift Left	X	H	L	H	u	Q6	Q5	Q4	Q3	Q2	Q1	Q0	H
Shift Right	L	X	H	L	u	L	Q7	Q6	Q5	Q4	Q3	Q2	Q1
Shift Right	H	X	H	L	u	H	Q7	Q6	Q5	Q4	Q3	Q2	Q1
Hold	X	X	H	H	X	No Change							
Hold	X	X	X	X	H	No Change							
Hold	X	X	X	X	L	No Change							

**NOTE:**

- 1. H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Don't Care
- u = LOW-to-HIGH Transition

**DC ELECTRICAL CHARACTERISTICS**

V<sub>EE</sub> = -4.2V to -5.5V unless otherwise specified; V<sub>CC</sub> = V<sub>CCA</sub> = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I <sub>IH</sub>	Input HIGH Current, All Inputs	—	—	200	μA	V <sub>IN</sub> = V <sub>IH</sub> (Max.)
I <sub>EE</sub>	Power Supply Current	-150	-102	-71	mA	Inputs Open

**AC ELECTRICAL CHARACTERISTICS**

**CERPACK**

V<sub>EE</sub> = -4.2V to -5.5V unless otherwise specified; V<sub>CC</sub> = V<sub>CCA</sub> = GND

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
f <sub>shift</sub>	Shift Frequency	600	—	600	—	600	—	MHz	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Output	450	1200	450	1200	450	1200	ps	
t <sub>TLH</sub> t <sub>THL</sub>	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t <sub>s</sub>	Set-up Time D <sub>n</sub> , P <sub>n</sub> S <sub>n</sub>	300 600	— —	300 600	— —	300 600	— —	ps	
t <sub>H</sub>	Hold Time D <sub>n</sub> , P <sub>n</sub> S <sub>n</sub>	300 0	— —	300 0	— —	300 0	— —	ps	
t <sub>pw</sub> (H)	Pulse Width HIGH, CP	—	600	—	600	—	600	ps	

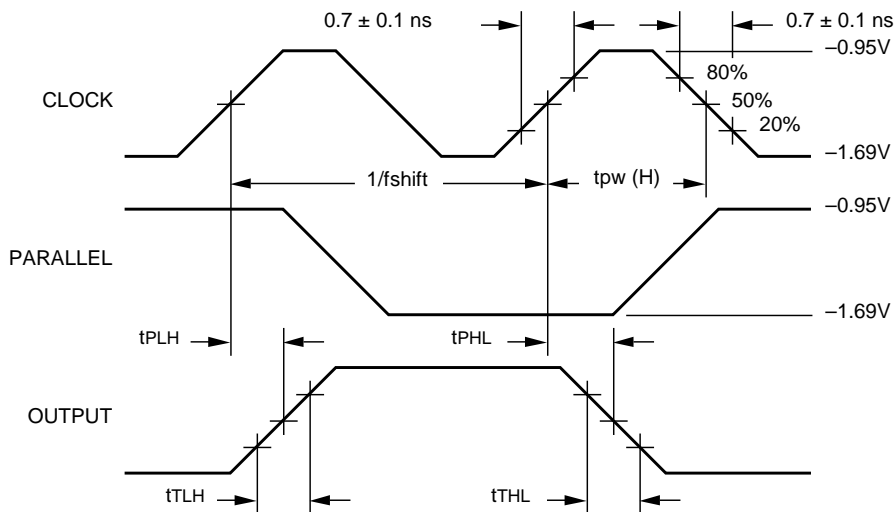
**AC ELECTRICAL CHARACTERISTICS**

**PLCC**

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

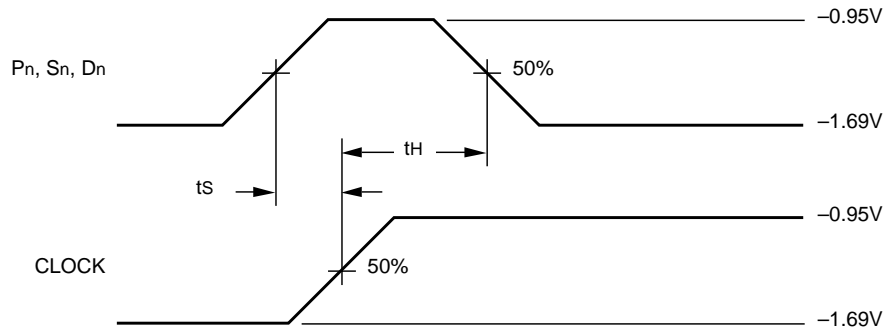
Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
fshift	Shift Frequency	600	—	600	—	600	—	MHz	
tPLH tPHL	Propagation Delay CP to Output	450	1200	450	1200	450	1200	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
ts	Set-up Time Dn, Pn	300	—	300	—	300	—	ps	
	Sn	600	—	600	—	600	—		
th	Hold Time Dn, Pn	300	—	300	—	300	—	ps	
	Sn	0	—	0	—	0	—		
tpw (H)	Pulse Width HIGH, CP	—	600	—	600	—	600	ps	

**TIMING DIAGRAMS**



Propagation Delay and Transition Times

**TIMING DIAGRAMS**

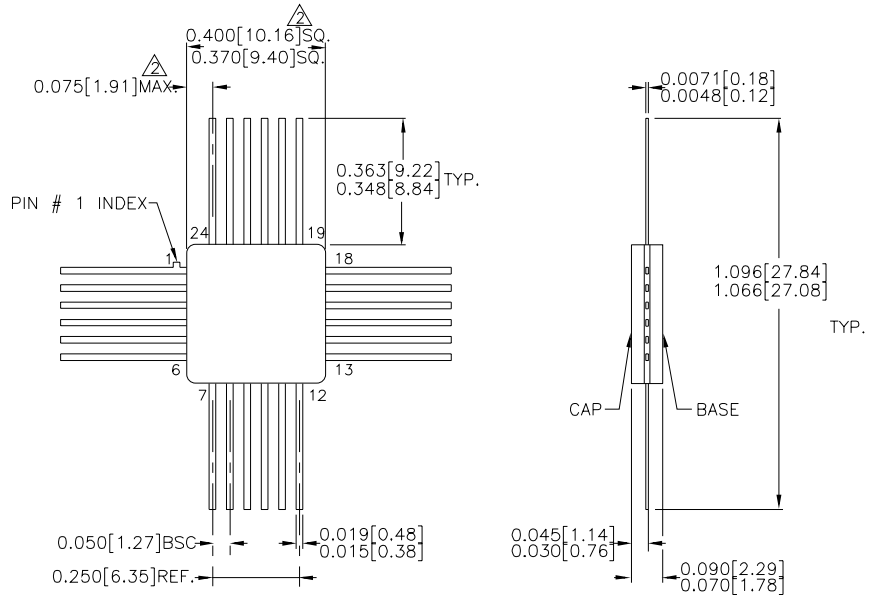


**Set-up and Hold Times**

**Notes:**

1. VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND.
2. ts is the minimum time before the transition of the clock that information must be present at the data input.
3. tH is the minimum time after the transition of the clock that information must remain unchanged at the data input.

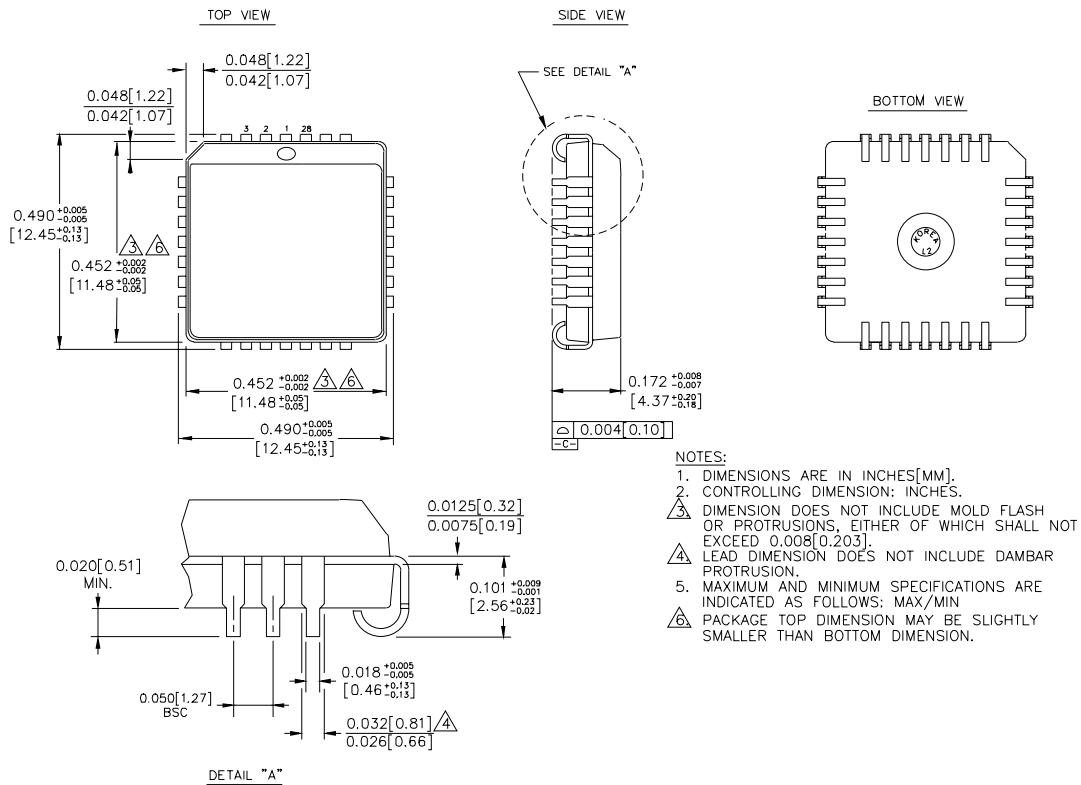
**24-PIN CERPACK (F24-1)**



- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
  2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
  3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

**28-PIN PLCC (J28-1)**



Rev. 03

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