DRAM

1024K x 16 DYNAMIC RAM

EDO PAGE MODE

FEATURES

- Industry-standard x 16 pinouts and timing functions.
- Single 5V (±10%) power supply.
- All device pins are TTL- compatible.
- 1K-cycle refresh in 16ms.
- Refresh modes: $\overline{RAS}$ only, $\overline{CAS}$ BEFORE $\overline{RAS}$ (CBR) and HIDDEN.
- Extended data-out (EDO) PAGE MODE access cycle.
- BYTE WRITE and BYTE READ access cycles.

OPTION

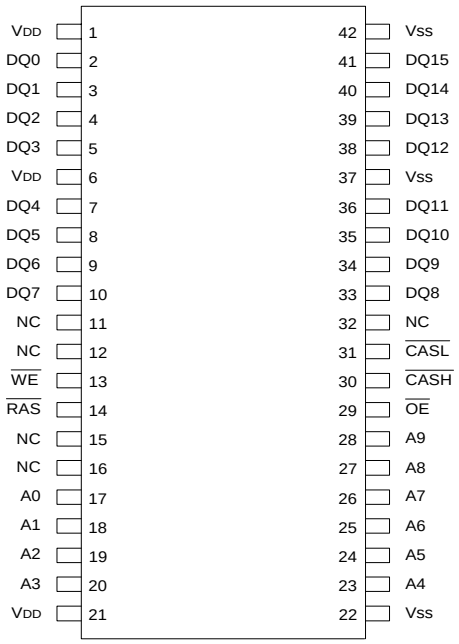
TIMING	MARKING
45ns	-45
50ns	-50
60ns	-60
PACKAGE	
42-pin SOJ	J
44/50-pin TSOPII	S

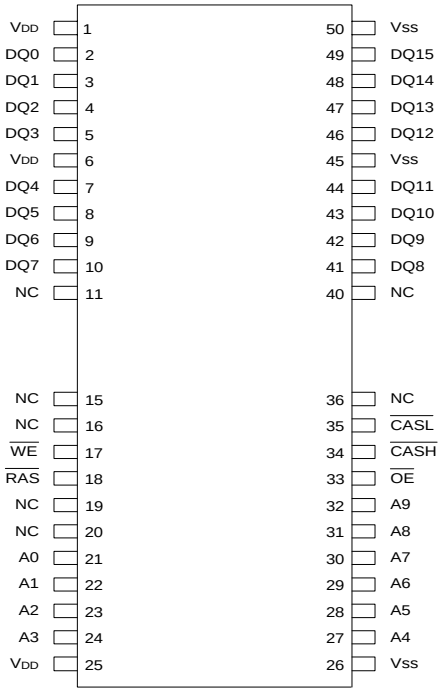
GENERAL DESCRIPTION

The T2316162A is a randomly accessed solid state memory containing 16,777,216 bits organized in a x16 configuration. The T2316162A has both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins. It offers Fast Page mode with Extended Data Output.

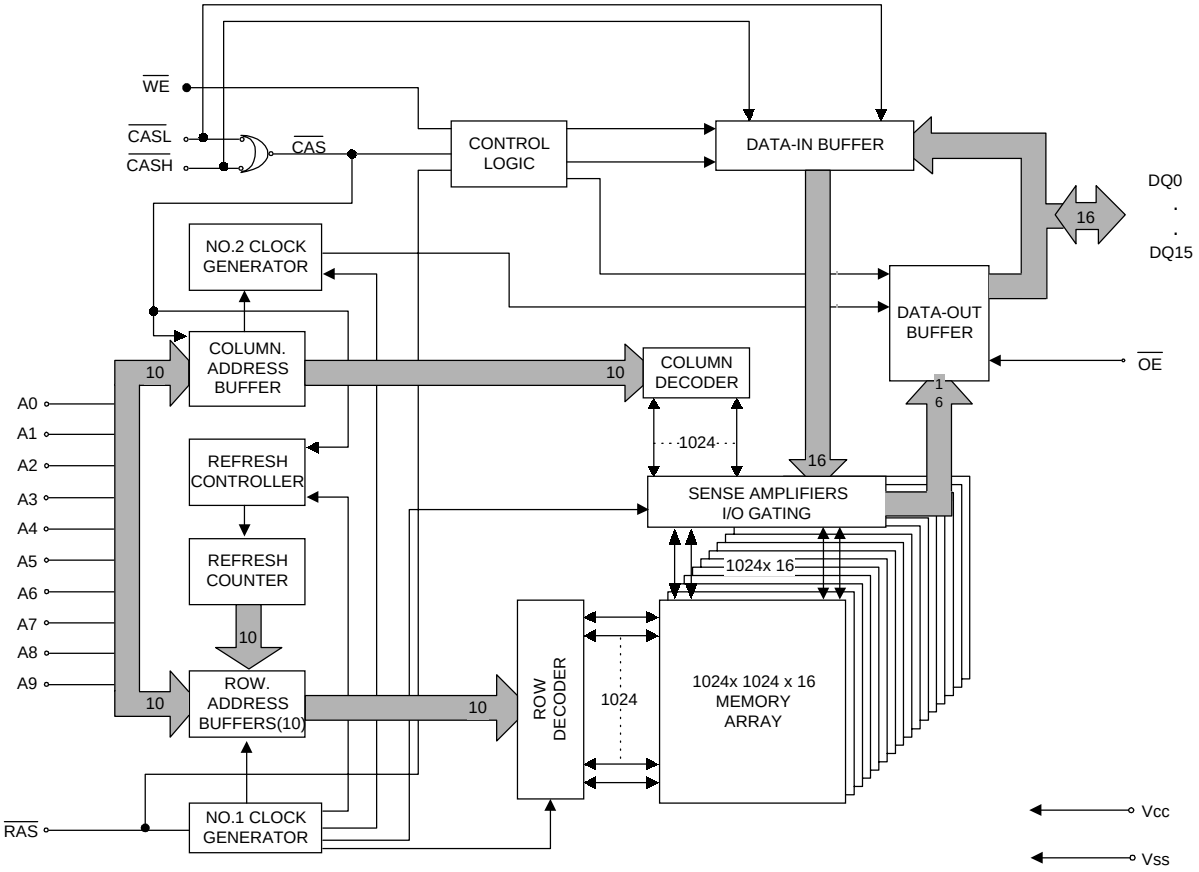
The T2316162A $\overline{CAS}$ function and timing are determined by the first $\overline{CAS}$ to transition low and by the last to transition back high. Use only one of the two $\overline{CAS}$ and leave the other staying high during WRITE will result in a BYTE WRITE. $\overline{CASL}$ transiting low in a WRITE cycle will write data into the lower byte (DQ0~DQ7), and $\overline{CASH}$ transiting low will write data into the upper byte (DQ8~DQ15).

PIN ASSIGNMENT (Top View)





FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SYM.	TYPE	DESCRIPTION
A0-A9	Input	Address Input
$\overline{RAS}$	Input	Row Address Strobe
$\overline{CASH}$	Input	Column Address Strobe /Upper Byte Control
$\overline{CASL}$	Input	Column Address Strobe /Lower Byte Control
$\overline{WE}$	Input	Write Enable
$\overline{OE}$	Input	Output Enable
DQ0 – DQ15	Input/ Output	Data Input/ Output
Vcc	Supply	Power, 5V
Vss	Ground	Ground
NC	-	No Connect

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any pin Relative to VSS.... -1V to +7V

Operating Temperature, Ta (ambient).....

……0°C to +70°C

Storage Temperature (plastic)..... -55°C to +150°C

Power Dissipation 1.2W

Short Circuit Output Current..... 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(0°C ≤ Ta ≤ 70°C; VCC = 5V ± 10 % unless otherwise noted)

DESCRIPTION	CONDITIONS	SYM.	MIN	MAX	UNITS	NOTES
Supply Voltage		Vcc	4.5	5.5	V	1
Supply Voltage		Vss	0	0	V	
Input High (Logic) voltage		V_{IH}	2.4	Vcc+1	V	1
Input Low (Logic) voltage		V_{IL}	-1.0	0.8	V	1
Input Leakage Current	$0V \le V_{IN} \le 7V$	I_{LI}	-10	10	uA	
Output Leakage Current	$0V \le V_{OUT} \le 7V$ Output(s) disabled	I_{LO}	-10	10	uA	
Output High Voltage	I_{OH} = -5 mA	V_{OH}	2.4	Vcc	V	
Output Low Voltage	I_{OL} = 4.2 mA	V_{OL}	0	0.4	V	

Note: 1.All Voltages referenced to Vss

			MAX				
DESCRIPTION	CONDITIONS	SYM.	-45	-50	-60	UNITS	NOTES
Operating Current	$\overline{RAS}$, $\overline{CAS}$ cycling , ^tRC = min	Icc1	190	180	170	mA	1,2
TTL Standby Current	TTL interface, $\overline{RAS}$, $\overline{CAS}$ =V_{IH}, D_{OUT}=High-Z	I_{cc2}	2	2	2	mA	
$\overline{RAS}$ -only refresh Current	^tRC = min	I_{cc3}	190	180	170	mA	2
EDO Page Mode Current	^tPC = min	I_{cc4}	150	140	130	mA	1,3
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	^tRC = min	Icc5	190	180	170	mA	
CMOS Standby Current	CMOS interface, $\overline{RAS}$, $\overline{CAS}$ >Vcc-0.2V	I_{cc6}	1.0	1.0	1.0	mA	1

Note: 1. Icc depends on output load condition when the device is selected.
Icc max is specified at the output open condition.
2. Address can be changed twice or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

CAPACITANCE

(Ta =25°C, Vcc =5V ±10 %)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (address)	C_{I1}	-	5	pF	1
Input Capacitance (clocks)	C_{I2}	-	7	pF	1
Output Capacitance (data-in, data-out)	C_{DQ}	-	10	pF	1

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

AC ELECTRICAL CHARACTERISTICS (note 14)

(Ta =0 to 70°C, Vcc=5V ±10 %, Vss=0V)
Test Conditions (note 29)

AC CHARACTERISTICS PARAMETER	SYM	-45		-50		-60		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Read or Write Cycle Time	t_{RC}	80		84		110		ns	
Read Write Cycle Time	t_{RWC}	105		113		140		ns	
EDO-Page-Mode Read or Write Cycle Time	t_{PC}	16		20		25		ns	22
EDO-Page-Mode Read-Write Cycle Time	t_{PCM}	46		58		70		ns	22
Access Time From $\overline{RAS}$	t_{RAC}		45		50		60	ns	4
Access Time From $\overline{CAS}$	t_{CAC}		11		13		15	ns	5,20
Access Time From $\overline{OE}$	t_{OAC}		11		13		15	ns	13,20
Access Time From Column Address	t_{AA}		19		25		30	ns	
Access Time From $\overline{CAS}$ Precharge	t_{ACP}		22		27		35	ns	20
$\overline{RAS}$ Pulse Width	t_{RAS}	45	10K	50	10K	60	10K	ns	
$\overline{RAS}$ Pulse Width (EDO Page Mode)	t_{RASC}	45	100K	50	100K	60	100K	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	11		13		15		ns	27
$\overline{RAS}$ Precharge Time	t_{RP}	28		30		40		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	6	10K	8	10K	15	10K	ns	26
$\overline{CAS}$ Hold Time	t_{CSH}	40		40		60		ns	19
$\overline{CAS}$ Precharge Time (EDO Page Mode)	t_{CP}	5		6		10		ns	23
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	10	34	12	37	20	45	ns	7,18
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		5		ns	19
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	5		8		10		ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	8	26	10	28	12	30	ns	8
Column Address Setup Time	t_{ASC}	0		0		0		ns	18
Column Address Hold Time	t_{CAH}	6		8		10		ns	18
Column Address Hold Time (Reference to $\overline{RAS}$)	t_{AR}	35		38		45		ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	19		23		30		ns	

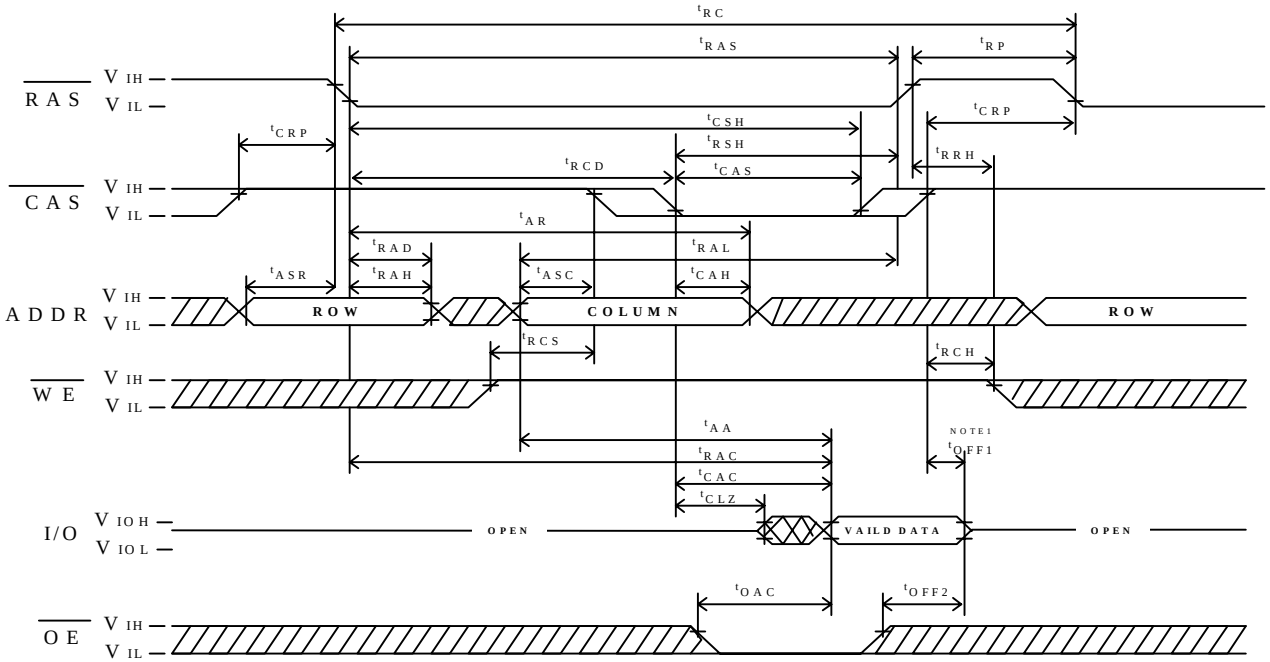
AC ELECTRICAL CHARACTERISTICS (continued)

AC CHARACTERISTICS PARAMETER	SYM	-45		-50		-60		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Command Setup Time	t_{RCS}	0		0		0		ns	15,18
Read Command Hold Time Reference to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9,15,19
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	3		3		3		ns	20
Output Buffer Turn-off Delay From $\overline{CAS}$ or $\overline{RAS}$	t_{OFF1}	3	15	3	15	3	15	ns	10,17, 20
Output Buffer Turn-off to $\overline{OE}$	t_{OFF2}		8		8		15	ns	17,28
Write Command Setup Time	t_{WCS}	0		0		0		ns	11,15,18
Write Command Hold Time	t_{WCH}	6		8		10		ns	15,27
Write Command Hold Time (Reference to $\overline{RAS}$)	t_{WCR}	35		38		45		ns	15
Write Command Pulse Width	t_{WP}	6		8		15		ns	15
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	9		9		10		ns	15
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	8		8		10		ns	15,19
Data-in Setup Time	t_{DS}	0		0		0		ns	12,20
Data-in Hold Time	t_{DH}	6		8		10		ns	12,20
Data-in Hold Time (Reference to $\overline{RAS}$)	t_{DHR}	35		38		45		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	61		64		85		ns	11
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	35		39		55		ns	11
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	27		27		40		ns	11,18
Transition Time (rise or fall)	t_T	2.5	50	2.5	50	2.5	50	ns	2,3
Refresh Period (1024 cycles)	t_{REF}		16		16		16	ms	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	10		10		10		ns	
$\overline{CAS}$ Setup Time (CBR REFRESH)	t_{CSR}	10		10		10		ns	1,18
$\overline{CAS}$ Hold Time (CBR REFRESH)	t_{CHR}	10		10		10		ns	1,19
$\overline{OE}$ Hold Time From $\overline{WE}$ During Read-Modify-Write Cycle	t_{OEH}	6		10		15		ns	16
$\overline{OE}$ Low to $\overline{CAS}$ High Setup Time	t_{OES}	5		5		5		ns	
$\overline{OE}$ High Hold Time From $\overline{CAS}$ High	t_{OEHC}	3		5		10		ns	
$\overline{OE}$ High Pulse Width	t_{OEP}	2		5		10		ns	
$\overline{OE}$ Setup Prior to $\overline{CAS}$ During Hidden Refresh Cycle	t_{ORD}	0		0		0		ns	
Last $\overline{CAS}$ Going Low to First $\overline{CAS}$ Returning High	t_{CLCH}	6		10		10		ns	21
Data Output Hold After $\overline{CAS}$ Returning Low	t_{COH}	4		5		5		ns	
Output Disable Delay From $\overline{WE}$	t_{WHZ}	3	7	3	10	3	15	ns	

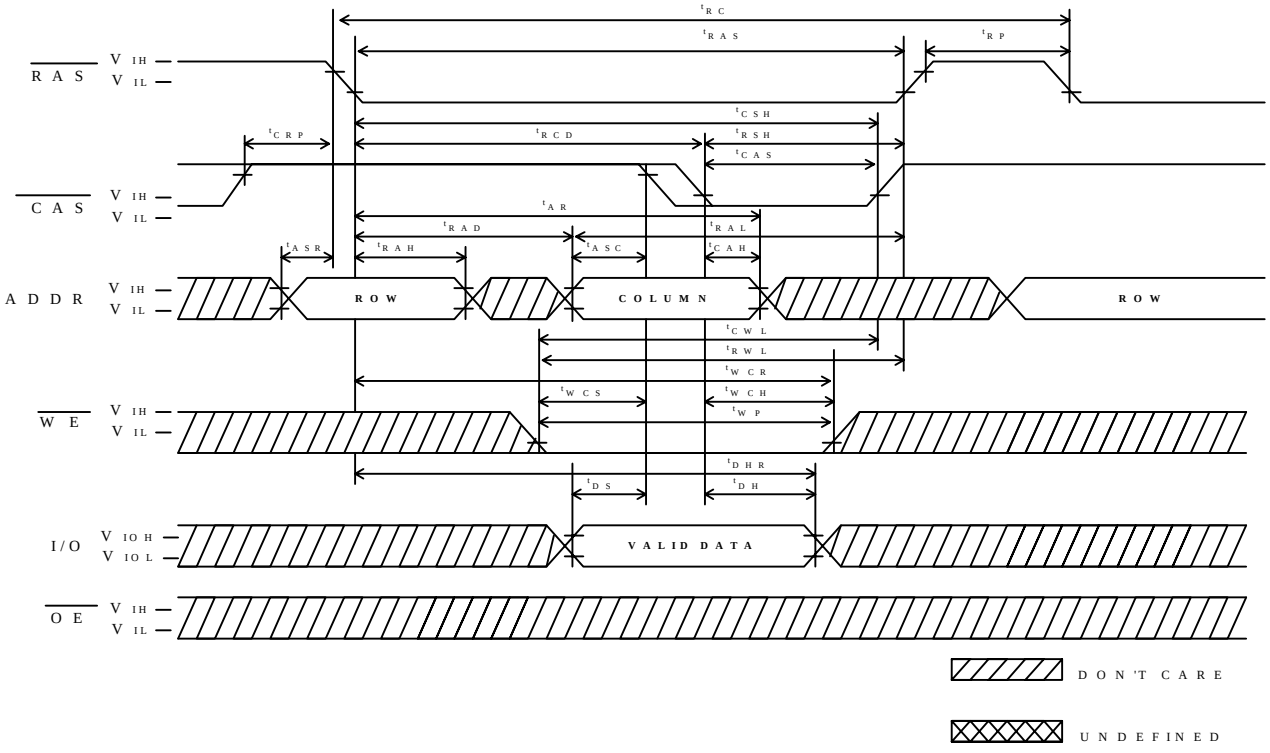
Notes:

1. Enables on-chip refresh and address counters.
2. V_{IH}(2.4V) and V_{IL}(0.8V) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (2.4V) and V_{IL} (0.8V).
3. In addition to meet the transition rate specification, all input signals must transit between V_{IH} and V_{IL} in a monotonic manner.
4. Assume that $t_{RCD} < t_{RCD}(max)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assume that $t_{RCD} \geq t_{RCD}(max)$.
6. If $\overline{CAS}$ is low at the falling edge of $\overline{RAS}$, data-out will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed high.
7. Operation within the $t_{RCD}(max)$ limit ensures that $t_{RAC}(max)$ can be met. $t_{RCD}(max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, access time is controlled by t_{CAC}.
8. Operation within the t_{RAD} limit ensures that $t_{RAC}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, access time is controlled by t_{AA}.
9. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
10. $t_{OFF1}(max)$ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
11. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If $t_{WCS} \geq t_{WCS}(min)$, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(min)$, $t_{AWD} \geq t_{AWD}(min)$ and $t_{CWD} \geq t_{CWD}(min)$, the cycle is READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to V_{IH}) is indeterminate. $\overline{OE}$ held high and $\overline{WE}$ taken low after $\overline{CAS}$ goes low result in a LATE WRITE($\overline{OE}$ -controlled) cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
13. During a READ cycle, if $\overline{OE}$ is low then taken HIGH before $\overline{CAS}$ goes high, I/O goes open, if $\overline{OE}$ is tied permanently low, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
14. An initial pause of 100ms is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
15. WRITE command is defined as $\overline{WE}$ going low.
16. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OFF2} and t_{OEH} met ($\overline{OE}$ high during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycles.
17. The I/Os open during READ cycles once t_{OFF1} or t_{OFF2} occur.
18. The first $\overline{CAS}$ edge to transition low.
19. The last $\overline{CAS}$ edge to transition high.
20. Output parameter (I/O) is referenced to corresponding $\overline{CAS}$ input, IO1~8 by $\overline{CASL}$ and IO9~16 by $\overline{CASH}$.
21. Last falling $\overline{CAS}$ edge to first rising $\overline{CAS}$ edge.
22. Last rising $\overline{CAS}$ edge to next cycle's last rising $\overline{CAS}$ edge.
23. Last rising $\overline{CAS}$ edge to first falling $\overline{CAS}$ edge.
24. First IOs controlled by the first $\overline{CAS}$ to go low.
25. Last IOs controlled by the last $\overline{CAS}$ to go high.
26. Each $\overline{CAS}$ must meet minimum pulse width.
27. Last $\overline{CAS}$ to go low.
28. All IOs controlled, regardless $\overline{CASL}$ and $\overline{CASH}$.
29. Data outputs are measured with a load of 50pF. The output reference levels are V_{OH}/V_{OL} =2.0V/0.8V; The input levels are V_{IH}/V_{IL}= 3.0V/0V.

READ CYCLE

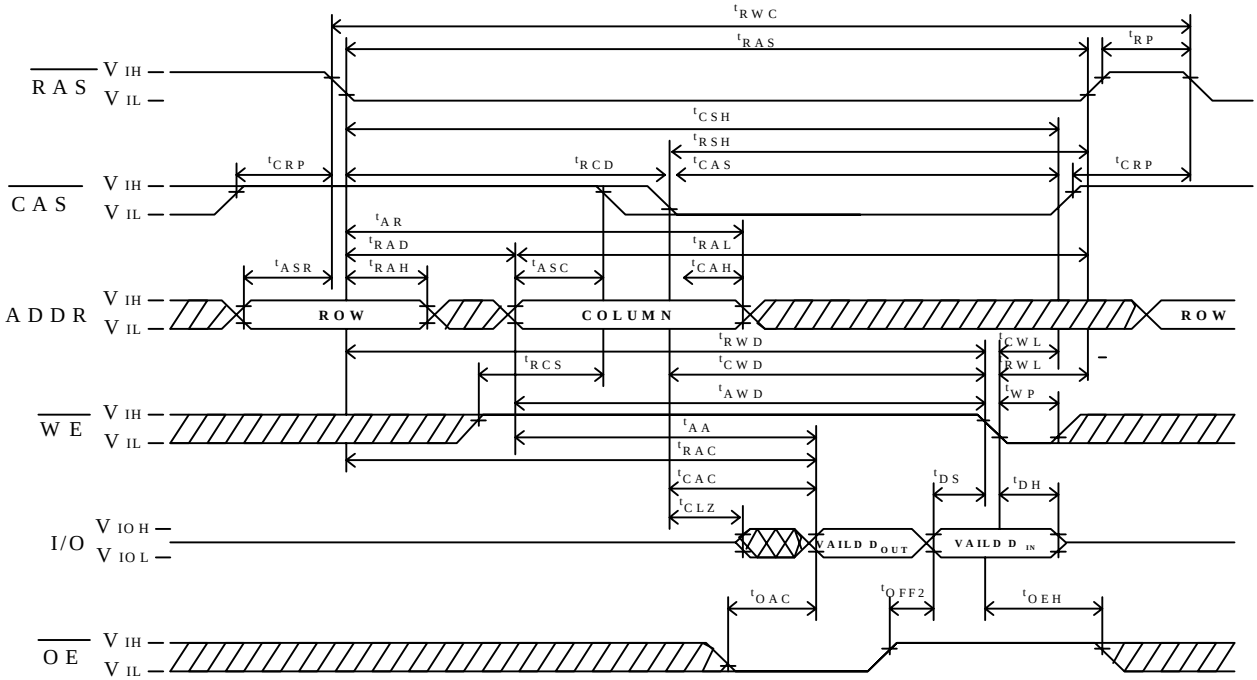


EARLY WRITE CYCLE

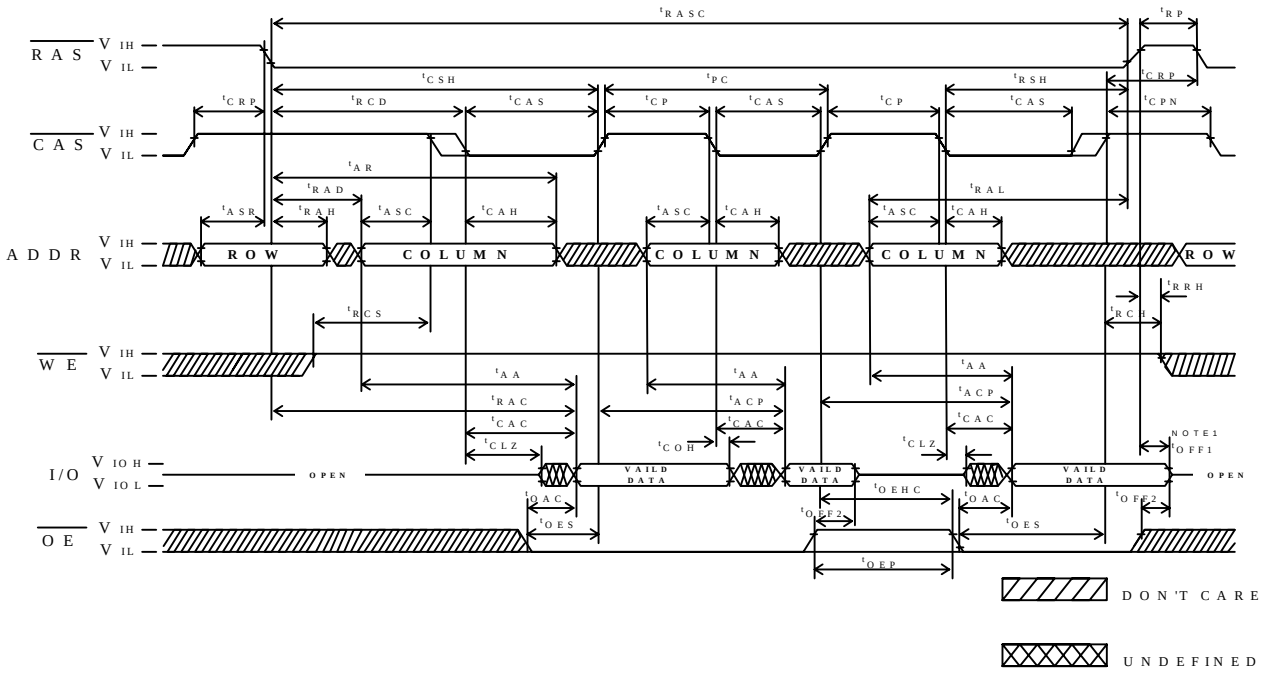


Note: 1. t_{OFF1} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



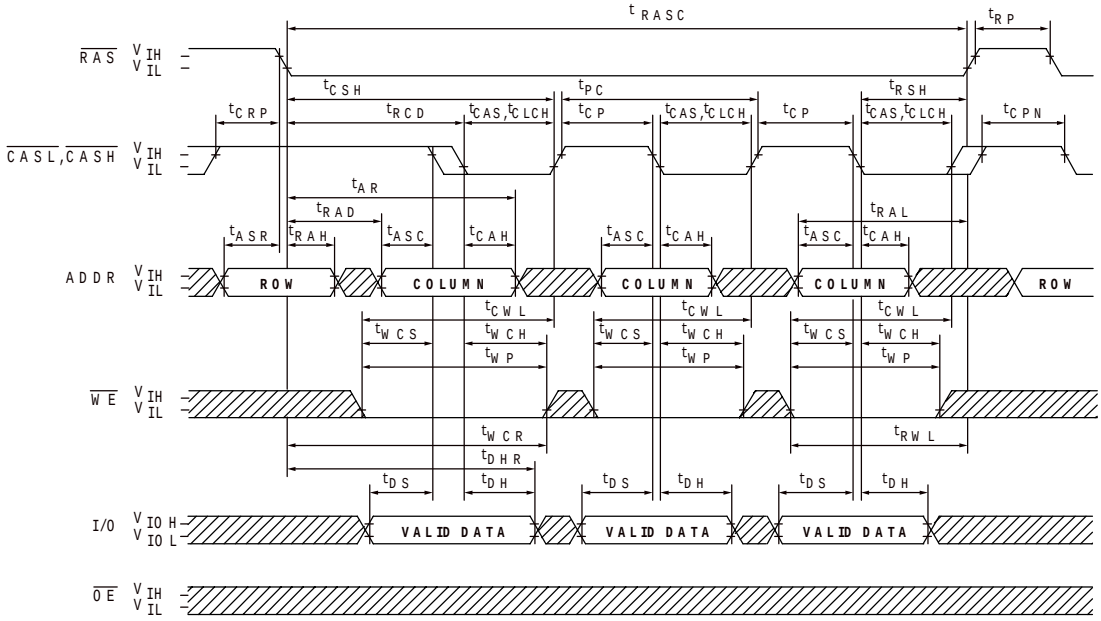
EDO-PAGE-MODE READ CYCLE



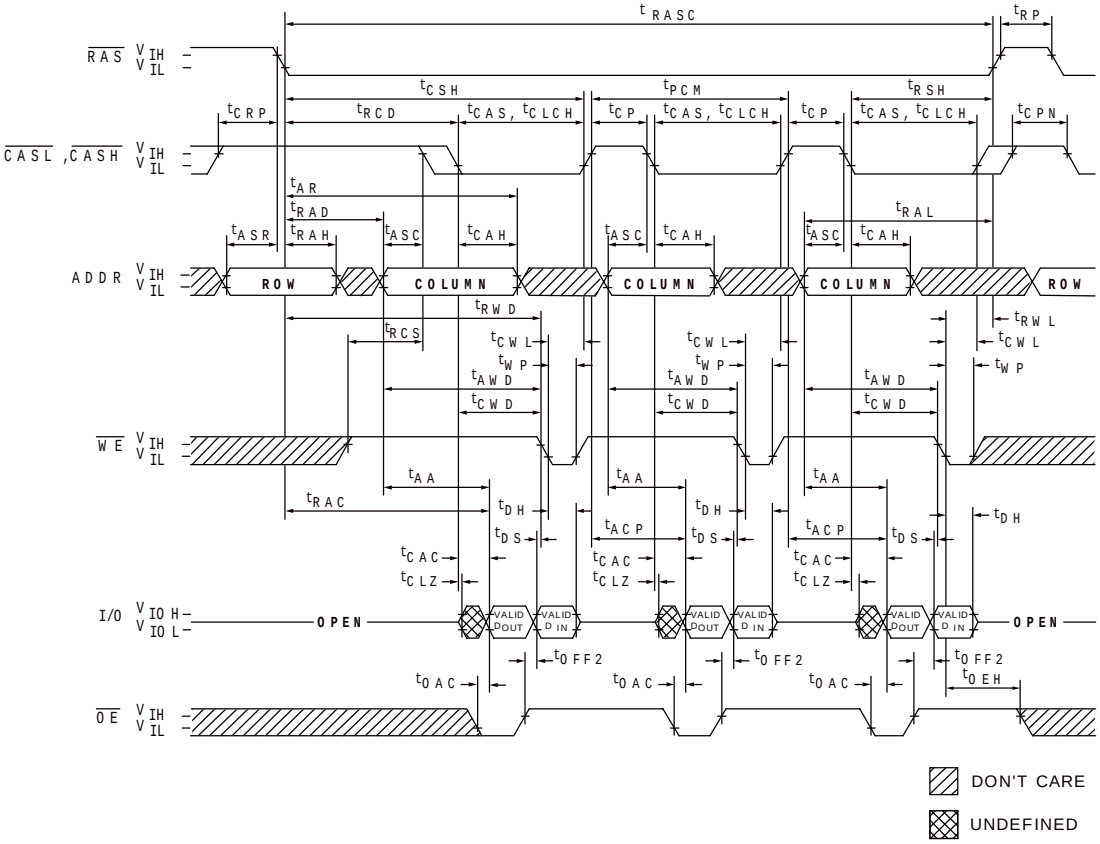
Note: 1. t_{OFF1} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

2. t_{PC} can be measured from falling edge of $\overline{CAS}$ to falling edge of $\overline{CAS}$, or from rising edge of $\overline{CAS}$ to rising edge of $\overline{RAS}$. Both measurements must meet the t_{PC} specification.

EDO-PAGE-MODE EARLY-WRITE CYCLE

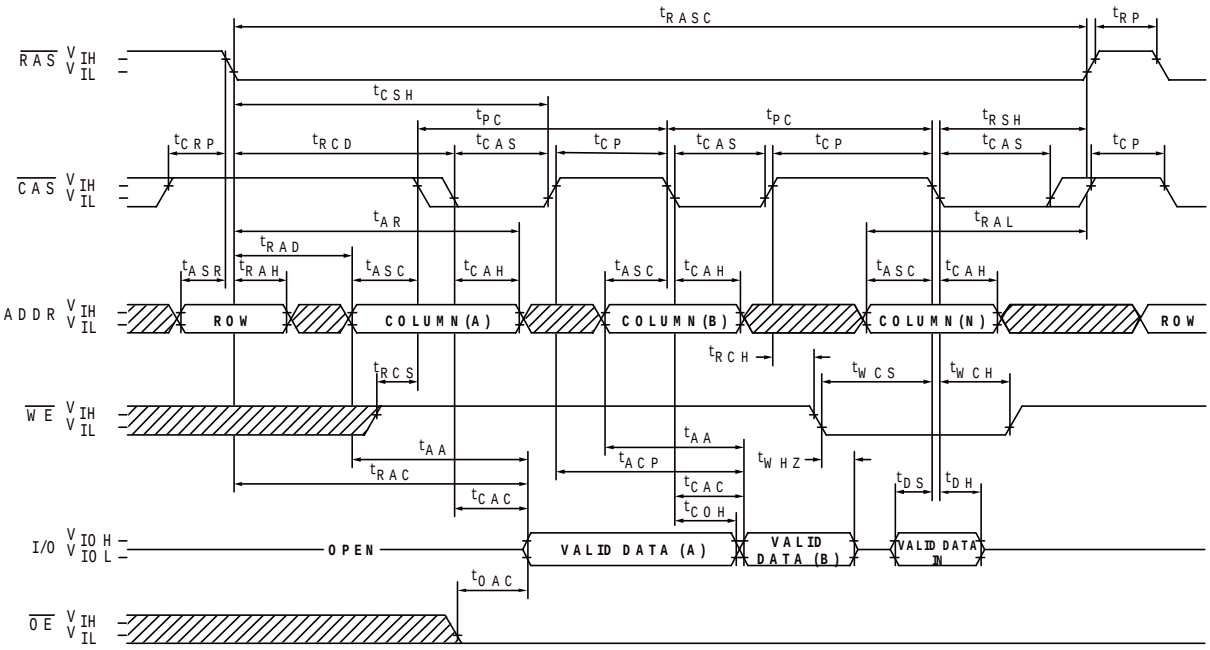


EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)

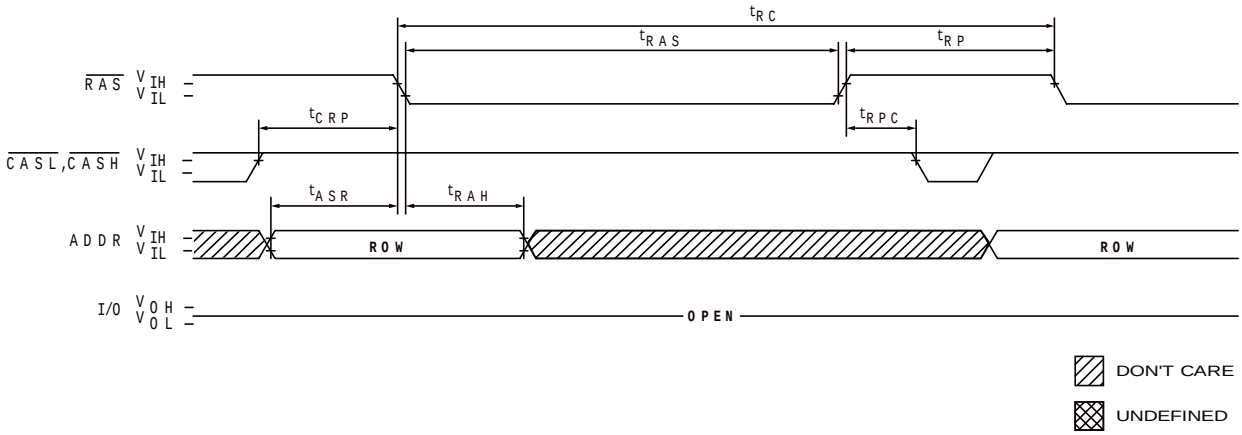


Note: 1. t_{PC} can be measured from falling edge to falling edge of $\overline{CAS}$, or from rising edge to rising edge of $\overline{CAS}$. Both measurements must meet the t_{PC} specification.

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Psuedo READ-MODIFY-WRITE)

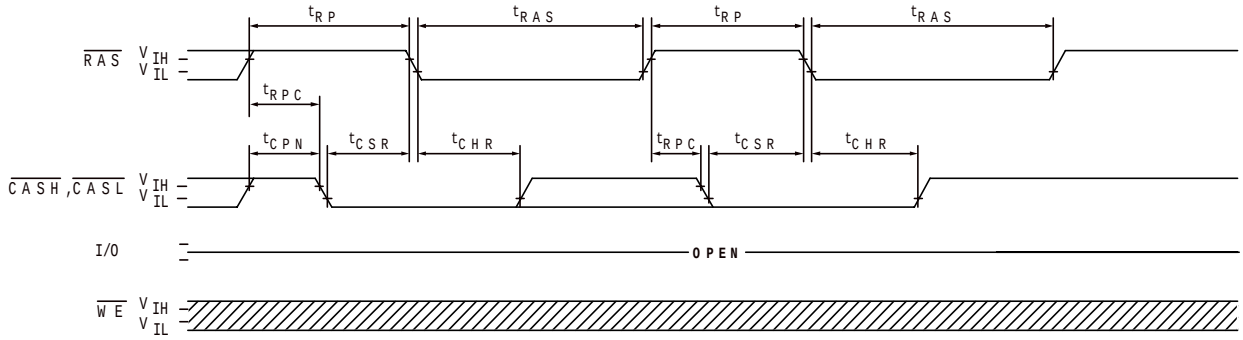


$\overline{\text{RAS}}$ ONLY REFRESH CYCLE
(ADDR=A0-A8 ; $\overline{\text{OE}}$, $\overline{\text{WE}}$=DON'T CARE)



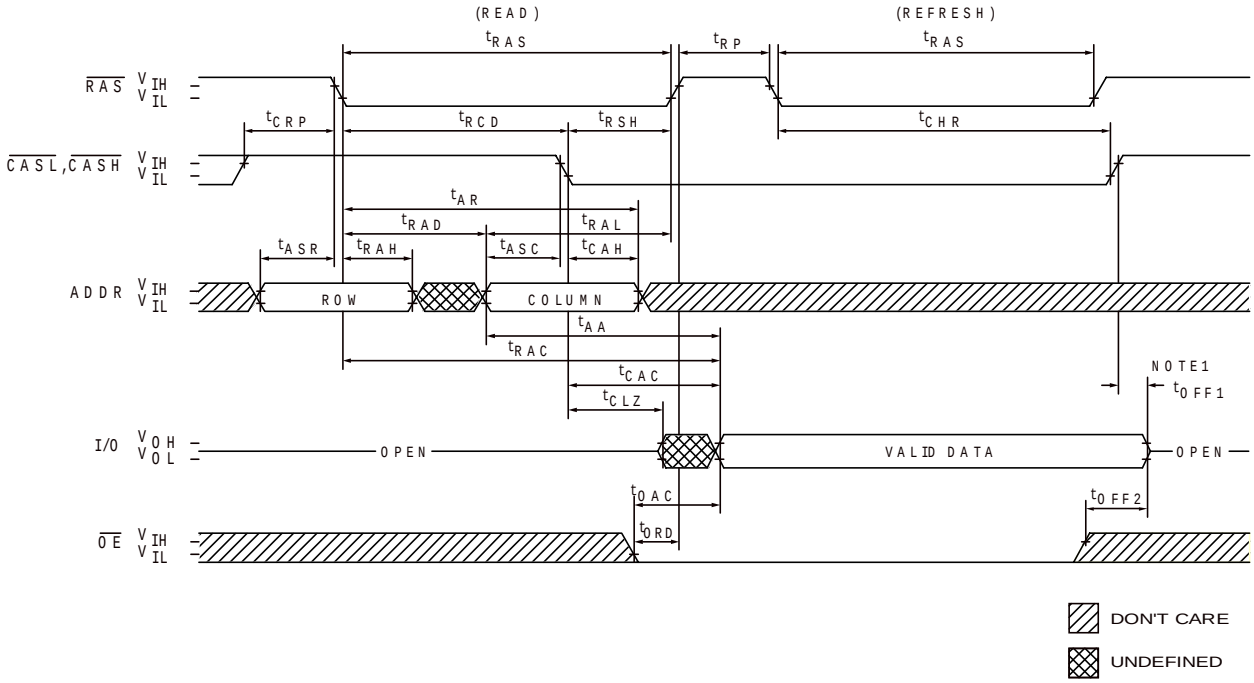
CBR REFRESH CYCLE

(A0-A8 ; $\overline{OE}$ =DON'T CARE)



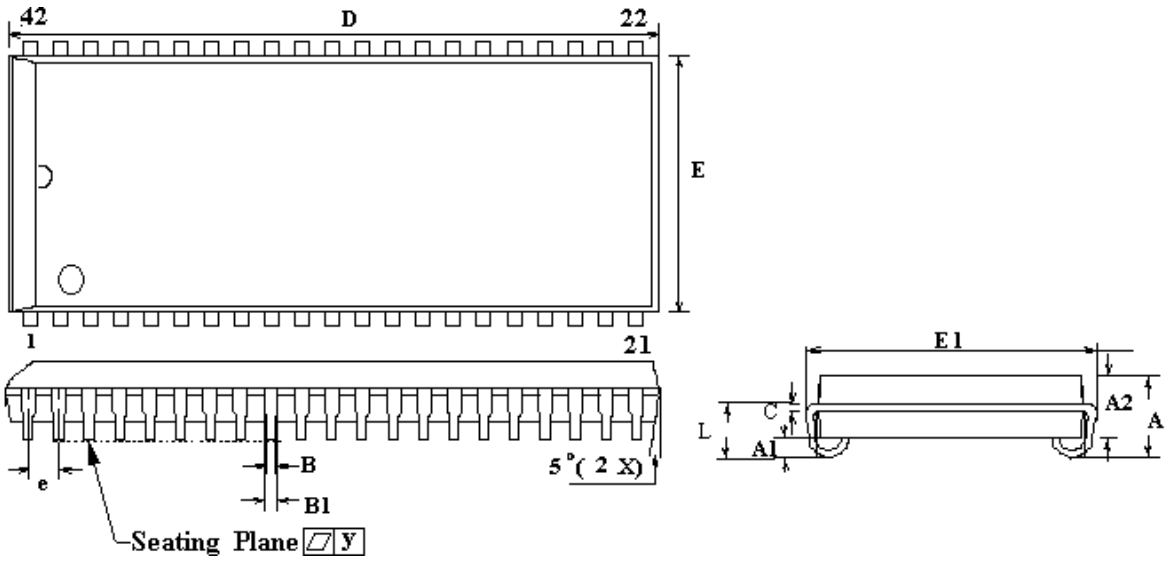
HIDDEN REFRESH CYCLE

($\overline{WE}$ =HIGH ; $\overline{OE}$ =LOW)



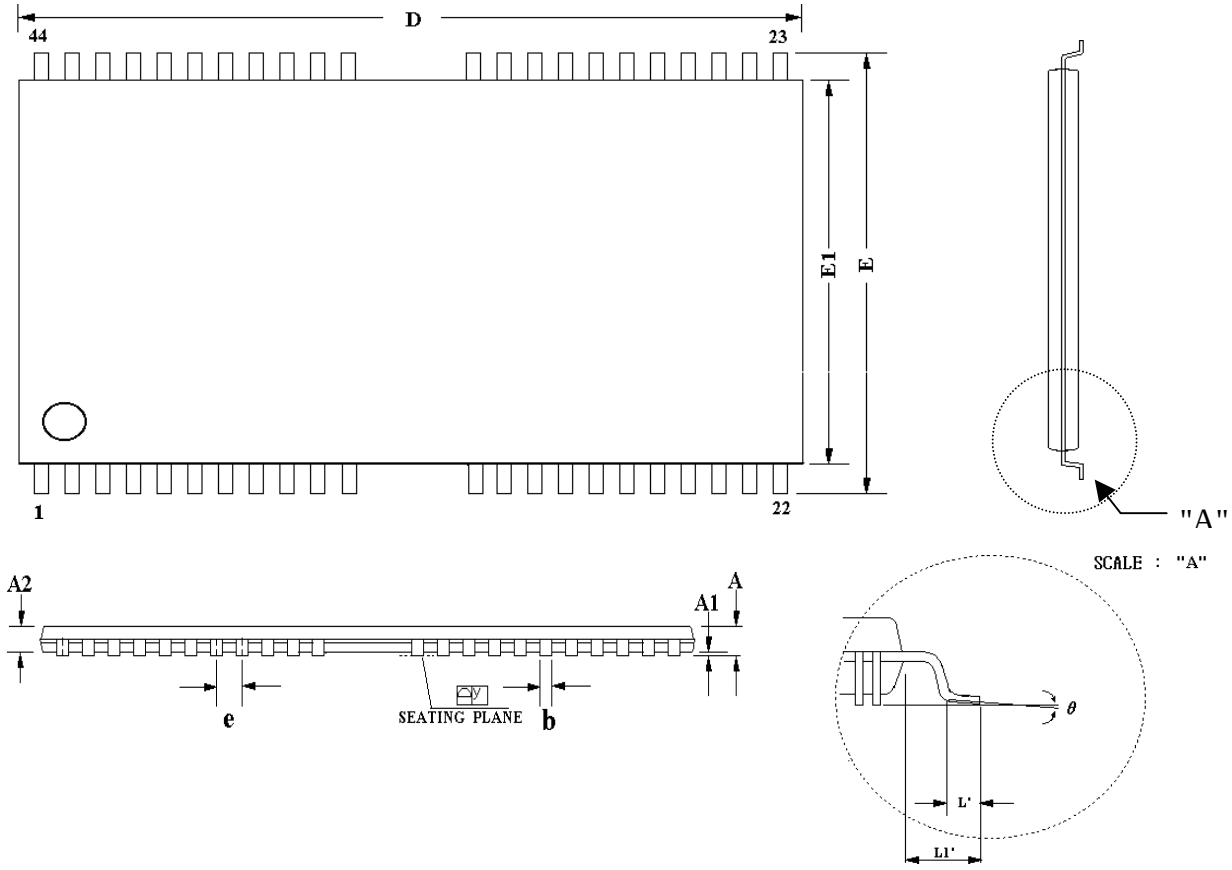
Note: 1. t_{OFF1} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

PACKAGE DIMENSIONS
42-LEAD SOJ DRAM (400 mil)



SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.128~0.148	3.251~3.759
A1	0.025(MIN)	0.635(MIN)
A2	0.105~0.115	2.657~2.920
B	0.026~0.032	0.660~0.813
b	0.015~0.020	0.381~0.508
c	0.007~0.013	0.178~0.330
D	1.070~1.080	27.178~27.432
E	0.395~0.405	10.033~10.287
e	0.050	1.270
E1	0.435~0.445	11.049~11.303
L	0.082(MIN)	2.083(MIN)
y	0.004(MAX)	0.102(MAX)

PACKAGE DIMENSIONS
44/50L LEAD TSOPII DRAM (400 mil)



SYMBOL	DIMENSIONS IN INCHES	DIMENSIONS IN MM
A	0.047	1.200(MAX)
A1	0.002~0.006	0.050~0.150
A2	0.037~0.041	0.950~1.050
b	0.012~0.018	0.300~0.450
c	0.005~0.008	0.120~0.210
D	0.820~0.830	20.820~21.080
E	0.455~0.471	11.560~11.960
e	0.031	0.800
E1	0.395~0.405	10.030~10.290
L	0.016~0.024	0.400~0.600
L1	0.031	0.800
θ	0°~5°	0°~5°