

T6C24

ROW DRIVER LSI FOR A DOT MATRIX LCD

The T6C24 is a row (common) driver LSI for a dot matrix LCD. The T6C24 generates the timing signals for the display using a built-in oscillator and also controls the T6C23 column (segment) LCD driver.

The T6C24 features a low-impedance 240-output row driver. The T6C24 also includes internal resistors to divide the bias voltage, a power supply op-amp and a contrast control circuit. The T6C24 can be used in conjunction with the T6C23 to construct a low-power LCD system.

Features

- Dot matrix graphic LCD row driver
- Built-in oscillator (additional external resistor)
- Duty : 1/240
- Display OFF function : /DSPOF = L, all LCD outputs = VSS
- Low power consumption
- Logic power supply : 2.7 to 5.5 V
- LCD power supply : 8.0 V to 30.0 V
- CMOS process
- Package : TCP (Tape Carrier Package)

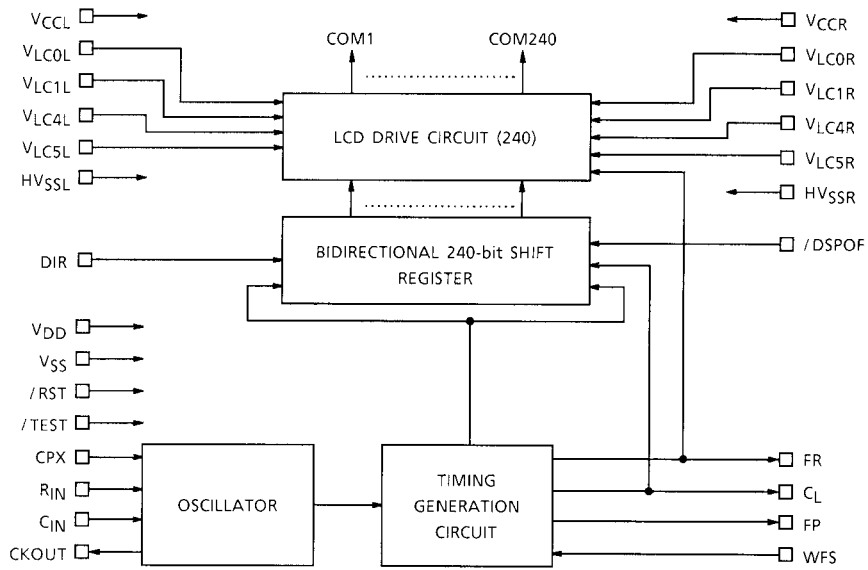
Unit: mm

T6C24	LEAD PITCH	
	IN	OUT
(UAW)	1.2	0.22
(UBW)	1.2	0.21
(UFW, 6FS)	1.2	0.21

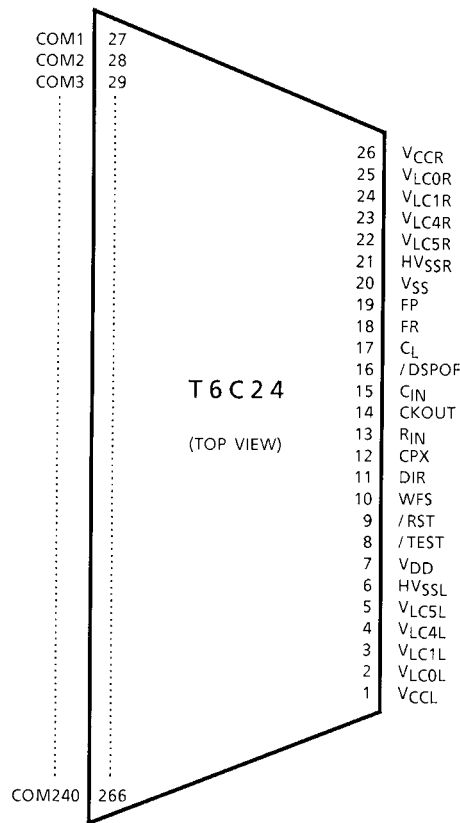
Please contact Toshiba or on authorized Toshiba dealer for information on package dimensions.

TCP (Tape Carrier Package)

Block Diagram



Pin Assignment



Note: The above diagram shows the pin configuration of the LSI chip; it does not show the configuration of the tape carrier package.

Pin Functions

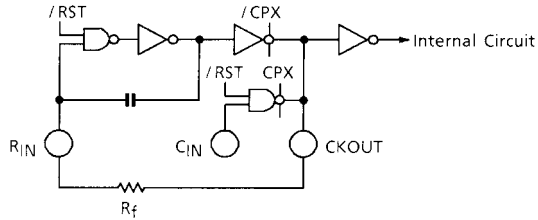
Pin Name	Pin No.	I / O	Functions						
COM1 to COM240	27 to 266	Output	Row driver outputs						
C _L	17	Output	Shift clock pulse						
FP	19	Output	Display synchronous signal						
FR	18	Output	Frame signal						
DIR	11	Input	Data flow direction select. Usually connected to V _{DD} <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DIR</th> <th>DATA FLOW</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>COM1 → COM240</td> </tr> <tr> <td>L</td> <td>COM240 → COM1</td> </tr> </tbody> </table>	DIR	DATA FLOW	H	COM1 → COM240	L	COM240 → COM1
DIR	DATA FLOW								
H	COM1 → COM240								
L	COM240 → COM1								
WFS	10	Input	Frame signal inversion select. Usually connected to V _{DD} . WFS = H: FR phase change per 13 lines. WFS = L: FR phase change per 17 lines.						
/ DSPOF	16	Input	Display off. Usually connected to V _{DD} / DSPOF = H: Display-on mode, (COM1 to COM240) are operational. / DSPOF = L: Display-off mode, (COM1 to COM240) are at the V _{SS} level.						
/ RST	9	Input	/ RST = L: Reset state. Usually connected to V _{DD}						
CPX	12	Input	Crystal oscillation / CR oscillation Select CPX = L : CR oscillation CPX = H: Crystal oscillation or external clock input from C _{IN}						
R _{IN}	13	Input	Connected to resistor for built-in oscillator						
C _{IN}	15	Input	Connected to crystal						
CKOUT	14	Output	Connected to resistor or crystal for built-in oscillator						
/ TEST	8	Input	Test pin. Usually connected to V _{DD}						
V _{DD} , V _{SS}	7, 20	—	Power supply						
V _{CCL} , V _{CCR} V _{LC0L} , V _{LC0R} V _{LC1L} , V _{LC1R} V _{LC4L} , V _{LC4R} V _{LC5L} , V _{LC5R} HV _{SSL} , HV _{SSR}	1, 26 2, 25 3, 24 4, 23 5, 22 6, 21	—	Power supply for LCD drive						

Function of Each Block

- **Oscillator**

The T6C24 has an on-chip oscillator (an external resistor is required).

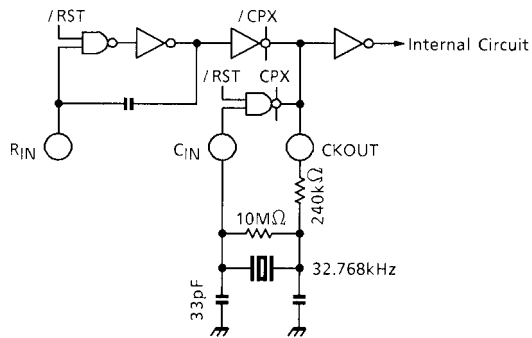
(1) **CPX = L**



R_f	f_{osc}
390 k Ω	54 kHz
620 k Ω	34 kHz
780 k Ω	27 kHz

Note: The resistor values are typical values. The oscillation frequency depends on how the device has been mounted. Hence R_f must be adjusted to achieve the target oscillation frequency.

(2) **CPX = H**



- **Timing generation circuit**

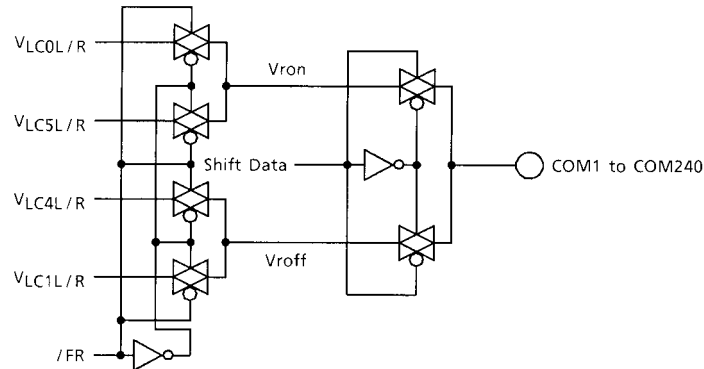
This circuit divides the oscillator frequency and generates the display timing signals (CL, FP and FR).

- **Shift register**

240-bit shift register

• Row driver circuit and LCD voltage generation circuit

The T6C24 has 240 row drivers and four different LCD drive output voltage levels. The display data from the latch circuit and the M signal determine which of the four LCD drive voltage is selected. The voltage generation circuit and row driver circuit are shown in the following diagram.



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage (1)	V _{DD} (Note 2)	-0.3 to 7.0	V
Supply Voltage (2)	(Note 1, 2)	-0.3 to 32.0	V
Input Voltage	V _{in} (Note 2, 3)	-0.3 to V _{DD} + 0.3	V
Operating Temperature	T _{opr}	-20 to 75	°C
Storage Temperature	T _{stg}	-55 to 125	°C

Note 1: V_{CCL}, V_{CCR}, V_{LC0L}, V_{LC0R}, V_{LC1L}, V_{LC1R}, V_{LC4L}, V_{LC4R}, V_{LC5L} and V_{LC5R}

Note 2: Referenced to V_{SS}, HV_{SSL} and HV_{SSR}

Note 3: Applies to all data bus and I/O pins.

Note 4: Ensure that the following condition is always maintained.

$$V_{CCL/R} \geq V_{LC0L/R} \geq V_{LC1L/R} \geq V_{LC4L/R} \geq V_{LC5L/R} \geq HV_{SSL/R}$$

Electrical Characteristics

DC Characteristics

Test Conditions (1)

(Unless Otherwise Noted, $V_{SS} = 0\text{ V}$, $V_{DD} = 3.0\text{ V} \pm 10\%$, $V_{CCL/R} = 23.0\text{ V} \pm 10\%$,
 $T_a = -20\text{ to }75^\circ\text{C}$)

Item	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Operating Supply (1)	V_{DD}	—	—	2.7	—	3.3	V	V_{DD}
Operating Supply (2)	V_{CC}	—	—	8.0	—	30.0	V	V_{CCL} , V_{CCR}
Input Voltage	H Level	V_{IH}	—	0.7 V_{DD}	—	V_{DD}	V	WFS , CPX , DIR , / $DSPOF$, / RST , / $TEST$
	L Level	V_{IL}	—	0	—	0.3 V_{DD}	V	
Output Voltage	H Level	V_{OH}	—	$V_{DD} - 0.4$	—	—	V	C_L , FP , FR
	L Level	V_{OL}	—	V_{SS}	—	$V_{SS} + 0.4$	V	
Row Driver Output Resistance	R_{row}	—	(Note 5) Load voltage = output level of 0.5 V	—	—	1.5	k Ω	COM1 to COM240
Input Leakage	I_{IL}	—	$V_{IN} = V_{DD}$ to GND	-1	—	1	μA	WFS , CPX , DIR , / $DSPOF$, / RST , / $TEST$
Current Consumption (1)	I_{SS}	—	(Note 1)	—	-35	-50	μA	V_{DD}
Current Consumption (2)	I_{CC}	—	(Note 2)	—	10	20	μA	V_{CCL} , V_{CCR} V_{LC0L} , V_{LC0R}
Current Consumption (3)	I_{DOF}	—	(Note 3)	—	25	40	μA	V_{SS} , V_{SSL} , V_{SSR} V_{LC5L} , V_{LC5R}
Current Consumption (4)	I_{STB}	—	(Note 4)	-1	—	1	μA	V_{SS} , V_{SSL} , V_{SSR} V_{LC5L} , V_{LC5R}
Operating Freq.	f_{osc}	—	—	20	—	100	kHz	R_{IN} , C_{IN}
External Clock Frequency	f_{ex}	—	—	20	—	100	kHz	C_{IN}
External Clock Duty	f_{duty}	—	—	40	50	60	%	C_{IN}
External Clock Rise / Fall Time	t_r / t_f	—	—	—	—	50	ns	C_{IN}

Note 1: Logic current : $V_{DD} = 3.0\text{ V} \pm 10\%$, $T_a = 25^\circ\text{C}$, $R_f = 620\text{ k}\Omega$ (33.6 kHz), no load

Note 2: LCD driver current : $V_{DD} = 3.0\text{ V} \pm 10\%$, $V_{CCL/R} = 23.0\text{ V}$, $T_a = 25^\circ\text{C}$, 1 / 13 bias,
 $R_f = 620\text{ k}\Omega$, no load

Note 3: Display-off current : $V_{DD} = 3.0\text{ V} \pm 10\%$, $V_{CCL/R} = 23.0\text{ V}$, $T_a = 25^\circ\text{C}$, 1 / 13 bias,
 $R_f = 620\text{ k}\Omega$, / $DSPOF = L$, no load

Note 4: Standby current : $V_{DD} = 3.0\text{ V} \pm 10\%$, $V_{CCL/R} = 23.0\text{ V}$, $T_a = 25^\circ\text{C}$, 1 / 13 bias,
 $R_f = 620\text{ k}\Omega$, / $RST = L$, no load

Note 5: $V_{CCL/R} = V_{LC0L/R} = 23.0\text{ V}$, $V_{LC1L/R} = V_{CC} \times 12 / 13$, $V_{LC4L/R} = V_{CC} \times 1 / 13$,
 $HV_{SSL/R} = V_{LC5L/R} = 0\text{ V}$

Test Conditions (2)

(Unless Otherwise Noted, $V_{SS} = 0\text{ V}$, $V_{DD} = 5.0\text{ V} \pm 10\%$, $V_{CCL/R} = 23.0\text{ V} \pm 10\%$,
 $T_a = -20\text{ to }75^\circ\text{C}$)

Item	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name
Operating Supply (1)	V_{DD}	—	—	4.5	—	5.5	V	V_{DD}
Operating Supply (2)	V_{CC}	—	—	8.0	—	30.0	V	V_{CCL} , V_{CCR}
Input Voltage	H Level	V_{IH}	—	0.7 V_{DD}	—	V_{DD}	V	WFS , CPX , DIR , / $DSPOF$, / RST , / $TEST$
	L Level	V_{IL}	—	0	—	0.3 V_{DD}	V	
Output Voltage	H Level	V_{OH}	—	$V_{DD} - 0.4$	—	—	V	C_L , FP , FR
	L Level	V_{OL}	—	V_{SS}	—	$V_{SS} + 0.4$	V	
Row Driver Output Resistance	R_{row}	—	(Note 5) Load voltage = output level of 0.5 V	—	—	1.5	k Ω	COM1 to COM240
Input Leakage	I_{IL}	—	$V_{IN} = V_{DD}$ to GND	-1	—	1	μA	WFS , CPX , DIR , / $DSPOF$, / RST , / $TEST$
Current Consumption (1)	I_{SS}	—	(Note 1)	—	-60	-90	μA	V_{DD}
Current Consumption (2)	I_{CC}	—	(Note 2)	—	10	20	μA	V_{CCL} , V_{CCR} V_{LC0L} , V_{LC0R}
Current Consumption (3)	I_{DOF}	—	(Note 3)	—	50	80	μA	V_{SS} , V_{SSL} , V_{SSR} V_{LC5L} , V_{LC5R}
Current Consumption (4)	I_{STB}	—	(Note 4)	-1	—	1	μA	V_{SS} , V_{SSL} , V_{SSR} V_{LC5L} , V_{LC5R}
Operating Freq.	f_{osc}	—	—	20	—	100	kHz	R_{IN} , C_{IN}
External Clock Frequency	f_{ex}	—	—	20	—	100	kHz	C_{IN}
External Clock Duty	f_{duty}	—	—	40	50	60	%	C_{IN}
External Clock Rise / Fall Time	t_r / t_f	—	—	—	—	50	ns	C_{IN}

Note 1: Logic current : $V_{DD} = 5.0\text{ V} \pm 10\%$, $T_a = 25^\circ\text{C}$, $R_f = 620\text{ k}\Omega$ (33.6 kHz), no load

Note 2: LCD driver current : $V_{DD} = 5.0\text{ V} \pm 10\%$, $V_{CCL/R} = 23.0\text{ V}$, $T_a = 25^\circ\text{C}$, 1 / 13 bias,
 $R_f = 620\text{ k}\Omega$, no load

Note 3: Display-off current : $V_{DD} = 5.0\text{ V} \pm 10\%$, $V_{CCL/R} = 23.0\text{ V}$, $T_a = 25^\circ\text{C}$, 1 / 13 bias,
 $R_f = 620\text{ k}\Omega$, / $DSPOF = L$, no load

Note 4: Standby current : $V_{DD} = 5.0\text{ V} \pm 10\%$, $V_{CCL/R} = 23.0\text{ V}$, $T_a = 25^\circ\text{C}$, 1 / 13 bias,
 $R_f = 620\text{ k}\Omega$, / $RST = L$, no load

Note 5: $V_{CCL/R} = V_{LC0L/R} = 23.0\text{ V}$, $V_{LC1L/R} = V_{CC} \times 12 / 13$, $V_{LC4L/R} = V_{CC} \times 1 / 13$,
 $HV_{SSL/R} = V_{LC5L/R} = 0\text{ V}$

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