TOSHIBA Bipolar Linear Integrated Circuit Silicon Monolithic

T6L24

Source Driver for TFT LCD Panels

The T6L24 is a 240-channel-output source driver for TFT LCD panels.
The T6L24 offers both low power consumption and high integration circuit due to CMOS technology.

Unit : mm

T6L24	USER AREA PITCH	
	IN	OUT
(SDN, 5ES)	0.85	0.09

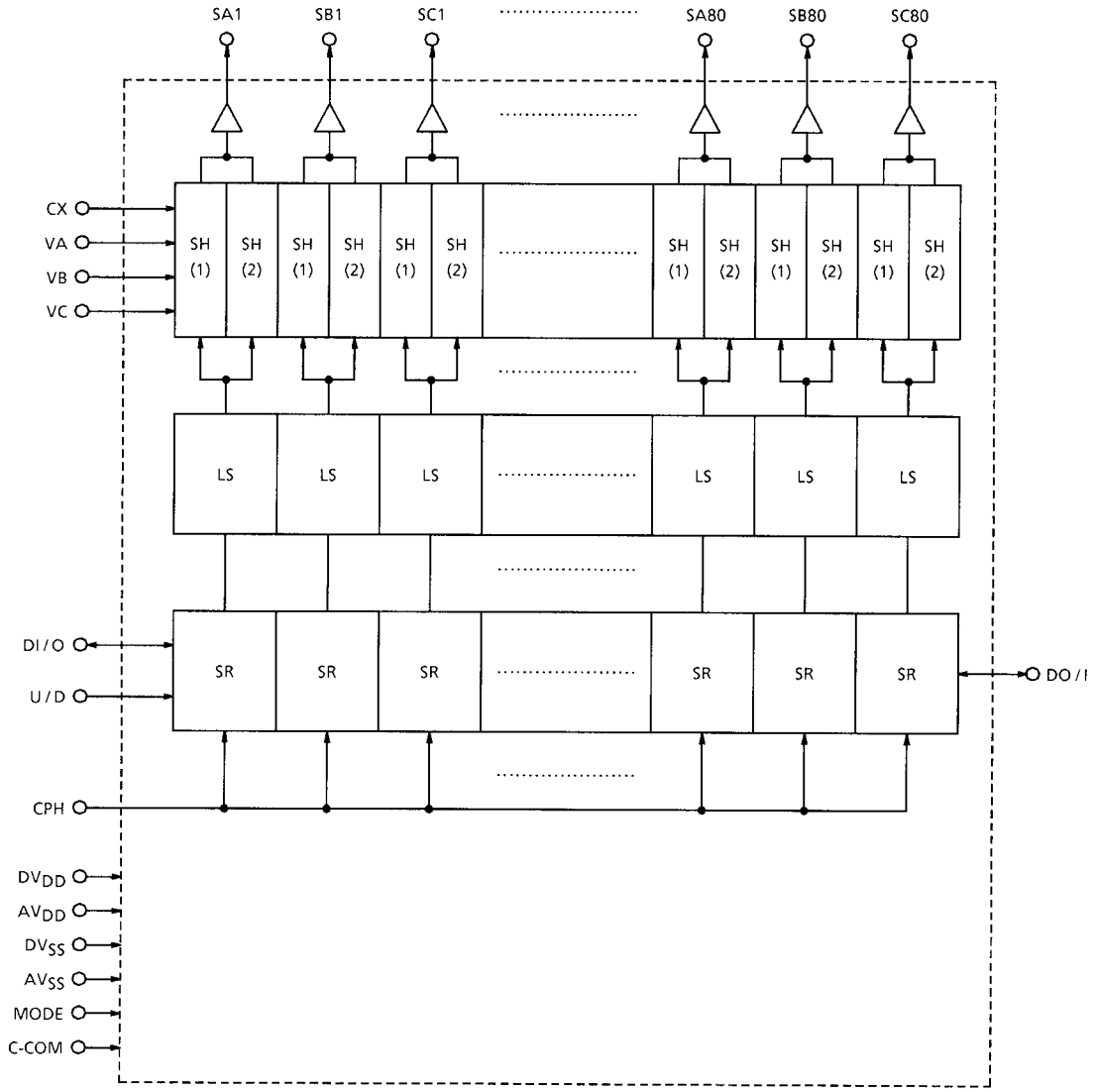
Please contact Toshiba or an authorized Toshiba dealer for information on package dimensions.

TCP (Tape Carrier Package)

Features

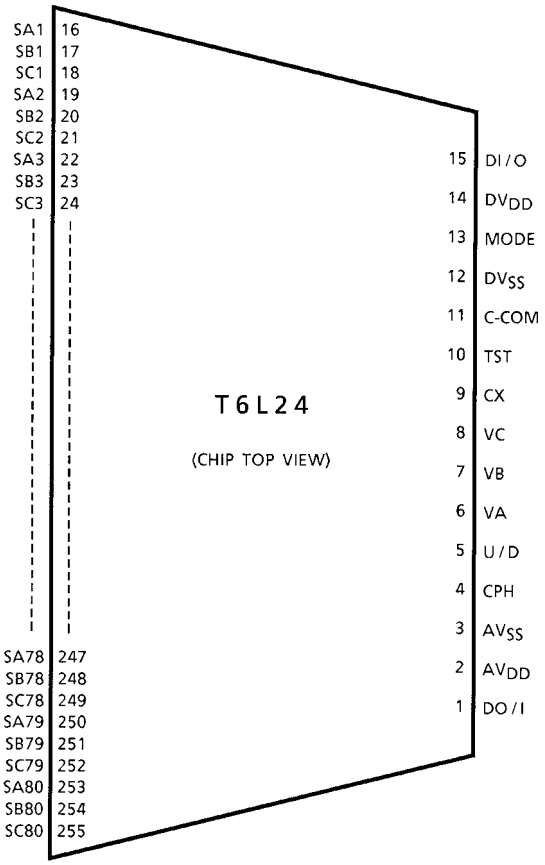
- LCD drive outputs : 240 outputs (80 outputs each for R, G and B)
- Power supply voltage : Digital power supply voltage ...2.7 to 5.5 V
  Analog power supply voltage ...Max 5.5 V
- Sampling method : 2 latches
- Data transfer method : Bi directional shift register
- Operating temperature : −20 to 75°C
- Package : Tape carrier package (TCP)
- Switching simultaneous/sequential sampling

Block Diagram



SR : Shift Register
LS : Level Shifter
SH : Sample-and-Hold Circuit

Pin Assignment



The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributor for the latest TCP specification.

Pin Function

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>DI/O
DO/I</td><td>I/O</td><td>Vertical shift data I/O pins
These pins are used to input and output shift data. These pins are switched between input and output by setting the U/D pin as shown below:
<table>
<tr><th>U/D</th><th>DI/O</th><th>DO/I</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table>
When set for input
● When MODE = low
The data is latched into the internal logic synchronously with the rising edge of CPH. The data is sampling in sequentially, starting at the rise of CPH after three clock period.
● When MODE = high
The data is latched into the internal logic synchronously with the rising edge of CPH. The data is sampling in sequentially, starting at the next rise of CPH.
When set for output
When two or more T6L24s are cascaded, this pin outputs the data to be fed into the next stage.</td></tr>
<tr><td>U/D</td><td>I</td><td>Transfer direction select pin
This pin specifies the direction of sampling performed by the sample-and-hold circuit.
● When MODE = low
When U/D is high, data is sampled in the sequence
SA1 → SB1 → SC1 → SA2 → SB2 → · · · → SC80
When U / D is low, the sequence is reversed to give
SC80 → SB80 → SA80 → SC79 → · · · → SA1
● When MODE = high
When U/D is high, data is sampled in the sequence
SA1, SB1, SC1 → SA2, SB2, SC2 → · · · → SA80, SB80, SC80
When U/D is low, the sequence is reversed to give
SC80, SB80, SA80 → SC79, SB79, SA79 → · · · → SC1, SB1, SA1</td></tr>
<tr><td>CPH</td><td>I</td><td>Shift clock input
This clock sequentially shift the signals necessary to sample the data that are output to the LCD drive output pins (QA1 to QC80).</td></tr>
<tr><td>CX</td><td>I</td><td>Sample-and-hold switching pin.
This pin switches between two sample−and−hold circuits.</td></tr>
<tr><td>MODE</td><td>I</td><td>Sampling mode setting pin.
● When MODE = high
Simultaneously samples three video output signals corresponding to the LCD drive outputs.
● When MODE = low
Sequentially samples the video output signals corresponding to the LCD drive outputs.</td></tr>
<tr><td>VA
VB
VC</td><td>I</td><td>Analog signal input
These pins accept as their input the analog signals that are output to the LCD drive output pins.</td></tr>
<tr><td>C-COM</td><td>I</td><td>Sample and hold reference voltage input
This is the reference voltage for the sample-and-hold circuit.
Apply stable DC voltage to the pin.</td></tr>
<tr><td>QA1 to QA80
QB1 to QB80
QC1 to QC80</td><td>O</td><td>LCD drive output pins
These pins output one of the analog signal inputs (VA, VB and VC) after it has been sampled and held by the sample-and-hold circuit.</td></tr>
<tr><td>DV_{DD}</td><td>—</td><td>Power supply for the device’s logic block</td></tr>
<tr><td>AV_{DD}</td><td>—</td><td>Power supply for the device’s high−voltage block</td></tr>
<tr><td>DV_{SS}</td><td>—</td><td>Digital GND for the device</td></tr>
<tr><td>AV_{SS}</td><td>—</td><td>Analog GND for the device</td></tr>
<tr><td>TST</td><td>—</td><td>Test pin
Use the pin as required.</td></tr>
</table>

Device Operation

(1) Analog signal sampling

Data transfer begins with the assertion of DI/O (U/D = high) or DO/I (U/D = low).

<Simultaneous sampling>

- **When MODE = high, U/D = high**

  A high on DI/O is latched into the internal logic synchronously with the rising edge of CPH, and the analog signal to be output to (SA1, SB1, SC1) is sampled at next rising edge of CPH. In this way, all analog signals are sampled of each three channel sequentially at the rising edge of CPH and so on, and the analog signals are output to (SA2, SB2, SC2), (SA3, SB3, SC3) and so on.
  After the device finishes sampling the data for (SA80, SB80, SC80), it automatically enters standby state. Unless DI/O is asserted again, no data is sampled, irrespective of whether CPH are input to the device.

- **When MODE = high, U/D = low**

  A high on DO/I is latched into the internal logic synchronously with the rising edge of CPH, and the analog signal to be output to (SA80, SB80, SC80) is sampled at next rising edge of CPH. In this way, all analog signals are sampled of each three channel sequentially at the rising edge of CPH and so on, and the analog signals are output to (SA79, SB79, SC79), (SA78, SB78, SC78) and so on.
  After the device finishes sampling the data for (SA1, SB1, SC1), it automatically enters standby state. Unless DO/I is asserted again, no data is sampled, irrespective of whether CPH are input to the device.

<Sequential sampling>

- **When MODE = low, U/D = high**

  A high on DI/O is latched into the internal logic synchronously with the rising edge of CPH, and the analog signal to be output to SA1 is sampled at the rising edge of CPH after three clock period. In this way, all analog signals are sampled sequentially at the rising edge of CPH and so on, and the analog signals are output to SB1, SC1, SA2, SB2, SC2, SA3, SB3, SC3 and so on.
  After the device finishes sampling the data for SC80, it automatically enters standby state. Unless DI/O is asserted again, no data is sampled, irrespective of whether CPH are input to the device.

- **When MODE = low, U/D = low**

  A high on DO/I is latched into the internal logic synchronously with the rising edge of CPH, and the analog signal to be output to SC80 is sampled at the rising edge of CPH after three clock period. In this way, all analog signals are sampled sequentially at the rising edge of CPH and so on, and the analog signals are output to SB80, SA80, SC79, SB79, SA79, SC78, SB78, SA78 and so on.
  After the device finishes sampling the data for SA1, it automatically enters standby state. Unless DO/I is asserted again, no data is sampled, irrespective of whether CPH are input to the device.

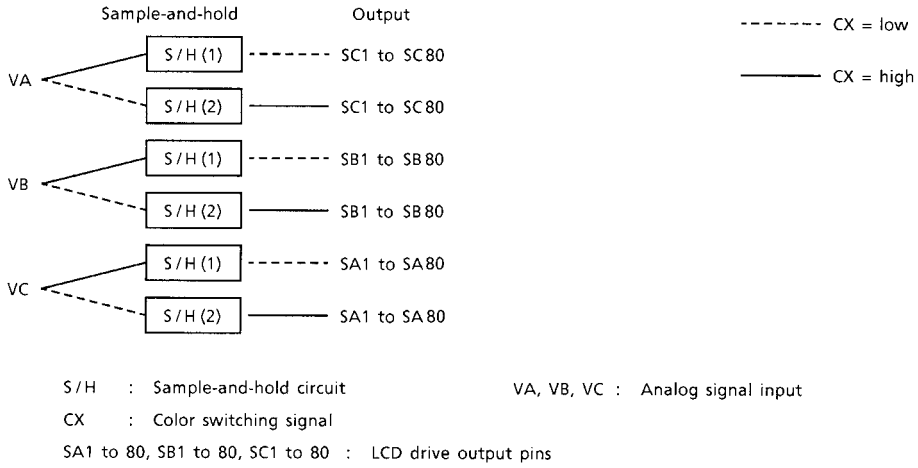
(2) LCD drive output

- The T6L24 has two sample-and-hold circuits called Sample-And-Hold (1) and (2).
  These two circuits alternate between serving as the output and the sample-and-hold. Which circuit fulfils which function is determined by the setting of the CX pin.

CX	Output	Sample-and-Hold
L	Sample-and-hold circuit (1)	Sample-and-hold circuit (2)
H	Sample-and-hold circuit (2)	Sample-and-hold circuit (1)

- The analog signal inputs VA, VB and VC are output as follows: VA is sent to the LCD driver output pins SC1 to SC80, VB is sent to output pins SB1 to SB80, and VC is sent to output pins SA1 to SA80. The analog signal inputs will be sent to LCD driver output pins by the setting of the CX pin as shown below:

  Note: The CX pin setting must not be altered while the device is sampling data.



S/H : Sample-and-hold circuit
VA, VB, VC : Analog signal input
CX : Color switching signal
SA1 to 80, SB1 to 80, SC1 to 80 : LCD drive output pins

(3) Vertical shift data output

- **When MODE = high**

  The output DO/I (U/D = high) or DI/O (U/D = low) is driven high for one clock period synchronously with the rising CPH, one clock period before the data (which is to be output to (SA80, SB80, SC80) or (SA1, SB1, SC1)) is latched into the shift register.

- **When MODE = low**

  The output DO/I (U/D = high) or DI/O (U/D = low) is driven high for one clock period synchronously with the rising CPH, one clock period before the data (which is to be output to SA80 or SC1) is latched into the shift register.

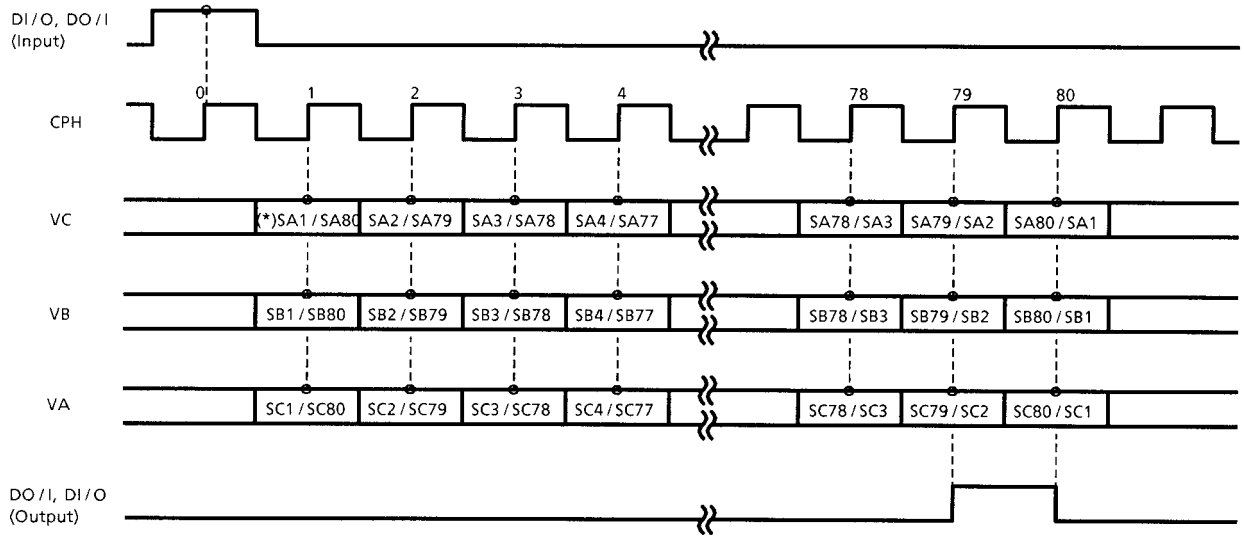
  When using two or more of these devices to drive a large screen, connect the vertical shift data output from the first stage of the LCD driver directly to the vertical shift data input at the next stage. In this way, the device's LCD drive output pin can easily be expanded as necessary.

(4) Sample-and-hold reference voltage (C-COM)

The device's sample-and-hold circuits are configured using the internal capacitors. The C-COM pin is used to supply the reference voltage for these circuits. Apply stable DC voltage to the pin.

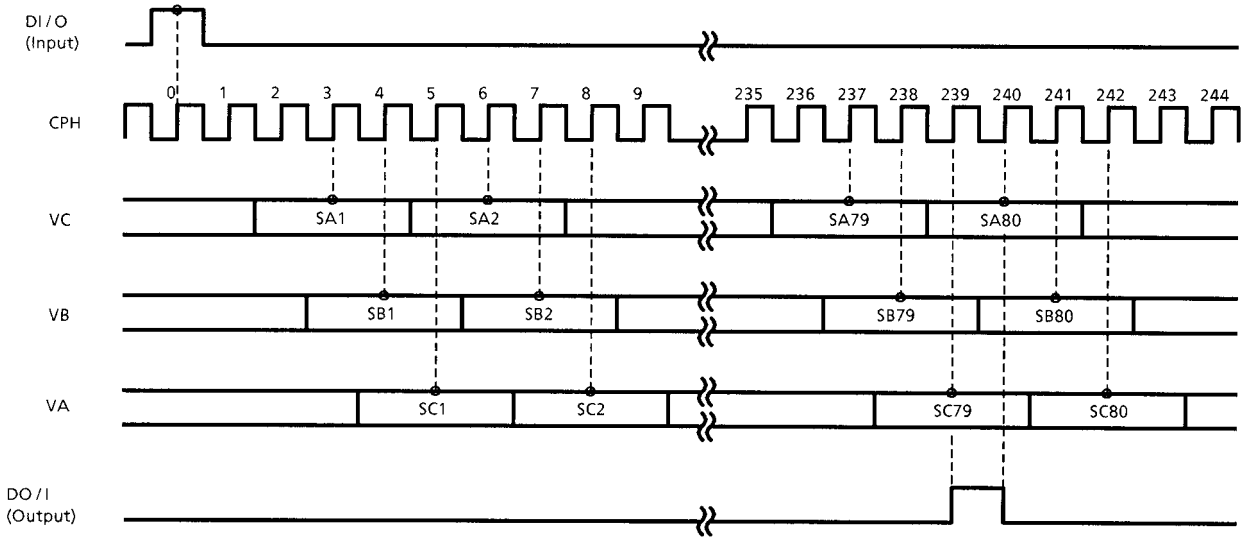
Timing Diagram

- **Simultaneous sampling (MODE = high)**

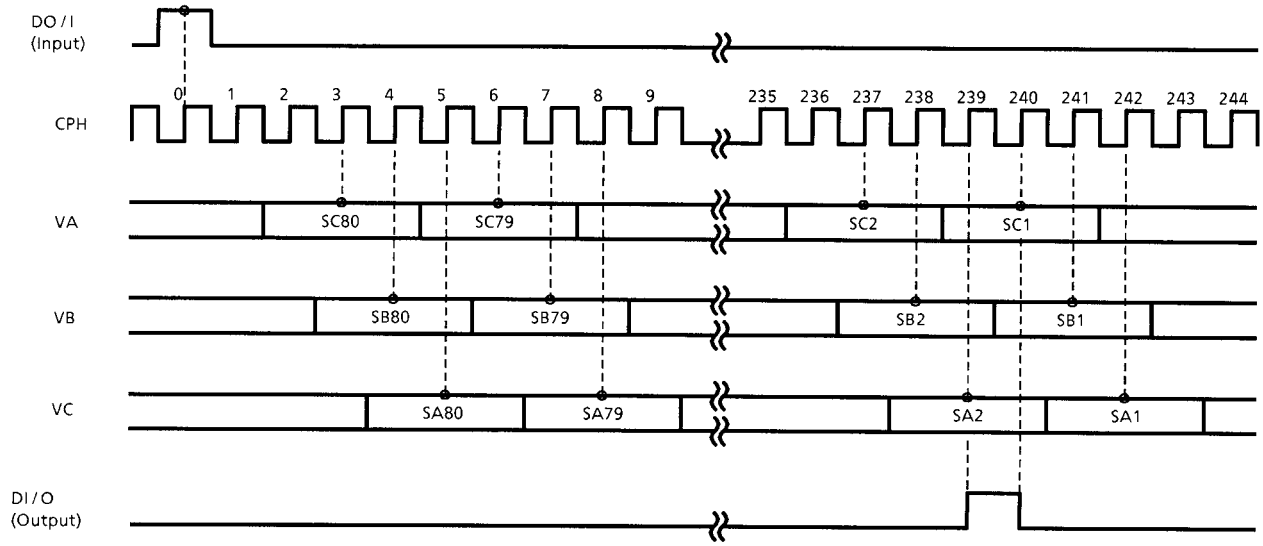


(*) SA1 / SC80 : SA1 → U / D = high
SA80 → U / D = low

- **Sequential sampling (MODE = low, U/D = high)**



- **Sequential sampling (MODE = low, U/D = low)**



Absolute Maximum Ratings (AV_{SS} = DV_{SS} = 0 V)

Parameter	Symbol	Rating	Unit	Relevant Pin
Supply Voltage (1)	DV_{DD}	−0.3 to 6.5	V	—
Supply Voltage (2)	AV_{DD}	−0.3 to 6.5	V	—
Digital Input Voltage	V_{IN}	−0.3 to DV_{DD} + 0.3	V	(Note 1)
Reference Analog Voltage	V_{ID}	−0.3 to AV_{DD} + 0.3	V	(Note 2)
Storage Temperature	T_{stg}	−55 to 125	°C	—

Recommended Operating Conditions (AV_{SS} = DV_{SS} = 0 V)

Parameter		Symbol	Rating	Unit	Relevant Pin
Supply Voltage (1)		DV_{DD}	2.7 to 5.5	V	—
Supply Voltage (2)		AV_{DD}	DV_{DD} to 5.5	V	—
Reference Analog Voltage		V_{ID}	0.2 to AV_{DD} − 0.2	V	(Note 2)
Operating Temperature		T_{OP}	−20 to 75	°C	—
Operating Frequency	MODE = high	f_{CLK}	0.5 to 15	—	—
	MODE = low	f_{CLK}	0.5 to 30	—	—
Output Load Capacitance		C_L	50 (max)	pF/PIN	—
Input Capacitance		C_{IN}	10 (max)	pF	—

Electrical Characteristics

DC Characteristics

(DV_{DD} = 3.0 ± 0.3 V, AV_{DD} = 5.0 ± 0.5 V, AV_{SS} = DV_{SS} = 0 V, Ta = −20 to 75°C)

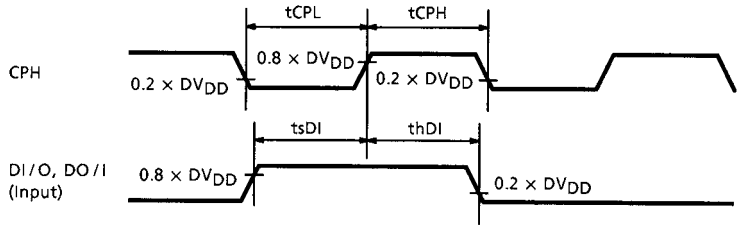
Parameter		Symbol	Test Circuit	Test Conditions	Min	Typ.	Max	Unit	Relevant Pin
Input Voltage	Low Level	V_{IL}	—	—	0	—	0.2 × DV_{DD}	V	(Note 1)
	High Level	V_{IH}		—	0.8 × DV_{DD}	—	DV_{DD}		
Output Voltage	Low Level	V_{OL}	—	I_{OL} = 40 μA	0	—	0.3	V	DI/O, DO/I
	High Level	V_{OH}		I_{OL} = −40 μA	V_{DD} − 0.3 V	—	DV_{DD}		
Output Offset Voltage		V_{OFF}	—	—	−20	—	—	mV	SA1 to SC80
Input Current		I_{IN}	—	—	−1	—	—	μA	(Note 1)
Current Consumption (1)		DI_{DD}	—	—	—	—	—	mA	DV_{DD}
Current Consumption (2)		AI_{DD}	—	—	—	—	—	mA	AV_{DD}

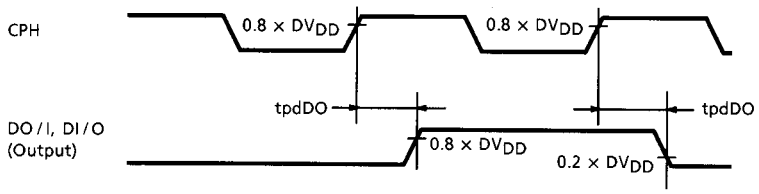
Note 1: All input pins except the analog signal input pins (VA, VB, VC)
Note 2: Analog signal input pins (VA, VB, VC)

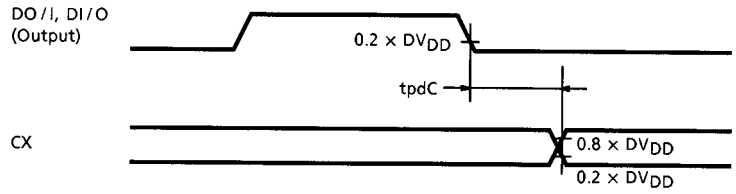
AC Characteristics

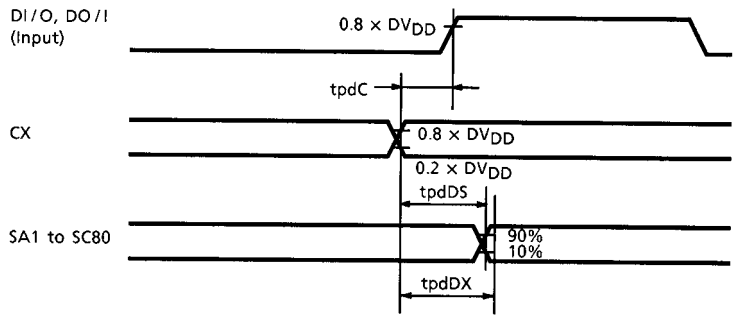
(DV_{DD} = 3.0 ± 0.3 V, AV_{DD} = 5.0 ± 0.5 V, AV_{SS} = DV_{SS} = 0 V, Ta = –20 to 75°C)

Parameter	Symbol	Test Circuit	Test Conditions	Min	Typ.	Max	Unit
Operating Frequency	fCPH (1 / tCPH)	—	MODE = low	0.5	—	30	MHz
			MODE = high	0.5	—	15	
CPH Pulse Width H	t_{CWH}	—	—	12	—	—	ns
CPH Pulse Width L	t_{CWL}	—	—	12	—	—	ns
Data Set-up Time	t_{DSU}	—	—	5	—	—	ns
Data Hold Time	t_{DHD}	—	—	5	—	—	ns
CX Set-up Time	tpdC	—	—	5	—	—	CPH period
Output Delay Time 1	tpdDO	—	C_L = 30 pF	—	—	16	ns
Output Delay Time 2	tpdDS	—	C_L = 50 pF Target output voltage (90%, 10%)	—	—	8	µs
Output Delay Time 3	tpdDX	—	C_L = 50 pF, Target output voltage	—	—	15	µs


tCPL
tCPH
CPH
0.8 × DVDD
0.2 × DVDD
0.2 × DVDD
tsDI
thDI
DI/O, DO/I
(Input)
0.8 × DVDD
0.2 × DVDD


CPH
0.8 × DVDD
0.8 × DVDD
tpdDO
tpdDO
DO/I, DI/O
(Output)
0.8 × DVDD
0.2 × DVDD


DO/I, DI/O
(Output)
0.2 × DVDD
tpdC
CX
0.8 × DVDD
0.2 × DVDD


DI/O, DO/I
(Input)
0.8 × DVDD
tpdC
CX
0.8 × DVDD
0.2 × DVDD
tpdDS
SA1 to SC80
90%
10%
tpdDX

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