MCU   **8-bit A/D Type MCU**

1. Features

- Compatible with MCS-51
- Embedded 8K Bytes OTP ROM
- 128 x 8-bit Internal RAM
- 15/19 Programmable I/O Lines for 20/24-pin Package
- Two 16-bit Timer/Counter & One 16-bit Timer
- Two External Interrupt Input (Only One Input for 20-pin Package)
- Two Channel PWM (Only One Channel PWM for 20-pin Package) Driving Capability up to 40 mA
- Embedded 1k bits EEPROM (for T81L0006B only)
- Programmable Serial UART Interface
- Low Power Idle & Power-down Modes
- Watch-dog Timer
- On-chip Crystal & RC Oscillator (Selected by Bonding Option)
- Internal Power-on Reset and External Reset Supported
- 8-Channel 8-bit A/D Converter
- SOP20/DIP20 & SOP24/DIP24 Package
- 3.3V Operating Voltage
- EEPORM Interface
- Low Voltage Reset

2. Applications

- Meter
- Household Appliances Controller
- Handwriting Board
- Charger
- Sport Devices
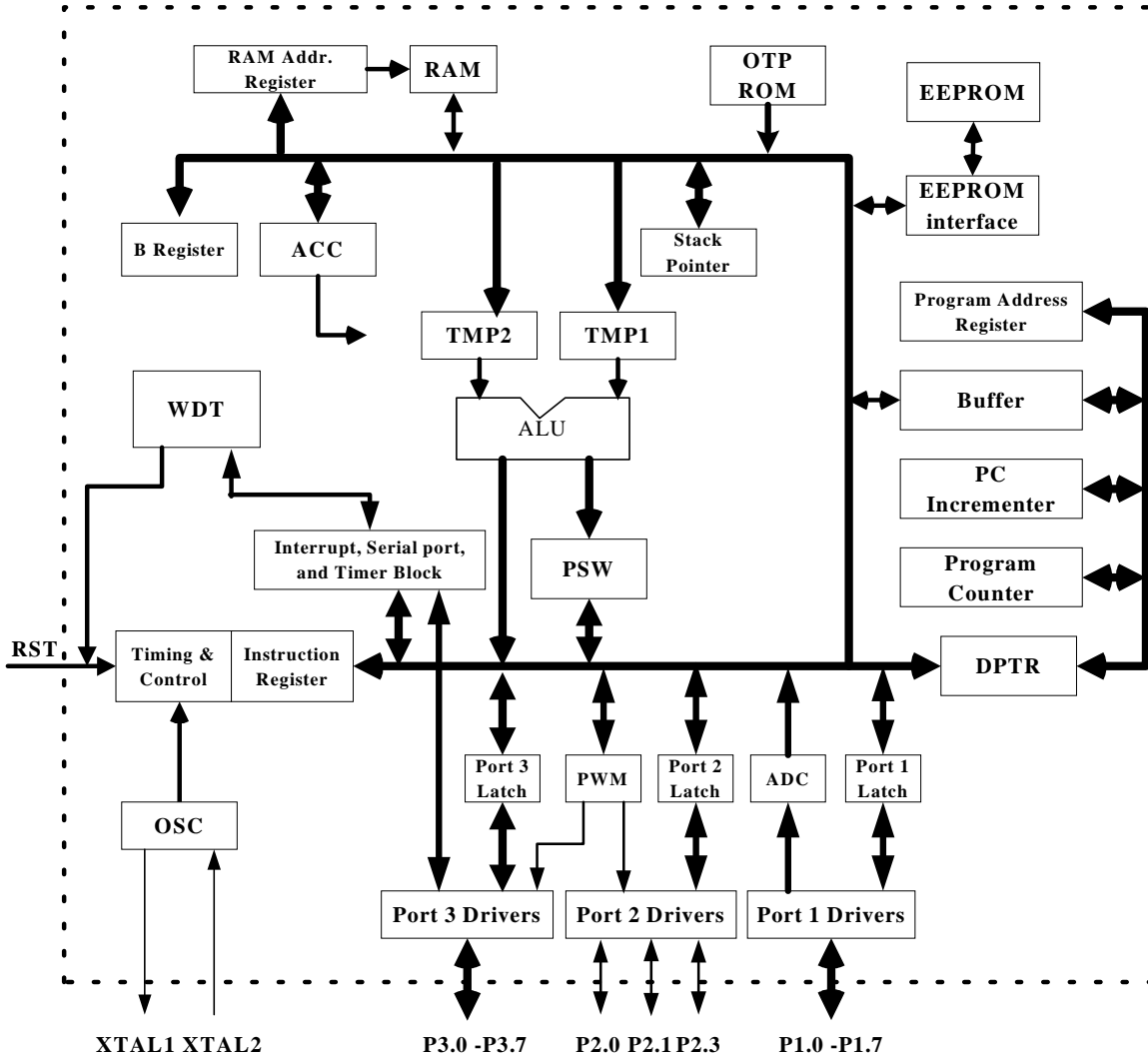- Other Controller (Automotive, Toy…)

3. General Description

The T81L0006A/B is 8-bit microcontroller designed and developed with low power and high speed CMOS technology. It contains a 8K bytes OTP ROM, a 128×8 RAM, an 8-channels 8-bit A/D converter, 15/19 I/O lines, a watchdog timer, two 16-bit counter/timers, a seven source, two-priority level nested interrupt structure, two channel pulsed-width modulator (PWM), a full duplex UART, and an on-chip oscillator and clock circuits.

In addition, the T81L0006A/B has two selectable modes of power reduction-idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.
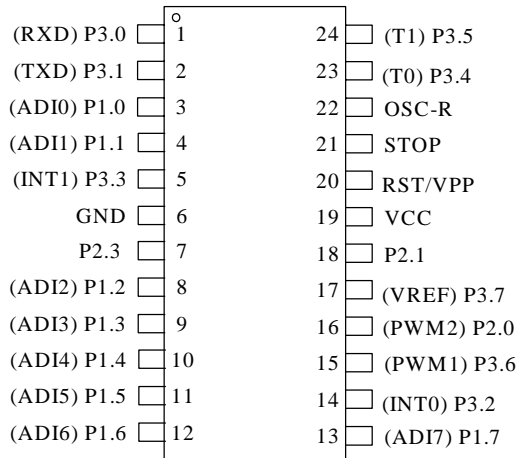
4. Order information

Part number	Oscillator type	EEPROM	Package
T81L0006A-AK	RC	NONE	24-pin DIP
T81L0006A-BK	Crystal	NONE	24-pin DIP
T81L0006A-CK	RC	NONE	20-pin DIP
T81L0006A-DK	Crystal	NONE	20-pin DIP
T81L0006A-AD	RC	NONE	24-pin SOP
T81L0006A-BD	Crystal	NONE	24-pin SOP
T81L0006A-CD	RC	NONE	20-pin SOP
T81L0006A-DD	Crystal	NONE	20-pin SOP
T81L0006B-AK	RC	Embedded	24-pin DIP
T81L0006B-BK	Crystal	Embedded	24-pin DIP
T81L0006B-AD	RC	Embedded	24-pin SOP
T81L0006B-BD	Crystal	Embedded	24-pin SOP

5. Block Diagram

6. Pin Configuration

```
            (RXD) P3.0  ▢ 1        24 ▢  (T1) P3.5
            (TXD) P3.1  ▢ 2        23 ▢  (T0) P3.4
           (ADI0) P1.0  ▢ 3        22 ▢  OSC-R
           (ADI1) P1.1  ▢ 4        21 ▢  STOP
           (INT1) P3.3  ▢ 5        20 ▢  RST/VPP
                  GND   ▢ 6        19 ▢  VCC
                  P2.3  ▢ 7        18 ▢  P2.1
           (ADI2) P1.2  ▢ 8        17 ▢  (VREF) P3.7
           (ADI3) P1.3  ▢ 9        16 ▢  (PWM2) P2.0
           (ADI4) P1.4  ▢ 10       15 ▢  (PWM1) P3.6
           (ADI5) P1.5  ▢ 11       14 ▢  (INT0) P3.2
           (ADI6) P1.6  ▢ 12       13 ▢  (ADI7) P1.7
```

DIP-24/SOP-24 For RC Oscillator
T81L0006A-AK/ T81L0006A-AD
T81L0006B-AK/ T81L0006B-AD

```
            (RXD) P3.0  ▢ 1        24 ▢  (T1) P3.5
            (TXD) P3.1  ▢ 2        23 ▢  (T0) P3.4
           (ADI0) P1.0  ▢ 3        22 ▢  XIN
           (ADI1) P1.1  ▢ 4        21 ▢  XOUT
           (INT1) P3.3  ▢ 5        20 ▢  RST/VPP
                  GND   ▢ 6        19 ▢  VCC
                  P2.3  ▢ 7        18 ▢  P2.1
           (ADI2) P1.2  ▢ 8        17 ▢  (VREF) P3.7
           (ADI3) P1.3  ▢ 9        16 ▢  (PWM2) P2.0
           (ADI4) P1.4  ▢ 10       15 ▢  (PWM1) P3.6
           (ADI5) P1.5  ▢ 11       14 ▢  (INT0) P3.2
           (ADI6) P1.6  ▢ 12       13 ▢  (ADI7) P1.7
```
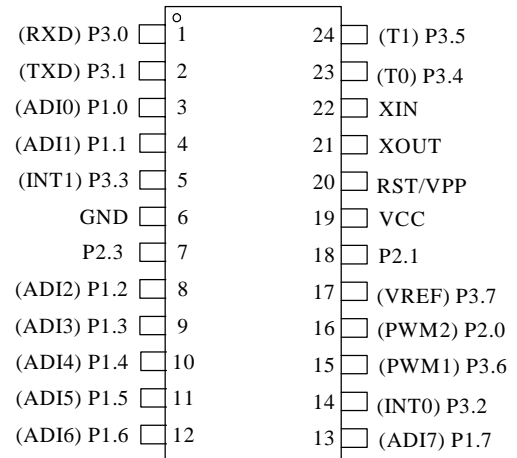
DIP-24/SOP-24 For Crystal Oscillator
T81L0006A-BK/ T81L0006A-BD
T81L0006B-BK/ T81L0006B-BD

```
            (RXD) P3.0  ▢ 1        20 ▢  (T1) P3.5
            (TXD) P3.1  ▢ 2        19 ▢  (T0) P3.4
           (ADI0) P1.0  ▢ 3        18 ▢  OSC-R
           (ADI1) P1.1  ▢ 4        17 ▢  STOP
                  GND   ▢ 5        16 ▢  RST/VPP
           (ADI2) P1.2  ▢ 6        15 ▢  VCC
           (ADI3) P1.3  ▢ 7        14 ▢  (VREF) P3.7
           (ADI4) P1.4  ▢ 8        13 ▢  (PWM1) P3.6
           (ADI5) P1.5  ▢ 9        12 ▢  (INT0) P3.2
           (ADI6) P1.6  ▢ 10       11 ▢  (ADI7) P1.7
```
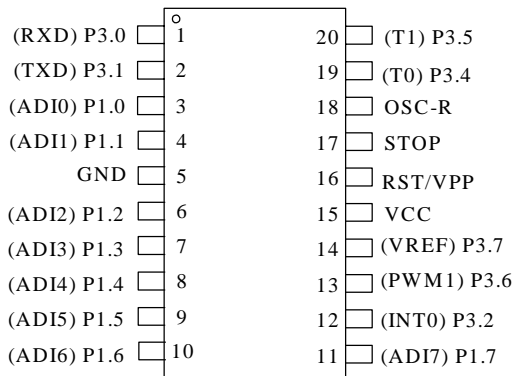
DIP-20/SOP-20 For RC Oscillator
T81L0006A-CK/ T81L0006A-CD

```
            (RXD) P3.0  ▢ 1        20 ▢  (T1) P3.5
            (TXD) P3.1  ▢ 2        19 ▢  (T0) P3.4
           (ADI0) P1.0  ▢ 3        18 ▢  XIN
           (ADI1) P1.1  ▢ 4        17 ▢  XOUT
                  GND   ▢ 5        16 ▢  RST/VPP
           (ADI2) P1.2  ▢ 6        15 ▢  VCC
           (ADI3) P1.3  ▢ 7        14 ▢  (VREF) P3.7
           (ADI4) P1.4  ▢ 8        13 ▢  (PWM1) P3.6
           (ADI5) P1.5  ▢ 9        12 ▢  (INT0) P3.2
           (ADI6) P1.6  ▢ 10       11 ▢  (ADI7) P1.7
```
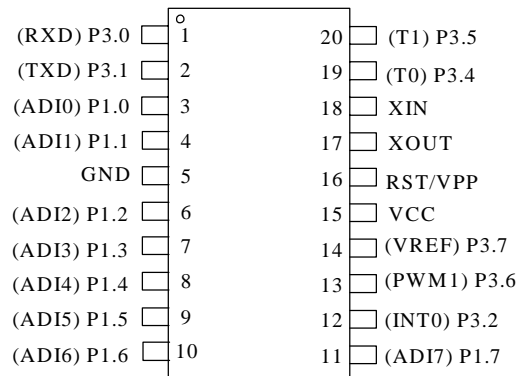
DIP-20/SOP-20 For Crystal Oscillator
T81L0006A-DK/ T81L0006A-DD

7. Pin Description

Number (24-Pin)	Number (20-Pin)	Name	Type	Description
1	1	P3.0/(RXD)	I/O	General-purpose I/O pin (Default) or Serial input port.
2	2	P3.1/(TXD)	I/O	General-purpose I/O pin (Default) or Serial output port.
3	3	P1.0/(ADI0)	I/O	General-purpose I/O pin (Default) or ADC input channel 0.
4	4	P1.1/(ADI1)	I/O	General-purpose I/O pin (Default) or ADC input channel 1.
5	-	P3.3/(INT1)	I/O	General-purpose I/O pin (Default) or External interrupt source 1.
6	5	GND		Ground
7	-	P2.3	I/O	General-purpose I/O pin.
8	6	P1.2/(ADI2)	I/O	General-purpose I/O pin (Default) or ADC input channel 2.
9	7	P1.3/(ADI3)	I/O	General-purpose I/O pin (Default) or ADC input channel 3.
10	8	P1.4/(ADI4)	I/O	General-purpose I/O pin (Default) or ADC input channel 4.
11	9	P1.5/(ADI5)	I/O	General-purpose I/O pin (Default) or ADC input channel 5.
12	10	P1.6/(ADI6)	I/O	General-purpose I/O pin (Default) or ADC input channel 6.
13	11	P1.7/(ADI7)	I/O	General-purpose I/O pin (Default) or ADC input channel 7.
14	12	P3.2/(INT0)	I/O	General-purpose I/O pin (Default) or External interrupt source 0.
15	13	P3.6/(PWM1)	I/O	General-purpose I/O pin (Default) or PWM signal output channel 1.
16	-	P2.0/(PWM2)	I/O	General-purpose I/O pin (Default) or PWM signal output channel 2.
17	14	P3.7/(VREF)	I/O	General-purpose I/O pin (Default) or External reference voltage input pin for ADC.
18	-	P2.1	I/O	General-purpose I/O pin.
19	15	VCC		3.3V power supply.
20	16	RST/VPP	I	Reset signal input or programming supply voltage input.
21	17	XOUT/(STOP)	O	Crystal oscillator output terminal or stop RC oscillator network.
22	18	XIN/(OSC-R)	I	Crystal oscillator input terminal or RC oscillator external resister connect pin.
23	19	P3.4/(T0)	I/O	General-purpose I/O pin (Default) or Timer 0 external input pin.
24	20	P3.5/(T1)	I/O	General-purpose I/O pin (Default) or Timer 1 external input pin.

8. Temperature Limit Ratings

Parameter	Rating	Units
Operating temperature Range	-40 to +85	°C
Storage Temperature Range	-55 to +125	°C

9. Electrical Characteristics

D.C Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V$_{CC}$	Operating Voltage	25°C		3.0	3.3	3.6	V
I$_{CC}$	Operating Current	No load, ADC disable Vcc=3.3V		-	6	-	mA
I$_{PD}$	Power-Down Current	No load, Vcc=3.3V				1	uA
I$_{ADC}$	Only ADC Enable, Others Disable	No load		-	120	-	uA
V$_{ADC}$	ADC Input Voltage Range			0	-	V$_{REF}$	V
V$_{REF}$	V$_{REF}$ input voltage range			2	-	V$_{CC}$	V
V$_{IH}$	Hi-Level input voltage	V$_{out}$ >=V$_{VOH(MIN.)}$ V$_{out}$ <=V$_{VOL(MIN.)}$		2.1	-	-	V
V$_{IL}$	Low-Level input voltage	V$_{out}$ >=V$_{VOH(MIN.)}$ V$_{out}$ <=V$_{VOL(MIN.)}$		-	-	0.6	V
V$_{OH}$	Hi-Level Output voltage	V$_{CC}$=MIN. V$_I$=V$_{IH}$ or V$_{IL}$	I$_{OH}$=-7uA	2.9	-	-	V
			I$_{OH}$=-45uA	2.4			
			I$_{OH}$=-70uA	1.9			
			I$_{OH}$=-12mA**	2.4			
			I$_{OH}$=-20mA**	1.9			
V$_{OL}$1 *	Low-Level Output voltage	V$_{CC}$=MIN. V$_I$=V$_{IH}$ or V$_{IL}$	I$_{OL}$=12mA	-	-	0.2	V
			I$_{OL}$=25mA			0.4	
			I$_{OL}$=40mA			0.6	
V$_{OL}$2 **	Low-Level Output voltage	V$_{CC}$=MIN. V$_I$=V$_{IH}$ or V$_{IL}$	I$_{OL}$=4mA			0.2	V
			I$_{OL}$=12mA			0.4	
			I$_{OL}$=20mA			0.6	

Note :   *   for PWM pins (P3.6/PWM1 and P2.0/PWM2).
   **   for high driving current mode.

A.C Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F$_{SYS1}$	System Clock 1 (Crystal OSC)	V$_{CC}$=3.3V	-	12	24	MHz
F$_{SYS2}$	System Clock 2 (RC OSC)	V$_{CC}$=3.3V	-	12	-	MHz
F$_{ADC}$	ADC Clock Frequency		-	125	-	KHz
t$_{ACT}$	ADC Conversion Time		-	128		us
t$_{RES}$	External Reset High Pulse Width		-	10	-	system cycle
t$_{POS}$	Power ON Start up Time		-	20	-	ms
t$_{LHLL}$	ALE pulse width		127	-	-	ns
t$_{AVLL}$	Address Valid to ALE Low		43	-	-	ns
t$_{LLAX}$	Address Hold after ALE Low		48	-	-	ns
t$_{LLIV}$	ALE Low to Valid Instruction In		-	-	233	ns
t$_{LLPL}$	ALE Low to PSEN Low		43	-	-	ns
t$_{PLPH}$	PSEN pulse width		205	-	-	ns
t$_{PLIV}$	PSEN Low to Valid Instruction In		-	-	145	ns
t$_{AVIV}$	Address to Valid Instruction In		-	-	312	ns
t$_{RLRH}$	RD pulse width		400	-	-	ns
t$_{WLWH}$	WR pulse width		400	-		ns
t$_{RLDV}$	RD Low to Valid data in		-	-	252	ns
t$_{LLDV}$	ALE Low to Valid data in		-	-	517	ns
t$_{AVDV}$	Address to Valid data in		-	-	585	ns
t$_{LLWL}$	ALE Low to RD or WR Low		200	-	300	ns
t$_{AVWL}$	Address to RD or WR Low		203	-	-	ns
t$_{WHLH}$	RD or WR High to ALE High		43	-	123	ns

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                                                                              Revsion : B

10. Function Description

10.1 Reset
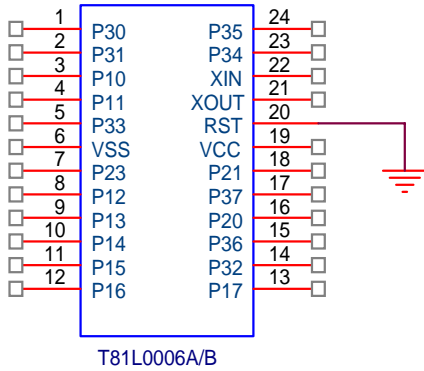
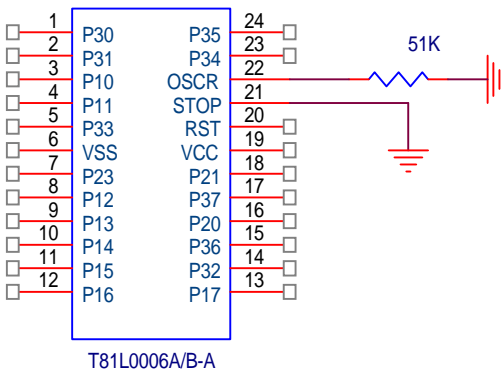For Power on Reset only
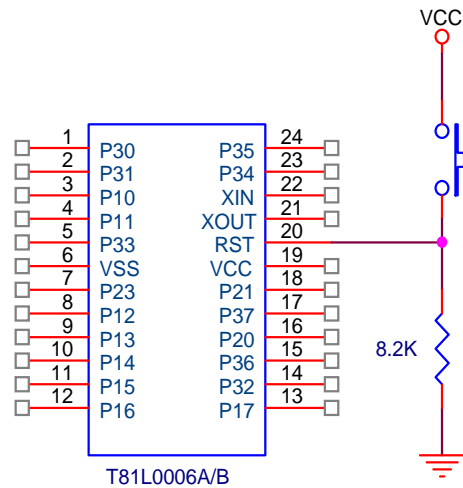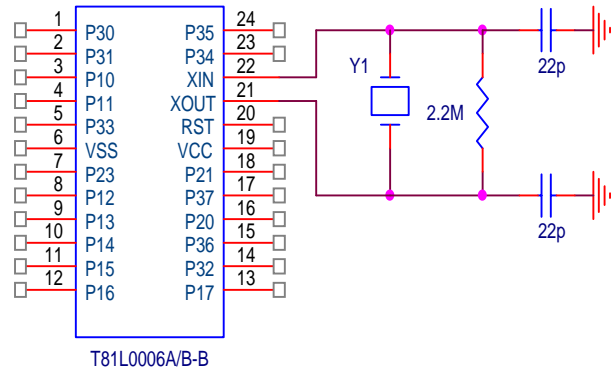

For Power on Reset and External Reset

10.2 Oscillation

RC Oscillator

Crystal Oscillator

10.3 Special Function Register

F8H									
F0H	B								
E8H									
E0H	ACC								
D8H									
D0H	PSW								
C8H	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2			
C0H									
B8H	IP								
B0H	P3								
A8H	IE								
A0H	P2								
98H	SCON	SBUF							
90H	P1								
88H	TCON	TMOD	TL0	TL1	TH0	TH1			
80H	P0*	SP	DPL	DPH				WDREL	PCON

*Note: P0:Internal still keeping, but for pad dominate, no external pin assignment

Accumulator : ACC

ACC is the Accumulator register. The mnemonics for Accumulator-Specific instructions, however, refer to the Accumulator simply as A.

B Register : B

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Program Status Word : PSW

The PSW register contains program status information as detailed in

CY	AC	F0	RS1	RS0	OV	--	P

BIT SYMBOL FUNCTION

PSW.7   CY   Carry flag.

PSW.6   AC   Auxiliary Carry flag. (For BCD operations.)

PSW.5   F0   Flag 0. (Available to the user for general purposes.)

PSW.4   RS1   Register bank select control bit 1.

     Set/cleared by software to determine working register bank. (See **Note.**)

PSW.3   RS0   Register bank select control bit 0.

     Set/cleared by software to determine working register bank. (See **Note.**)

PSW.2   OV   Overflow flag.

PSW.1   —   User-definable flag.

PSW.0   P   Parity flag.

     Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the Accumulator, i.e., even parity.

NOTE: The contents of (RS1, RS0) enable the working register banks as follows:

   (0,0)— Bank 0 (00H–07H)

   (0,1)— Bank 1 (08H–0fH)

   (1,0)— Bank 2 (10H–17H)

   (1,1)— Bank 3 (18H–17H)

Stack Pointer : SP

The Stack Pointer register is 8 bits wide. It is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the Stack Pointer is initialized to 07H after a reset. This causes the stack to begin at locations 08H.

Data Pointer (DPTR) : DPH & DPL

The Data Pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

Ports 1.0~1.7 & 2.0,2.1,2.3 & 3.0~3.7

All Ports are the SFR latches, respectively. Writing a one to a bit of a port SFR (P1 or P2 or P3) causes the corresponding port output pin to switch high. Writing a zero causes the port output pin to switch low. When used as an input, the external state of a port pin will be held in the port SFR (i.e., if the external state of a pin is low, the corresponding port SFR bit will contain a '0'; if it is high, the bit will contain a '1').

Serial Data Buffer : SBUF

The Serial Buffer is actually two separate registers, a transmit buffer and a receive buffer. When data is moved to SBUF, it goes to the transmit buffer and is held for serial transmission. (Moving a byte to SBUF is what initiates the transmission.) When data is moved from SBUF, it comes from the receive buffer.

Timer Registers : TH0, TL0, TH1, TL1,TH2,TL2

Register pairs (TH0, TL0) and (TH1, TL1) and (TH2, TL2) are 16-bit Counting registers for Timer/Counters 0 and Timer1and Timer2, respectively.
.

Control Register : IP, IE, TMOD, TCON, SCON, PCON

Special Function Registers IP, IE, TMOD, TCON, SCON, and PCON contain control and status bits for the interrupt system, the Timer/Counters, and the serial port. They are described in later sections.

Standard Serial Interface

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost.) The serial port receive and transmit registers are both accessed at Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0: Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 the oscillator frequency.

Mode 1: 10 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.

Mode 2: 11 bits are transmitted (through TxD) or received (through RxD): start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On Transmit, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable. In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = '0' and REN = '1'. Reception is initiated in the other modes by the incoming start bit if REN = '1'.

Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = '1'. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows: When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is '1' in an address byte and '0' in a data byte. With SM2 = '1', no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, in Mode 1 can be used to check the validity of the stop bit. In   Mode 1 reception, if SM2 = '1', the receive interrupt will not active unless a valid stop bit is received.

Serial Port Control Register

The serial port control and status register is the Special Function Register SCON, shown in Figure 11. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Baud Rates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = Oscillator Frequency / 12. The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If SMOD = '0' (which is the value on reset), the baud rate is 1/64 the oscillator frequency. If SMOD = '1', the baud rate is 1/32 the oscillator frequency.

Mode 2 Baud Rate $=2^{SMOD}/64*$ (Oscillator Frequency)

In the T81L0006A/B, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate.

SCON

MSB							LSB
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Where SM0, SM1 specify the serial port mode, as follows:

SM0	SM1	Mode	Description	Baud Rate
0	0	0	shift register	f_{osc} / 12
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	UART F_{OSC} /64 or F_{OSC} /32
1	1	3	9-bit UART	Variable

Using Timer 1 to Generate Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

Mode 1, 3 Baud Rate $=2^{SMOD}/32*$ (Timer 1 Overflow Rate)

The Timer 1 interrupt should be disabled in this application. The Timer 1 itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In the most typical applications, it is configured for "timer" operation, in the auto-reload mode (high nibble of TMOD = 0010B). In that case the baud rate is given by the formula:

Mode 1, 3 Baud Rate $=2^{SMOD}*$(Oscillator Frequency)/ 32/12 / [256 _ (TH1)]

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload.

Using Timer 2 to Generate Baud Rates

Timer2 is selected as the baudrate generator by setting TCLK and/or RCLK in T2CON register as followed.

T2CON (address : C8h)

MSB							LSB
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

T2CON.7: TF2 Timer2 overflow flag set by timer2 overflow and must be cleared by software. TF2 will not be set when either RCLK=1 or TCLK=1.

T2CON.6: EXF2 Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2=1. when timer2 interrupt is enabled, EXF2=1 will cause the CPU to vector to the timer2 interrupt routine. EXF2 must be cleared by software.

T2CON.5: RCLK Receive clock flag. When set, cause the serial port to use timer2 overflow pulses for its receive clock in

mode 1 and 3. RCLK=0 causes timer1 overflow to be used for the receive clock
T2CON.4: TCLK Transmit clock flag. When set, cause the serial port to use timer2 overflow pulses for its transmit clock in mode 1 and 3. TCLK=0 causes timer1 overflow to be used for the transmit clock

T2CON.3: EXEN2 Timer2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if timer2 is not being used to clock the serial port. EXEN2=0 causes timer2 to ignore events at T2EX.
T2CON.2: Start/stop control for timer2. A logic 1 starts the timer
T2CON.1: Timer or counter select. (Timer 2) , 0 as internal timer
T2CON.0: Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2=1. When cleared, auto reloads will occur either with timer2 overflow or negative transitions at T2EX when EXEN2=1. When either RCLK=1 or TCLK=1, this bit is ignored and the timer is forced to auto-reload on timer2 overflow.
Note then the baudrates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer2 into its baudrate generator mode.
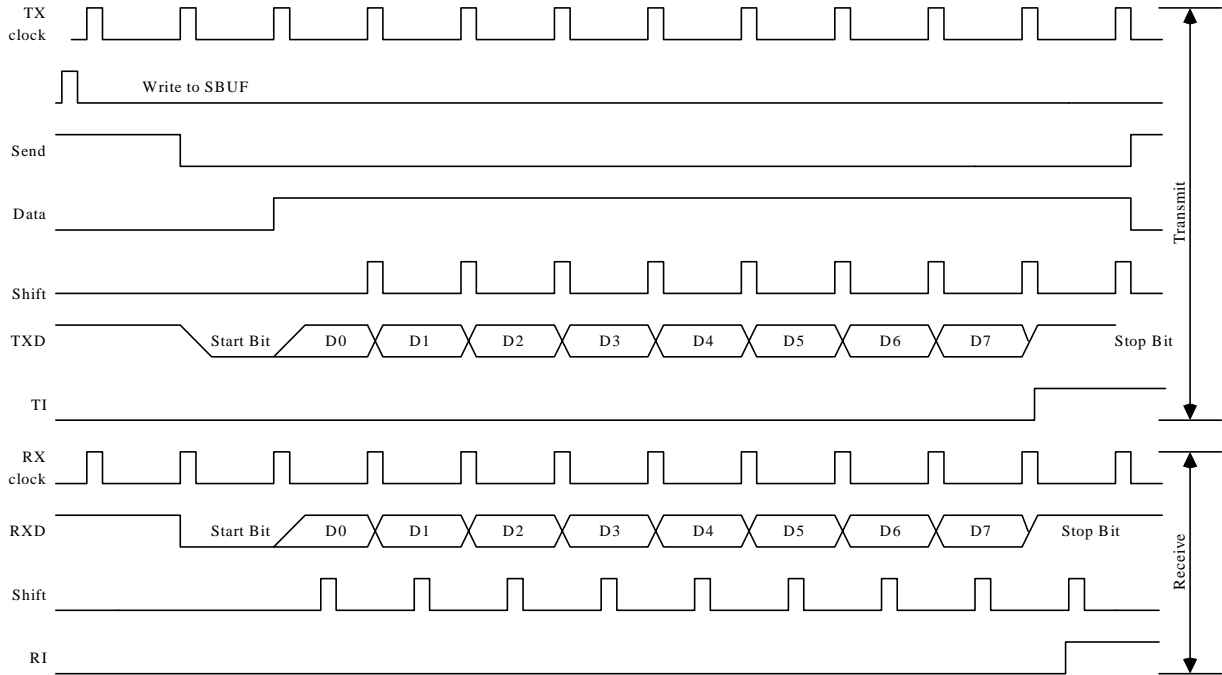The baudrate generator mode is similar to the auto reload mode, in that a rollover is TH2 causes the Timer2 registers to be reload with the 16 bit value in registers RCAP2H and RCAP2L, which are preset by software given by the formula.

Baudrate= (Timer2 overflow rate)/16 =(Oscillator Frequency) / (32*(65536-(RCAP2H,RCAP2L)))

Serial Interface Timing Diagram
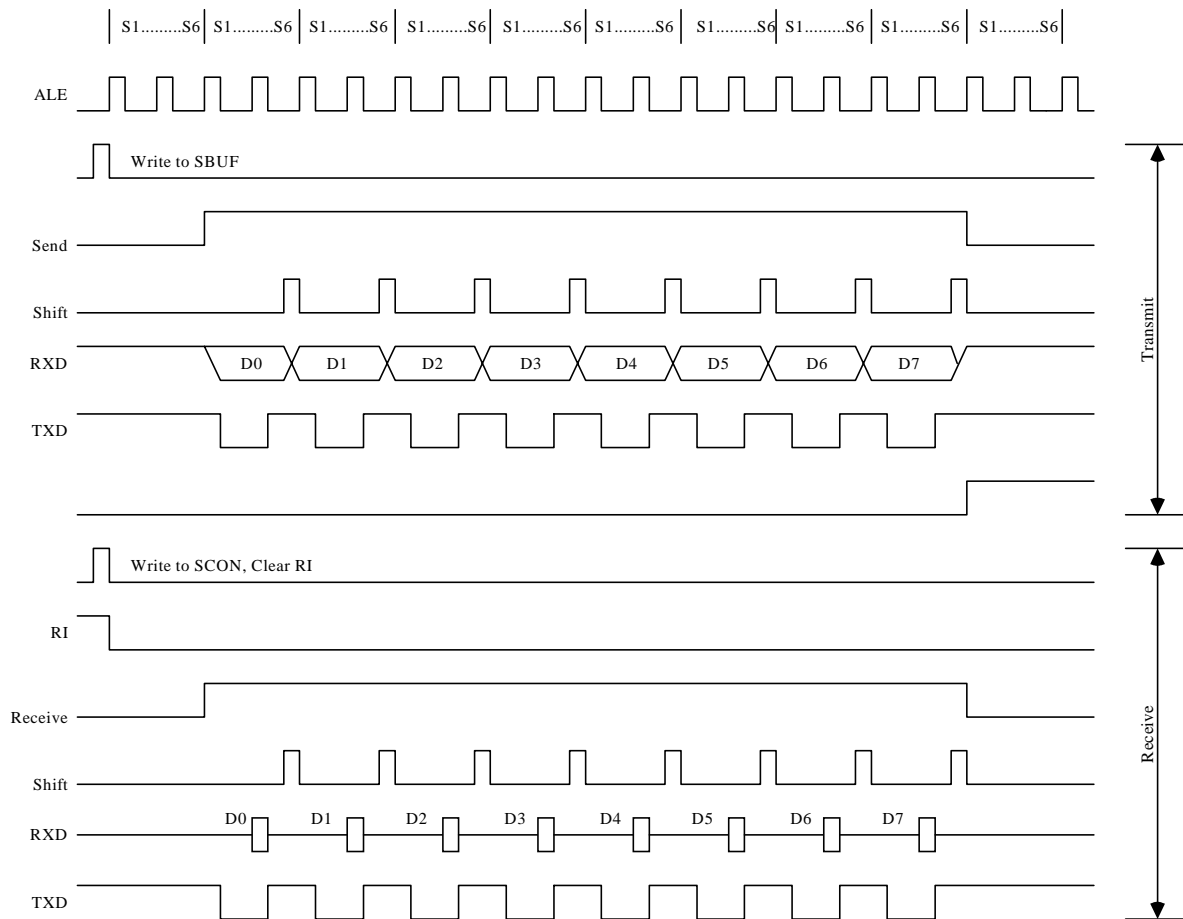
Serial Port Mode 0

Serial Port Mode 1
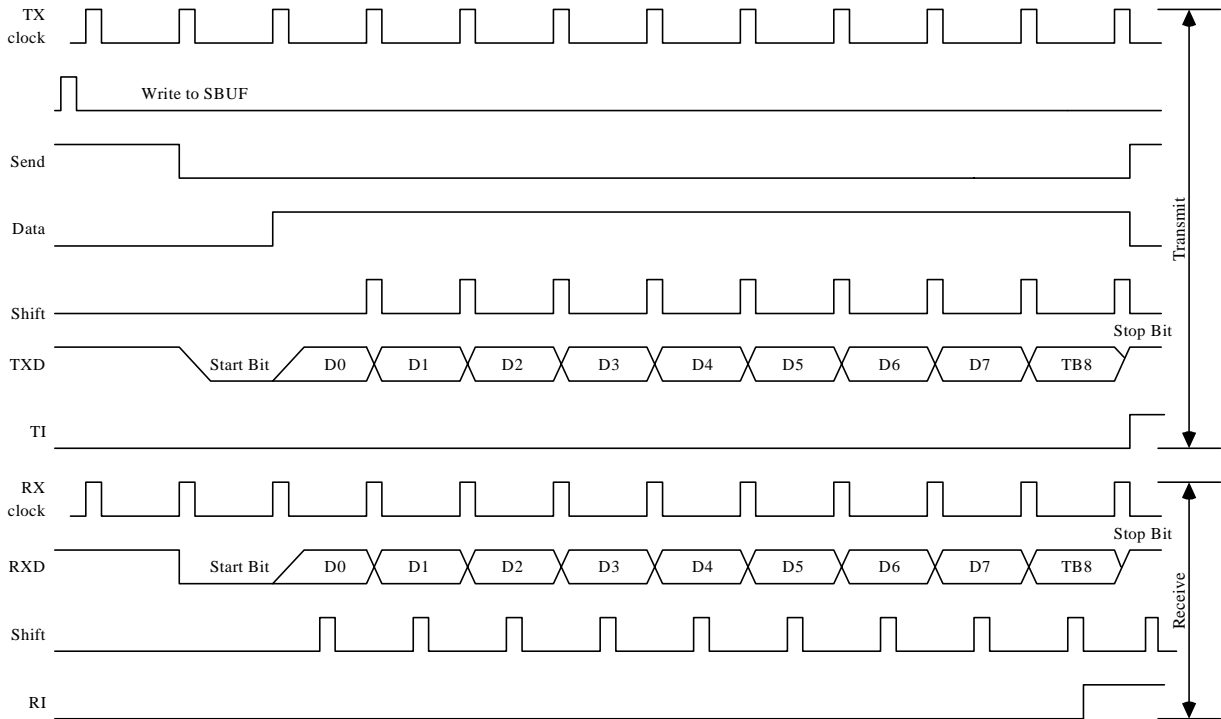
Serial Port Mode 2
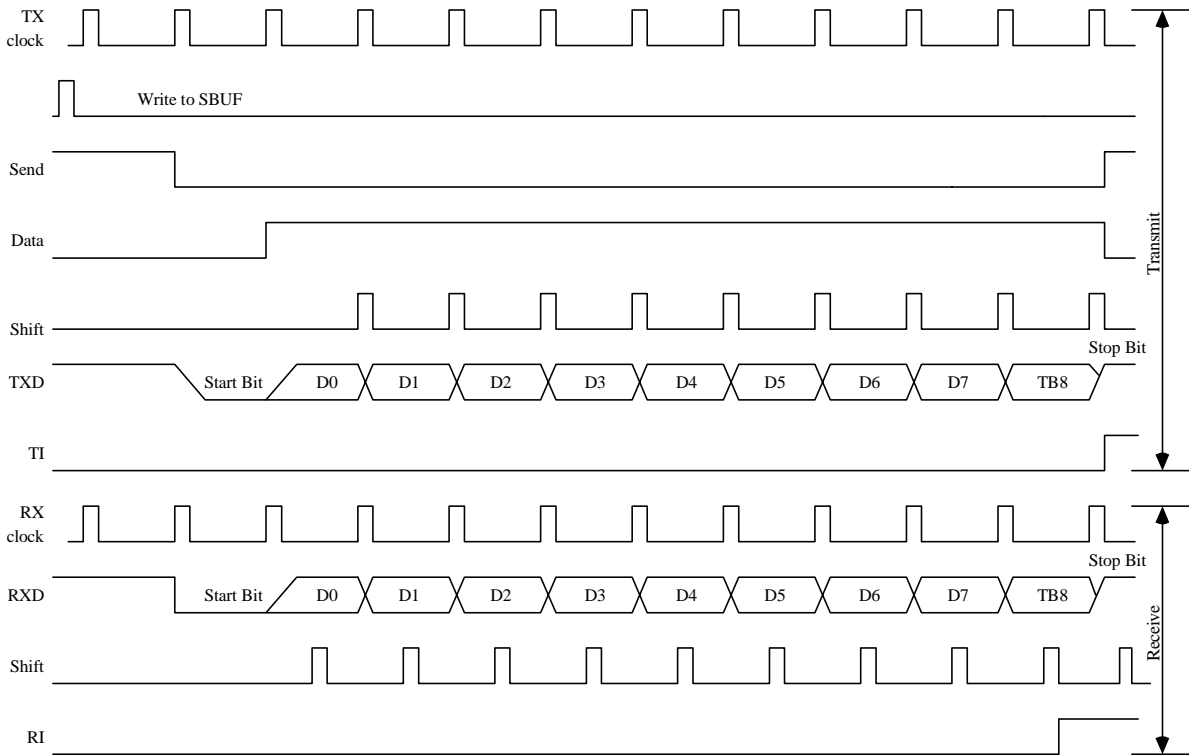
Serial Port Mode 3

Interrupt Enable Register : IE

MSB							LSB
EA	wdt	ET2	ES	ET1	EX1	ET0	EX0

EA   IE.7   Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.

wdt IE.6   Watchdog timer refresh flag.

ET2 IE.5   Enable or disable the Timer 2 overflow interrupt.

ES   IE.4   Enable or disable the serial port interrupt.

ET1 IE.3   Enable or disable the Timer 1 overflow interrupt.

EX1 IE.2   Enable or disable External Interrupt 1. (See **NOTE**)

ET0 IE.1   Enable or disable the Timer 0 overflow interrupt.

EX0 IE.0   Enable or disable External Interrupt 0.

NOTE: if A/D converter interrupts enabled, EX1 interrupt function will be replaced.

Watchdog Timer

The watchdog timer is a 16-bit counter that is incremented once every 24 or 384 clock cycles. After an external reset the watchdog timer is disabled and all registers are set to zeros.

● **Watchdog Timer structure**

The watchdog consists of 16-bit counter **wdt**, reload register **wdtrel**, prescalers by 2 and by 16 and control logic. Where wdtl=00h while start up.
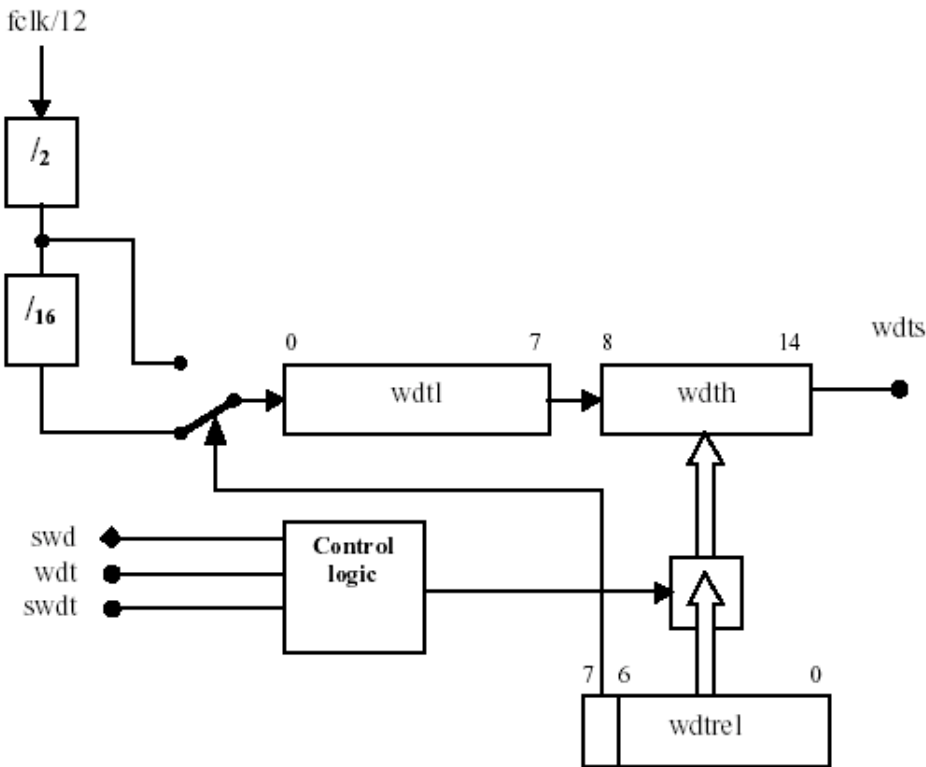

Figure   Watchdog block diagram

● **Start procedure**

There are one way to start the watchdog. A programmer can start the watchdog as refreshing procedure. Once the watchdog is started it cannot be stopped unless rst signal becomes active. When **wdt** registers enters the state 7FFCh, asynchronous **wdts** signal will become active. The signal **wdts** sets the bit 6 in ip0 register and requests reset state. The **wdts** is cleared either by rst signal or change of the state of the **wdt** timer.

Procedure: load wdtrel value → set "wdt" → set "swdt" in 12 instruction cycles.

● **Refreshing the watchdog timer**

The watchdog timer must be refreshed regularly to prevent reset request signal from becoming active. This requirement imposes obligation on the programmer to issue two followed instructions. The first instruction sets **wdt** and the second one **swdt**. The maximum allowed delay between settings of the **wdt** and **swdt** is 12 instruction cycles. While this period has expired and **swdt** has not been set, **wdt** is automatically reset, otherwise the watchdog timer is reloaded with the content of the **wdtrel** register and **wdt** is automatically reset. The procedure is as "Start procedure" before.

● **Special Function Registers**
a) Interrupt Enable 0 register (ien0)
The ien0 register (address : A8)

MSB							LSB
eal	wdt	et2	es0	et1	ex1	et0	ex0

The ien0 bit functions

Bit	Symbol	Function
ien0.6	wdt	Watchdog timer refresh flag. Set to initiate a refresh of the watchdog timer. Must be set directly before swdt is set to prevent an unintentional refresh of the watchdog timer. The wdt is reset by hardware 12 instruction cycles after it has been set.

Note: other bits are not used to watchdog control

b) Interrupt Enable 1 register (ien1)
The ien1 register (Address : B8)

MSB							LSB
-	swdt	pt2	ps	pt1	px1	pt0	px0

The ien1 bit functions

Bit	Symbol	Function
Ien1.6	swdt	Watchdog timer start refresh flag. Set to active/refresh the watchdog timer. When directly set after setting wdt, a watchdog timer refresh is performed. Bit swdt is reset by hardware 12 instruction cycles after it has been set.

Pay attention that when write ien1.6, it write the swdt bit, when read ien1.6, we will read out the wdts bit. Ie. Watch dog timer status flag. Set by hardware when the watchdog timer was started.

d) Watchdog Timer Reload register (wdtrel)
The wdtrel register (Address : 86)

MSB							LSB
7	6	5	4	3	2	1	0

The wdtrel bit functions

Bit	Symbol	Function
wdtrel.7	7	Prescaler select bit. When set, the watchdog is clocked through an additional divide-by-16 prescaler
wdtrel.6 t0 wdtrel.0	6-0	Seven bit reload value for the high-byte of the watchdog timer. This value is loaded to the wdt when a refresh is triggered by a consecutive setting of bits wdt and swdt

The wdtrel register can be loaded and read any time

● **WDT Reset**

A high on reset pin or watchdog reset request for two clock cycles while the oscillator is running resets the device.

Diagram
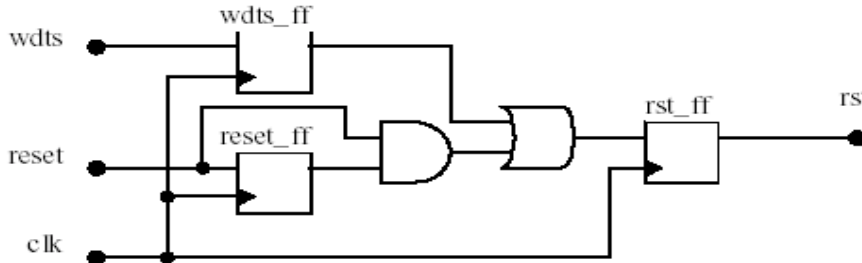
b) Watchdog timer reset
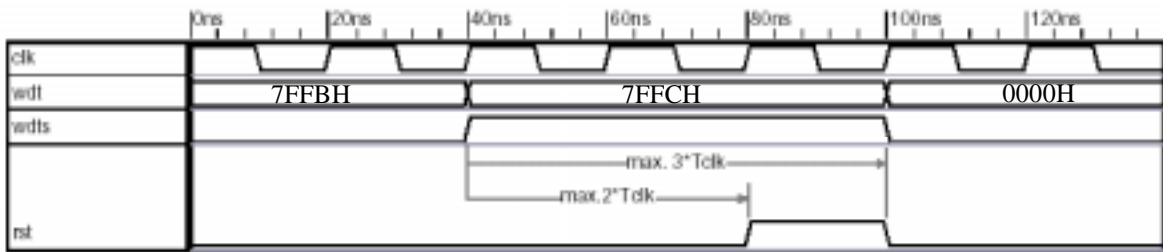
Figure Watchdog reset timing

**Note :
clk: external clock input
Tclk: clock period
wdt: watchdog timer registers
wdts: watchdog timer status flag
reset: external reset input
rst: internally generated reset signal

● *Reset Time Formula*

Reset time=(7FFCh-wdth.wdtl)*presc*48/ClockFrequency
while presc=16 if wdtrel.7=1, presc=1 if wdtrel.7=0.

For example if you use frequency clock=12MHz, wdtrel=10111111b which means wdtrel.7=1 and wdth=3Fh
Then reset time= (7FFCh-3F00h)*48/12M=66544 us

10.4 External Register Table (for A/D Converter , PWM, EEPROM & LVR)

Register Address		Name	Comments
(A15…A5-A0)	Hex		
100… 0010 0000	8020H	ADM	A/D Control & Status
100… 0010 0001	8021H	ADR	A/D Clock prescaler and A/D value LSB
100… 0010 0010	8022H	ADB	A/D value MSB
100… 0010 1010	802aH	ADE	A/D Converter Channel Enable
100… 0010 0101	8025H	PWMC1	PWM Control register1
100… 0010 1011	802bH	PWMC2	PWM Control register2 and LVR(Low Voltage Reset)*
100… 0010 0110	8026H	PWM1	PWM1 Value
100… 0010 0111	8027H	PWM2	PWM2 Value
100… 00101000	8028H	SPICON	EEPROM control & setup (for T81L0006B only)
100… 0010 1001	8029H	OPCODE	EEPROM opcode (for T81L0006B only)
100… 0010 1110	802eH	DATAW_H	EEPROM write high byte (for T81L0006B only)
100… 0010 1111	802fH	DATAW_L	EEPROM write low byte (for T81L0006B only)
100… 0010 1100	802cH	DATAR_H	EEPROM read high byte (for T81L0006B only)
100… 0010 1101	802dH	DATAW_L	EEPROM read high byte (for T81L0006B only)
100… 0011 0000	8030H	Port3 HDS	Port3 I/O high driving set**
100… 0011 0001	8031H	Port2 HDS	Port2 I/O high driving set**
100… 0011 0010	8032H	Port1 HDS	Port1 I/O high driving set**

Note :

* LVR (Low Voltage Reset) address : 802bH, read/write

MSB							LSB
Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
LVR[7]	LVR[6]	PWM Control register2					

LVR[7] : if LVR[7] write '1', low voltage reset function enable.
default is '0', low voltage reset function disable.

LVR[6] : if LVR[6] write '1'= 2.1V reset. if LVR[6] write '0'= 2.8V reset.
default is '0'= 2.8V reset.

** Port I/O high driving set
if write '0' = set I/O to high driving current mode.
if write '1' = set I/O to normal driving current mode.
default is set '1'.

Port 3 high driving address : 8030H

MSB							LSB
Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Port3.7	Port3.6	Port3.5	Port3.4	Port3.3	Port3.2	Port3.1	Port3.0

Port 2 high driving address : 8031H

MSB							LSB
Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
				Port2.3		Port2.1	Port2.0

Port 1 high driving address : 8032H

MSB							LSB
Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Port1.7	Port1.6	Port1.5	Port1.4	Port1.3	Port1.2	Port1.1	Port1.0

10.5 A/D converter

The data acquisition component is an 8-bit analog-to-digital converter, 8-channel multiplexer and microcontroller compatible control logic. The 8-bit A/D converter uses successive approximation conversion technique. The 8-channel multiplexer can directly access any of 8-single-ended analog signals. The device eliminates the need for external zero and full-scale adjustments. The design of the component has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The component offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suitable from process and machine control to consumer applications.

A/D Converter Register Control

	Default	R/W	R/W	R	R/W	-	R/W	R/W	R/W
ADM	00100000	ADENB	ADS	EOC	ADI	-	CHS2	CHS1	CHS0
ADR	Default	-	R/W	R/W	R/W	-	-	-	-
	x010xxxx	-	ADPS2	ADPS1	ADPS0	-	-	-	-
ADB	Default	R	R	R	R	R	R	R	R
	xxxxxxxx	ADB7	ADB6	ADB5	ADB4	ADB3	ADB2	ADB1	ADB0
ADE	Default	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	00000000	ENCH7	ENCH6	ENCH5	ENCH4	ENCH3	ENCH2	ENCH1	ENCH0

ADENB   Disable all A/D converter input channels: 0-Disable, 1-Enable
             If ADENB=0, all input channel will be closed. If ADENB =1, each input
         channels is individually enabled or disabled by setting or clearing ENCH7~ENCH0
         enable bits.
ADI   A/D Interrupt bit: 0-Disable, 1-Enable
             If ADI=1, external interrupt 1 will be inhibited. A/D converter interrupt function will
         in place of external interrupt 1 function.
ADS   A/D Start bit: 0-Stop, 1-Start
EOC   A/D Status bit: 0- Busy, 1-End of converting and clear ADS bit
CHS2: CHS0 --- Channel select

ADPS2: ADPS0 ---A/D clock divider, Input frequency = Fosc/3

ADPS2:1:0	Dividers Ratio Fad: Fosc/12
000	1:1
001	1:2
010	1:4
011	1:8
100	1:16
101	1:32
110	1:64
111	1:128

ADB7 ~ADB0--- 8-bit ADC converting data
ENCH7 ~ENCH0 --- ADC individual input channel enable bit:
                    0-Disable, 1-Enable

A/D converter conversion flow

```
┌─────────────────────────┐
│      Set ADENB=1         │
└─────────────────────────┘
             │
             ▼
┌─────────────────────────┐
│  Set ENCH7~ENCH0         │
│  (Enable individually    │
│   channel)               │
└─────────────────────────┘
             │
             ▼
┌─────────────────────────┐
│  Set CHS[2:0] register bit│
│  (Chose ADC input channel)│
└─────────────────────────┘
             │
             ▼
┌─────────────────────────┐
│  ADC starts conversion   │
└─────────────────────────┘
             │
             ▼
┌─────────────────────────┐
│ When set (ADS register )bit=1,│
│ and then (EOC register) bit will│
│ be turn low.             │
└─────────────────────────┘
             │
             ▼
┌─────────────────────────┐
│ Microcontroller generate ADS signal│
│ pulse to ADC.            │
│ 1'ADCLK<ADS pulse<16'ADCLk│
└─────────────────────────┘
```

```
┌─────────────────────────┐
│ EOC signal from high go low.│
│ (ADC operating)          │
└─────────────────────────┘
             │
             ▼
┌─────────────────────────┐
│ Microcontroller detect EOC signal.│
│ rising edge.             │
│ (ADC conversion complete)│
└─────────────────────────┘
             │
             ▼
┌─────────────────────────┐
│ Microcontroller read ADC │
│ conversion data from D[7:0]│
└─────────────────────────┘
             │
             ▼
┌─────────────────────────┐
│ (EOC register) bit turn '1'.│
│ (ADS register) bit turn '0'.│
└─────────────────────────┘
             │
             ▼
┌─────────────────────────┐
│          END             │
└─────────────────────────┘
```

A/D Converter Timing Diagram

RB

ADCLK   0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

ADS   10 ADCLK < TIME < 16 ADCLK

CHS[2:0]

AN[7:0]

EOC   16 ADCLK

PCHA   5 ADCLK

D[7:0]

1.5 ADCLK
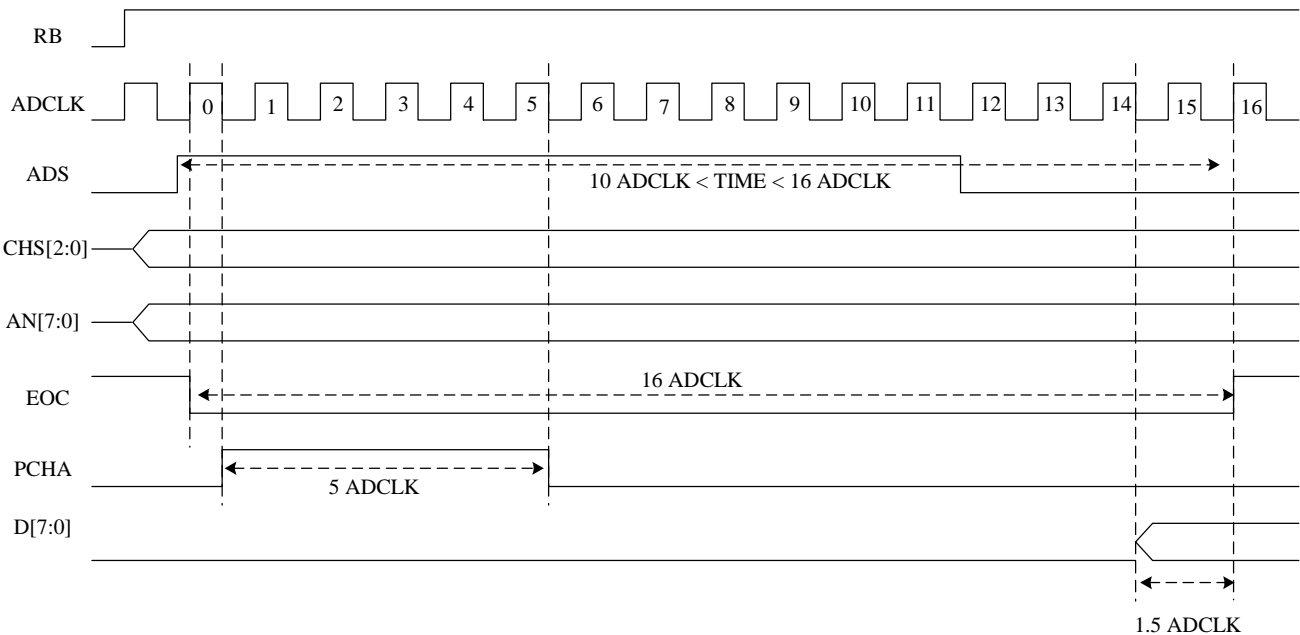
10.6 Pulsed Width Modulator (PWM)

The T81L0006A/B provides 2 channels 8 bits PWM output for peripheral. The frequency source of the PWM counter comes from Fosc. Writing 1 to PWMC register enable bit will enable the PWM output function. PWMPS2:1:0 control bit determine PWM output clock that range from Fosc/2 to Fosc/256. Each PWM output clock duty cycle can be programmed though set PWM0 or PWM1 register.

PWM Register Control

	Default	B7: R/W	B6: R/W	B5: R/W	B4: R/W	B3: R/W	B2: R/W	B1: R/W	B0: R/W
PWMC1	0x00	Pwm2EN	Pwm2PS2	Pwm2PS1	Pwm2PS0	Pwm1EN	Pwm1PS2	Pwm1PS1	Pwm1PS0
PWMC2	Default								R/W
	0x00	-	-	-	-	-	-	-	Mode
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PWM1	0x00								
PWM2	0x00								

PWMC1: PWM control register1
    Pwm1EN, Pwm2EN
           PWM1, PWM2 Enable bit: 0-Disable, 1-Enable
             When Enable bit=0, PWM output pin = High impedance.

    PWMPS2:1:0 --- PWM dividers ratio
       Fpwm= Fosc/PWMPS/256 while select 8-bit mode
       Fpwm= Fosc/PWMPS/65536 while select 16-bit mode

PS:2:1:0	Dividers ratio Fpwm:Fosc
000	1:2
001	1:4
010	1:8
011	1:16
100	1:32
101	1:64
110	1:128
111	1:256

   PWMC2: PWM control register2 Mode
      PWM 16-bit mode or 8-bit mode selects : '0'= 8-bit mode, '1'= 16-bit mode
      When select 16-bit mode, PWM2 register= PWM duty cycle value high byte.
      PWM1 register= PWM duty cycle value low byte.
      Note: 16-bit PWM just for PWM1 output

PWM1 register:
    Set PWM1's duty cycle. --- Duty1= PWM1/256 or 16-bit PWM duty cycle value low byte.

PWM2 register:
    Set PWM2's duty cycle. --- Duty2= PWM2/256 or 16-bit PWM duty cycle value high byte.
    Set 16-bit PWM duty cycle. --- Duty= (PWM2, PWM1)/65536

10.7 EEPROM Interface (for T81L0006B only)

The EEPROM interface timing is fully compatible with 93C46. To access or send data from/to T81L0006B , 6 registers are going to be controlled.

EEPROM Register Control

SPICON	Default	--	--	--	--	--	B2: R/W	B1: R/W	B0: R/W
	00H	--	--	--	--	--	Epdiv1	Epdiv0	Epst
OPCODE									W
	00H	-	-	-	-	-	-	-	
DATAW_H									
DATAW_L	00H								
DATAR_H									
DATAW_L	00H								

SPICON:

MSB   LSB

Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
					Epdiv1	Epdiv0	Epst

Epst: start EEPROM timing. "1" to start and will be auto cleared after timing finish.
Epdiv[1..0]: divide input clock into EEPROM system clock.
   10: divide by 64
   01: divide by 32
   else: divide by 16

OPCODE

MSB   LSB

Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
OP Code		address					

Instruction Set	OP Code	Address	Input Data
Read	10	A5-A0	
WEN (Write Enable)	00	11xxxx	
Write	01	A5-A0	D15-D0
WRALL (Write All Registers)	00	01xxxx	D15-D0
WDS (Write Disable)	00	00xxxx	
Erase	11	A5-A0	
ERAL	00	10xxxx	

11. I/O Ports

Port1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. Port 1 output buffers can sink/source four external TTL device inputs. When port 1 pins are written as 1's, these pins are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current because of the internal pull-ups.

Port 1 also serves the analog signal input of A/D converter, as listed below:

P1.0 ADI0 (analog input signal channel 0)
P1.1 ADI1 (analog input signal channel 1)
P1.2 ADI2 (analog input signal channel 2)
P1.3 ADI3 (analog input signal channel 3)
P1.4 ADI4 (analog input signal channel 4)
P1.5 ADI5 (analog input signal channel 5)
P1.6 ADI6 (analog input signal channel 6)
P1.7 ADI7 (analog input signal channel 7)

Port2.0, 2.1, 2.3

Port2.0, 2.1, 2.3 are a bi-directional I/O port with internal pull-ups. Port2.0, 2.1, 2.3 output buffers can sink/source four external TTL device inputs. When Port2.0, 2.1, 2.3 pins are written as 1's, these pins are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port2.0, 2.1, 2.3 pins that are externally being pulled low will source current because of the internal pull-ups.

Port 2.0 also serves the output signal of PWM 2.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. Port 3 output buffers can sink/source four external TTL device inputs. When port 3 pins are written as 1's, these pins are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current because of the internal pull-ups.

Port 3 also serves the functions of various special features, as listed below:

P3.0 RXD (serial input port)
P3.1 TXD (serial output port)
P3.2 INT0 (external interrupt 0)
P3.3 INT1 (external interrupt 1)
P3.4 T0 (timer 0 external input)
P3.5 T1 (timer 1 external input)
P3.6 PWM1 (PWM 1 signal output)
P3.7 VREF (external reference voltage input for ADC)