

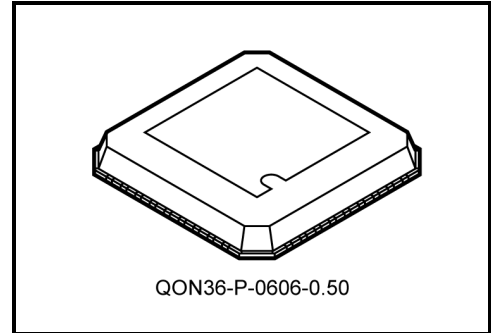
TENTATIVE TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB32301AFL

2.4-GHz Radio Communication IC

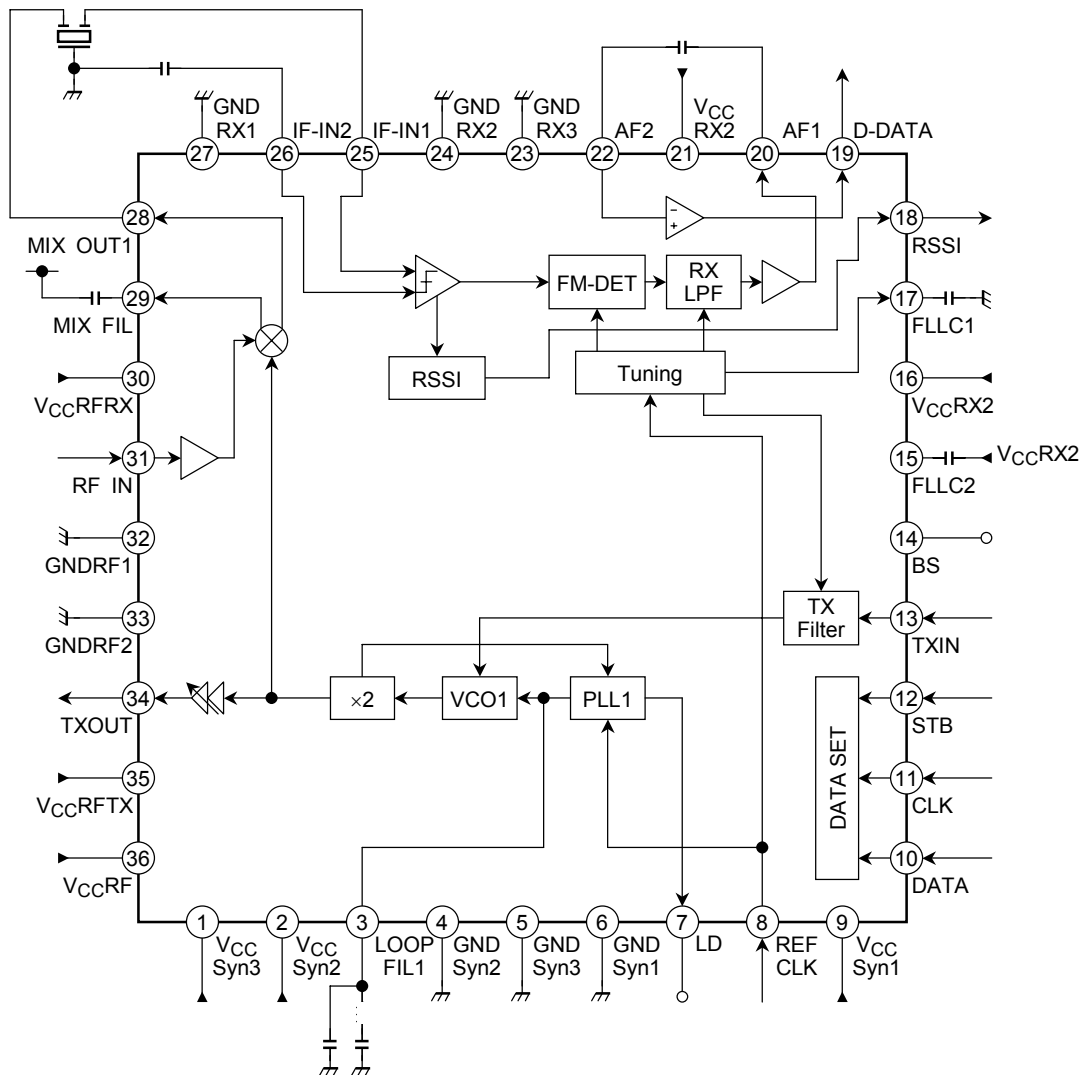
Features

- Consumption current : 35 mA (typ.) (at reception)
: 26 mA (typ.) (at transmission)
- Operating power supply voltage
: 2.7 V to 3.3 V (operating temperature range: -20°C to 70°C)
- Ultra-compact package: 36-pin QON
- On-chip LNA
- On-chip VCO
- On-chip PA



Weight: 0.08 g (typ.)
Marking: TB32301AFL

Block Diagram



This product is sensitive to electrostatic discharge. When handling the product, ensure that the environment is protected against electrostatic discharge.

Pin Functions (typical resistor and capacitor values)

| Pin No. | Pin Name | Function | Equivalent Circuit |
|---------|----------------------|---|--------------------|
| 1 | V _{CC} Syn3 | Power supply pin | — |
| 2 | V _{CC} Syn2 | Power supply pin | — |
| 3 | LOOPFIL1 | External pin for loop filter | |
| 4 | GNDSyn2 | Ground pin | — |
| 5 | GNDSyn3 | Ground pin | — |
| 6 | GNDSyn1 | Ground pin | — |
| 7 | LD | PLL lock detector output pin | |
| 8 | REFCLK | Reference clock input pin for PLL, TX filter and IF auto tuning | |
| 9 | V _{CC} Syn1 | Power supply pin | — |
| 10 | DATA | Serial data input pin | |
| 11 | CLK | Serial clock input pin | |
| 12 | STB | Serial strobe input pin | |
| 13 | TXIN | Transmit signal input pin | |

| Pin No. | Pin Name | Function | Equivalent Circuit |
|---------|---------------------|--|--------------------|
| 14 | BS | Battery-saving pin | |
| 15, 17 | FLLC2 FLLC1 | Auto-tuning pin. External capacitor determines the time constant of auto-tuning circuit. | |
| 16 | V _{CC} RX2 | Power supply pin | — |
| 18 | RSSI | This pin drives out DC voltage according to the RF input signal level. | |
| 19 | DDATA | Comparator output pin | |
| 20 | AF1 | Demodulation signal output pin | |

| Pin No. | Pin Name | Function | Equivalent Circuit |
|---------|--------------------|------------------------|--------------------|
| 21 | V _{CCRX1} | Power supply pin | — |
| 22 | AF2 | Comparator input pin | |
| 23 | GNDRX2 | Ground pin | — |
| 24 | GNDRX1 | | |
| 25 | IFIN1 | IF amplifier input pin | |
| 26 | IFIN2 | | |
| 27 | GNDRF3 | Ground pin | — |
| 28 | MIXOUT1 | Mixer output pin | |
| 29 | MIXFIL | Mixer filter pin | |
| 30 | V _{CCRF1} | Power supply pin | — |
| 31 | RFIN | RF signal input pin | |

| Pin No. | Pin Name | Function | Equivalent Circuit |
|---------|---------------------|----------------------|--------------------|
| 32 | GNDRF1 | Ground pin | — |
| 33 | GNDRF2 | | |
| 34 | TXOUT | RF signal output pin | — |
| 35 | V _{CC} RF2 | Power supply pin | — |
| 36 | V _{CC} RF3 | Power supply pin | — |

Note: The equivalent circuit diagrams above are intended as an aid for designing external circuits. They do not show the exact layout of the internal circuits.

Power Supply

| Power Supply Name | Pin No. | Ground Relevant Pin Name | Pin No. | Block Name |
|-----------------------|---------|-------------------------------|----------------|---|
| V _{CC} Syn3 | 1 | GND Syn3 | 5 | VCO Doubler |
| V _{CC} Syn2 | 2 | GND Syn2 | 2 | VCO1 |
| V _{CC} Syn1 | 9 | GND Syn1 | 6 | PLL, DATA SET |
| V _{CC} RX2 | 16 | GND RX3 | 23 | Tuning (FLL), RX-AMP, RX-LPF, DATA COMP, FM-DET |
| V _{CC} RX1 | 21 | GND RX2 | 24 | TX-FILTER, PA, RSSI, IF-AMP, (IF-BPF) |
| V _{CC} RFRX | 30 | GND RF1 GND RF2 | 32 33 | LNA |
| V _{CC} RX TX | 35 | GND RX1 GND RF1 GND RF2 | 27 32 33 | PA |
| V _{CC} RF | 36 | GND RX1 GND RF1 GND RF2 | 27 32 33 | PA, MIXER, LNA |

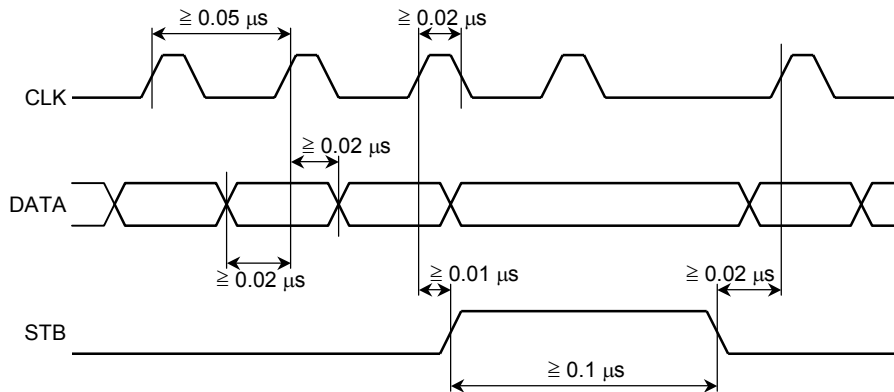
Supplementary: Pins as shown below are shorted together.

- (1) V_{CC} RX TX (35 pin) – V_{CC} Syn2 (2 pin)
- (2) V_{CC} RF (36 pin) – V_{CC} RFRX (30 pin)

Functions and Operation

1. Serial data input timing chart

- Data to control the TB32301AFL is serially applied to pins CLK, DATA and STB.
- Data is loaded into shift registers with MSB first on the rising edge of the clock and latched on the rising edge of the STB signal. When the STB pin is high, the data stored in the shift register is retained even if clock is applied. When the STB pin is low, the data can be rewritten.
- Input timings of the CLK, DATA and STB are shown below.



2. Serial data control contents

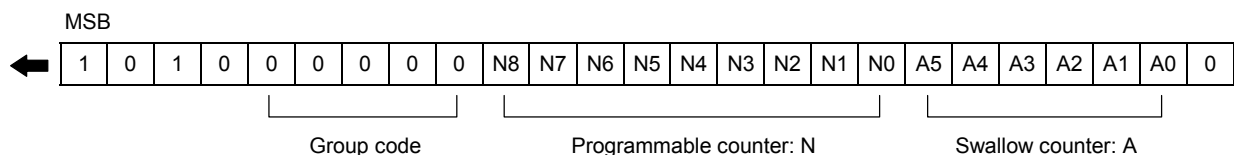
The TB32301F has five types of control contents. These types are determined by serial input 5-bit register address (group code). The control contents consist of PLL main counter setting, PLL reference counter setting, auto-tuning reference counter setting, transmit power amplifier gain setting and system control setting. These settings are controlled independently one another.

2.1 Register address setting table (group code)

| GC4 | GC3 | GC2 | GC1 | GC0 | Control Contents |
|-----|-----|-----|-----|-----|---------------------------------------|
| 0 | 0 | 0 | 0 | 0 | PLL main counter setting |
| 0 | 0 | 0 | 0 | 1 | PLL reference counter setting |
| 0 | 0 | 0 | 1 | 0 | Auto-tuning reference counter setting |
| 0 | 0 | 0 | 1 | 1 | Transmit power amplifier gain setting |
| 0 | 0 | 1 | 0 | 0 | System control register setting |

2.2 PLL main counter setting

- The PLL main counter employs a swallow counter.
- It consists of 6-bit swallow counter, 9-bit programmable counter and 1/64, 1/65 2-modulus prescaler.
- The divide factor can be set in the range 4032 to 32767 by sending any data to the swallow counter and the programmable counter.



$$A = A_0 + A_1 \times 2^1 + A_2 \times 2^2 + \dots + A_5 \times 2^5$$

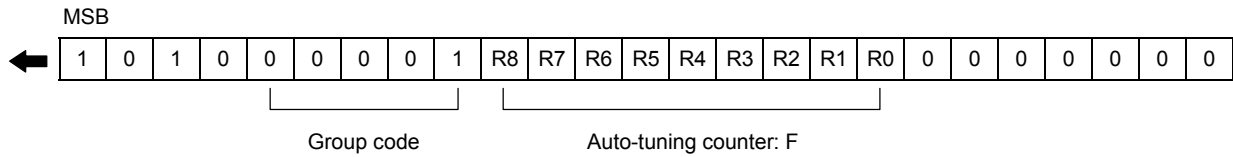
$$N = N_0 + N_1 \times 2^1 + N_2 \times 2^2 + \dots + N_8 \times 2^8$$

$$(\text{Divide factor}) = 64N + A$$

$$4032 \leq (\text{Divide factor}) \leq 32767$$

2.3 PLL reference counter setting

- The PLL reference counter generates phase comparison frequency0.
- It consists of 9-bit reference counter. The divide factor can be set in the range 4 to 511 by sending any data to the reference counter.



$$R = R0 + R1 \times 2^1 + R2 \times 2^2 + \dots + R8 \times 2^8$$

(Divide factor) = R

$$4 \leq (\text{Divide factor}) \leq 511$$

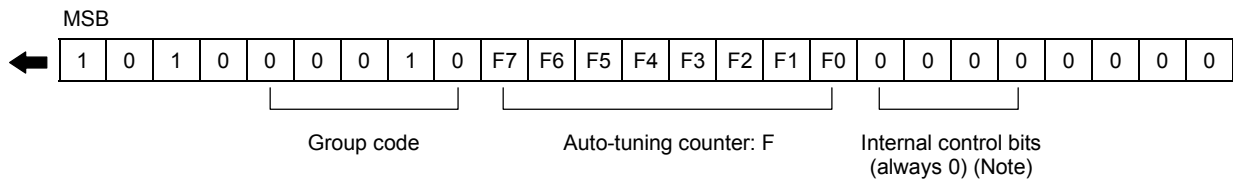
2.4 Auto-tuning reference counter setting

- The TB32301AFL has an automatic tuning system to correct the fluctuation of center frequency in FM detector, which is caused by, for example, temperature change. To generate a reference clock to correct the fluctuation, set the divide factor of auto-tuning reference counter to the value to obtain 200-kHz frequency, according to external reference clock frequency.
- The auto-tuning reference counter consists of 8 bits.
- The divide factor can be set in the range 6 to 255 by sending any data to the reference counter.

$$F = F0 + F1 \times 2^1 + F2 \times 2^2 + \dots + F7 \times 2^7$$

(Divide factor) = F

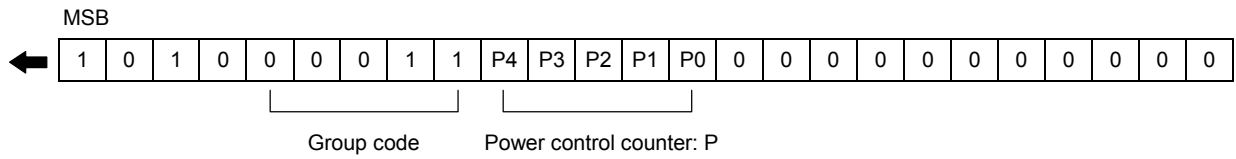
$$6 \leq (\text{Divide factor}) \leq 255$$



Note Internal control bits are used to control the PLL. Please clear the bits. Otherwise, the PLL may not operate properly.

2.5 Transmit power amplifier setting

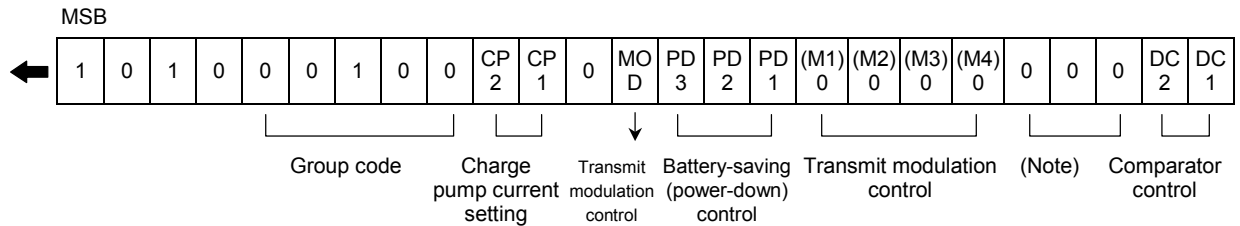
Applying data serially to pins CLK, DATA and STB changes the gain of the transmit power amplifier. The power control counter consists of 5 bits.



$$(\text{Control step number}) = P0 + P1 \times 2^1 + P2 \times 2^2 + \dots + P4 \times 2^4$$

2.6 System control register setting

In the system control register, applying data serially to pins CLK, DATA and STB sets the optional functions as described below.



Note: Please clear the bits.

- PLL charge pump current setting (CP1 and CP2 bits: 2.4 GHz)
The TB32301AFL contains a constant current charge pump circuit.
The output current of the circuit can be selected by setting the CP1 and CP2 bits.

| CP2 | CP1 | Charge Pump Current |
|-----|-----|---------------------|
| 0 | 0 | 4 mA |
| 0 | 1 | 2 mA |
| 1 | 0 | 1 mA |

- Transmit data timing setting (MOD bit)
Clearing the MOD bit makes the VCO circuit oscillate at the center frequency, which is controlled by the PLL. The circuit is not controlled by received data.

| MOD | Transmit Data Timing |
|-----|----------------------|
| 0 | Modulator OFF |
| 1 | Modulator ON |

- Battery-saving (power-down) mode setting (PD1, PD2 and PD3 bits)
Setting the PD1, PD2 and PD3 bits controls the circuits in the reception and transmission blocks. The settings of the external BS control pin (14 pin) and the control bits are shown in the table below.

| BS | Control Bits | | | Reception Block | | | | | Transmission Block | | Common Block | |
|----|--------------|-----|-----|-----------------|-----|--------|--------|--------|--------------------|--------|--------------|-------------|
| | PD3 | PD2 | PD1 | LNA | MIX | IF-AMP | FM-DET | RX-LPF | PA | TX-LPF | PLL, VCO | Auto tuning |
| L | * | * | * | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| H | 1 | 1 | 1 | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF |
| H | 1 | 0 | 0 | OFF | OFF | OFF | OFF | OFF | OFF | OFF | ON | ON |
| H | 1 | 0 | 1 | OFF | OFF | OFF | OFF | OFF | ON | ON | ON | ON |
| H | 0 | 0 | 1 | OFF | OFF | OFF | OFF | OFF | OFF | ON | ON | ON |
| H | 0 | 0 | 0 | ON | ON | ON | ON | ON | OFF | OFF | ON | ON |
| H | 0 | 1 | 1 | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | ON |

- Transmit modulation control bits (M1 to M4 bits)
M1 to M4 bits are cleared for normal operation, however, M2 to M4 bits can be set to high to control the transmit modulation as shown below.

| M1 | M2 | M3 | M4 | Transmit Modulation |
|----|----|----|----|--------------------------|
| 0 | 0 | 0 | 0 | Normal modulation |
| 0 | 1 | 1 | 1 | Normal modulation × 16/8 |

- Rise time constant setting of comparator reference level (D1 and D2 bits)
The rise time constant of data comparator reference level is determined by an external capacitance and an internal resistance. The internal resistance can be selected by applying data serially to pins CLK, DATA and STB.

(Rise time constant) = (External capacitance: C) × (Internal resistance: R)

| DC2 | DC1 | Internal Resistance: R |
|-----|-----|------------------------|
| 0 | 0 | 10 kΩ |
| 0 | 1 | 10 kΩ |
| 1 | 0 | 100 kΩ |
| 1 | 1 | 1000 kΩ |

3. Image canceller mixer in reception block

The TB32301AFL contains an image canceller mixer as the first stage of the reception block. The image canceller mixer is designed for upper local, therefore, please set the local signal frequency to f_0 (desired reception frequency) + 11 MHz (IF frequency).

4. Lock detector function (LD pin: 7 pin)

The TB32301AFL incorporates VCO lock detector function.

When a phase error is detected in the phase comparator, 0 is driven out from the LD pin. When the VCO is locked or all the circuits are OFF, 1 is driven out from the pin.

5. VCO modulation polarity and demodulation data polarity

- VCO modulation polarity

| Transmit Data | VCO Frequency Deviation |
|---------------|-------------------------|
| 1 | Positive (+) polarity |
| 0 | Negative (-) polarity |

- Demodulation data polarity

The polarity of the data, which is demodulated by the FM detector and the data comparator, is the same as that of transmit data.

| At Transmission | At Reception | |
|-----------------|-----------------------|------------------------|
| | FM Detector | Data Comparator Output |
| 1 | Positive (+) polarity | 1 |
| 0 | Negative (-) polarity | 0 |

Electrical Characteristics

Maximum Ratings

| Characteristics | Symbol | Rating | Unit |
|---------------------------|------------------------------|------------|------|
| Power supply voltage | VCC_A, VCC_D | 3.6 | V |
| Power dissipation | PD | 530 | mW |
| Input pin voltage | CLK, DATA, STB, BS, LD, TXIN | 3.6 | V |
| Storage temperature range | Tstg | -50 to 150 | °C |

Note 1: Maximum ratings are a set of specified parameter values which must not be exceeded during operation, even for an instant.

Operating Ratings

| Characteristics | Symbol | Test Circuit | Test Condition | Rating | Unit |
|-----------------------|--------|--------------|-----------------------------|------------|------|
| Operating voltage | Vopr1 | — | Ta = 25°C, ground reference | 2.7 to 3.3 | V |
| Operating temperature | Topr1 | — | | -20 to 70 | °C |

Note 2: These ratings specify the ranges within which the device can operate its basic functions, even when fluctuations in its electrical characteristics occur.

Electrical Characteristics

(Unless otherwise specified, Ta = 25°C, VCC = 3.0 V, f = 2450 MHz, Bit Rate = 100kHz, PA bit setting = 21, Dev = ± 160 kHz)

Power Supply

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|------------------------------------|--------|--------------|---|---------------------|------|---------------------|------|
| Current consumption 1 at no signal | ICC1 | 1 | At reception BS = H, PD1 = 0, PD2 = 0, PD3 = 0 (Note 3) | 28.0 | 35.1 | 42.0 | mA |
| Current consumption 2 at no signal | ICC2 | 1 | At transmission BS = H, PD1 = 1, PD2 = 0, PD3 = 1 (Note 3) | 19 | 25.6 | 42 | mA |
| Supply current at no signal | ICCQ1 | 1 | In battery-saving mode BS = L, PD1 = 1, PD2 = 1 PD3 = 1 (Note 3) | — | 0 | 10 | μA |
| High-level input voltage | VIH | — | CLK, DATA, STB, BS, TXIN | $V_{CC} \times 0.8$ | VCC | $V_{CC} + 0.2$ | V |
| Low-level input voltage | VIL | — | CLK, DATA, STB, BS, TXIN | -0.2 | 0 | $V_{CC} \times 0.2$ | V |

Note 3: Please refer to Section 2.6 “System control register setting”.

Integrated Characteristics

| Characteristics | Symbol | Test Circuit | Test Condition | Min | Typ. | Max | Unit |
|---------------------------|----------|--------------|--------------------|-----|------|-----|-------|
| Minimum input level | VIN(min) | 1 | S/N = 20dB | - | 20.4 | - | dBμV |
| Demodulation output level | Vod | — | Vin (LNA) = 70dBμV | - | 450 | - | mVp-p |

Electrical Characteristics

(Unless otherwise specified, Ta = 25°C, VCC = 3.0 V, f = 2450 MHz, Bit Rate = 100kHz, PA = 21 setting, Dev = ± 160 kHz)

LNA and Mixer Blocks

| | | | | | | | |
|---|--------------------|---|--|------|-----|------|------|
| Mixer image rejection ratio | IRR | 1 | | 20 | 33 | — | dB |
| Output impedance | R-OUT (MIX) | — | | — | 470 | — | Ω |
| Output capacitance | C-OUT (MIX) | — | | — | 2 | — | pF |
| Operating frequency range (LNA and mixer) | Fopr (LNA + MIX) | 1 | | 2400 | — | 2500 | MHz |
| Intercept point 1 output (LNA and mixer) | OIP3-1 (LNA + MIX) | — | f1 (UD1) = 2453 MHz, UD1: No modulation f2 (UD2) = 2456 MHz, UD2: No modulation | — | 85 | — | dBμV |

IF Amplifier, DET and RX-LPF Blocks

| | | | | | | | |
|--------------------------------|------------|---|-------------------------------------|--------|--------|--------|----|
| RSSI output voltage 1 | V (RSSI-1) | 1 | Vin (IF) = 41dBμV, No modulation | 0.36 | 0.54 | 0.72 | V |
| RSSI output voltage 2 | V (RSSI-2) | 1 | Vin (IF) = 91dBμV, No modulation | (1.25) | (1.75) | (2.25) | V |
| IF amplifier input impedance | R-IN (IF) | — | | — | 720 | — | Ω |
| IF amplifier input capacitance | C-IN (IF) | — | | — | 2 | — | pF |

Comparator

| | | | | | | | |
|----------------------------|---------------|---|--|----|----|----|----|
| Duty ratio | COMP (duty) | 1 | Open-drain output Internal time constant setting 1 (10 kΩ) | 40 | 50 | 60 | % |
| High-level leakage current | I (COMP-LEAK) | 1 | Open-drain output | — | 0 | 5 | μA |
| Output ON resistance | R (COMP-L) | — | IL = 100 μA | — | 1 | — | kΩ |

PLL Block

| | | | | | | | |
|---|-------------|---|--|-----|-----|-----|------|
| Lock-up time | t-lock | 1 | Phase comparison frequency: 500 kHz Charge pump output current = 4 mA | — | 150 | — | μs |
| Reference clock operating frequency range | fxin | 1 | | 4 | — | 20 | MHz |
| Reference clock input level range | vxin | 1 | | 92 | 100 | 112 | dBμV |
| Clock (serial data) input frequency | fclk | 1 | | — | — | 20 | MHz |
| Charge pump output current 1 | Icp (1) | 1 | Vcp = 1/2VCC | 350 | 500 | 650 | μA |
| Charge pump output current 2 | Icp (2) | 1 | Vcp = 1/2VCC | 0.7 | 1 | 1.3 | mA |
| Charge pump output current 3 | Icp (3) | 1 | Vcp = 1/2VCC | 1.4 | 2 | 2.6 | mA |
| Charge pump output current 4 | Icp (4) | 1 | Vcp = 1/2VCC | 2.8 | 4 | 5.2 | mA |
| LD OFF leakage current | LD-off-LEAK | 1 | Open-drain output | — | 0 | 5 | μA |
| LD ON resistance | R(LD-on) | 1 | Open-drain output | — | 1 | — | kΩ |

VCO Block

| | | | | | | | |
|---------------------------------------|---------|---|----------|------|-----|------|--------|
| VCO Oscillation frequency range (× 2) | f (VCO) | 1 | | 2400 | — | 2500 | MHz |
| VCO gain (× 2) | Kv | — | | — | 120 | — | MHz/V |
| VCO phase noise (× 2) | pn1 | — | @500 kHz | — | 107 | — | dBc/Hz |
| | pn2 | — | @2 MHz | — | 119 | — | dBc/Hz |

Electrical Characteristics

(Unless otherwise specified, $T_a = 25^\circ\text{C}$, $V_{CC} = 3.0\text{ V}$, $f = 2450\text{ MHz}$, Bit Rate = 100kHz, PA = 21 setting, Dev = $\pm 160\text{ kHz}$)

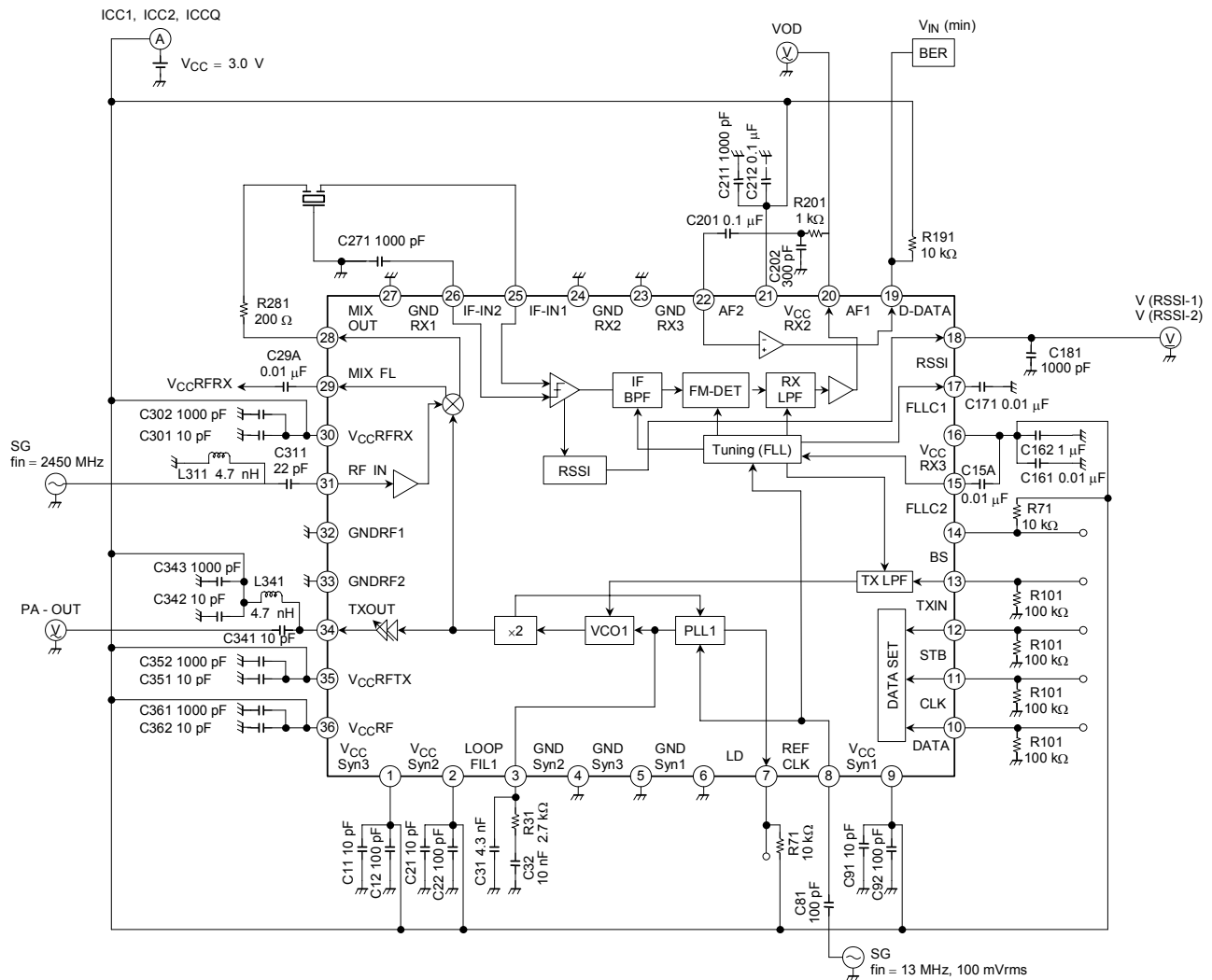
Transmission Block

| | | | | | | | |
|-----------------------------|----------|---|---------------------------|---------------------|----------|----------------|-----|
| Tx data input level | V_{tx} | — | | $V_{CC} \times 0.8$ | V_{CC} | $V_{CC} + 0.2$ | V |
| Local leakage spurious | SPRlo | 1 | Test frequency: 1.225 GHz | — | -30 | -20 | dBm |
| Maximum frequency deviation | dev (tx) | 1 | On loop, fBB=100kHz (CW) | (140) | (190) | (230) | KHz |

PA Block

| | | | | | | | |
|-----------------------------|---------------|---|--------------------------|------|-------|-------|----------|
| Nominal output signal level | PA-OUT (nom.) | 1 | DATA21 set for PA output | (-9) | (-3) | — | dBm |
| Minimum output signal level | PA-OUT (min.) | 1 | DATA3 set for PA output | — | (-30) | (-25) | dBm |
| Output impedance | Z-OUT (PA) | 1 | | — | 50 | — | Ω |

Test Circuit 1



- (1) Detailed test condition of minimum input level in the integrated characteristics
 - Detector LPF: C202 = 300 pF, R201 = 1 k Ω and f_T = 530 kHz
 - Total bits: 1.6 Mbits
 - Data comparator output: Monitors using a probe.
 - Input/output: LNA input, data comparator output
 - Transmission modulation (DEV): 157.5 kHz
 - Data: PRBS9 (1MBPS)
 - BT = 0.5 gaussian filter
 - IF filter used. (Note)
 - Tested using a Toshiba's mounting board

Note: Ceramic filter manufacturer and product no.

SFSCB11M0WF manufactured by Murata Manufacturing Co., Ltd.

- (2) Detailed test condition in the transmission block
 - Tested using a Toshiba's mounting board
- (3) Detailed test condition of output level in the PA block
 - Tested using a Toshiba's mounting board

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