Layout Recommendation and Test Board for PLL502-02

This note provides Layout recommendations for the PLL502-02 and documents the test board prepared for the PLL502-02

Best phase noise and jitter performance is achieved by applying good decoupling practices between VDD and GND, and best pull-range performance is obtained by optimizing the layout in order to minimize parasitic capacitances on the board.

As an example, and to simplify testing and evaluation of PLL502-02 by customers, PhaseLink provides a test board that implements the best approaches for decoupling the VCXO chip using discrete external components. It is brought to the attention of our customers that PLL502-02 is pin-to-pin compatible with PLL501-01 and PLL501-05, with the exception of pin#2 which is not connected internally on PLL502-02.

While this test board achieves satisfactory decoupling results, best results are achieved when the VCXO chip is laid out into the final PCB, following the recommendations indicated in the data sheet.

1. External Components and Layout Recommendations (as per PLL502-02 data sheet)

The PLL502-02 requires a minimum number of external components for proper operation. A standard low frequency decoupling capacitor of 4.7µF or more should be used between VDD (pin 6) and GND. Additionally, higher frequency decoupling capacitors of 0.1µF are required between VDD and GND. These higher frequency decoupling capacitors must be connected as close to the PLL502-02 chip as possible, and preferably directly next to the PLL502-02 pins. A series termination resistor of 33Ω may be used for the clock output (series termination resistor not implemented on test board).

The input crystal must be connected as close to the chip as possible, and preferably directly next to the PLL502-02 pins. Care must be given to the C_L rating of the crystal: at nominal voltage control (1.65V) the load capacitance presented to the crystal by the PLL502-02 is 9.5pF. Therefore, if a crystal with C_L higher than 9.5pF is used, it will require additional (fixed) loading capacitors externally to complement the internal 9.5pF of the PLL502-02: one between each crystal electrode and GND, as close to the crystal as possible, and preferably directly next to the crystal electrodes. Example, for crystal rated for C_L = 14.5pF, two external 10pF capacitors (one between each electrode of the crystal and GND) are required in order to load the crystal correctly. The two external capacitors (seen in series by the crystal) result in an additional 5pF in parallel to the 9.5pF presented by the PLL502-02, thus providing the total 14.5pF required by the crystal (9.5pF // 5pF = 14.5pF). However, if the crystal used with the PLL502-02 is rated for a CL = 9.5pF, no external capacitors are requiredConsult PhaseLink for recommended suppliers.

2. Crystal Specifications (as per PLL502-02 data sheet)

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode	10		20	MHz
Crystal Loading Capacitance Rating	C_L (xtal)	At VIN = 1.65V		9.5		pF
Crystal Pullability	C_0/C_1 (xtal)	AT cut			250	-
Recommended ESR	R_E	AT cut			30	Ω

3. Test board schematic

Note: C5 and C4 are only required if a crystal of C_L greater than 9.5 pF

Please order a test board without external C5 and C4 capacitors if you intend to use a crystal of CL equal to 9.5pF.