

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

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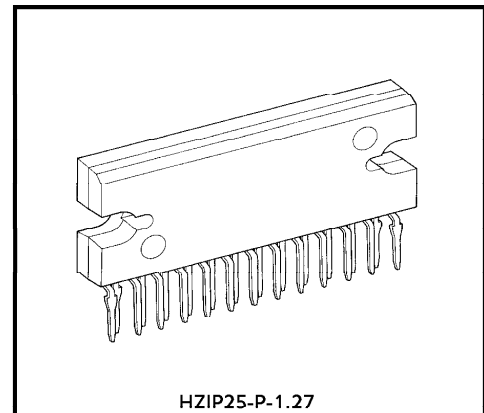
2 PHASE BIPOLAR STEPPER + FULL BRIDGE DRIVER

The TB6500AH is Stepping Motor Driver IC incorporates Dual Bipolar Stepping Motor Drivers.

DC Motor Driver and Serial to Parallel signal conversion circuit (12bit Serial to Parallel shift Resistor with Latch) which control the 3 output drivers states by means of input serial signal trains.

FEATURES

- Package : HZIP25-P
- All CMOS compatible input
- 2 Bipolar Stepping Motors and 1 Full Bridge Motor are controlled by input serial signal trains.
- Output current up to 0.8A (for Stepper) and 0.6A (for DC Motor)
- PWM chopper type Stepping Motor Drivers.
- Wide range of operating supply voltage : $V_M = 0 \sim 27V$
: $V_{CC} = 4.5 \sim 5.5V$
- Built-in thermal shut down, power supply monitor circuit.

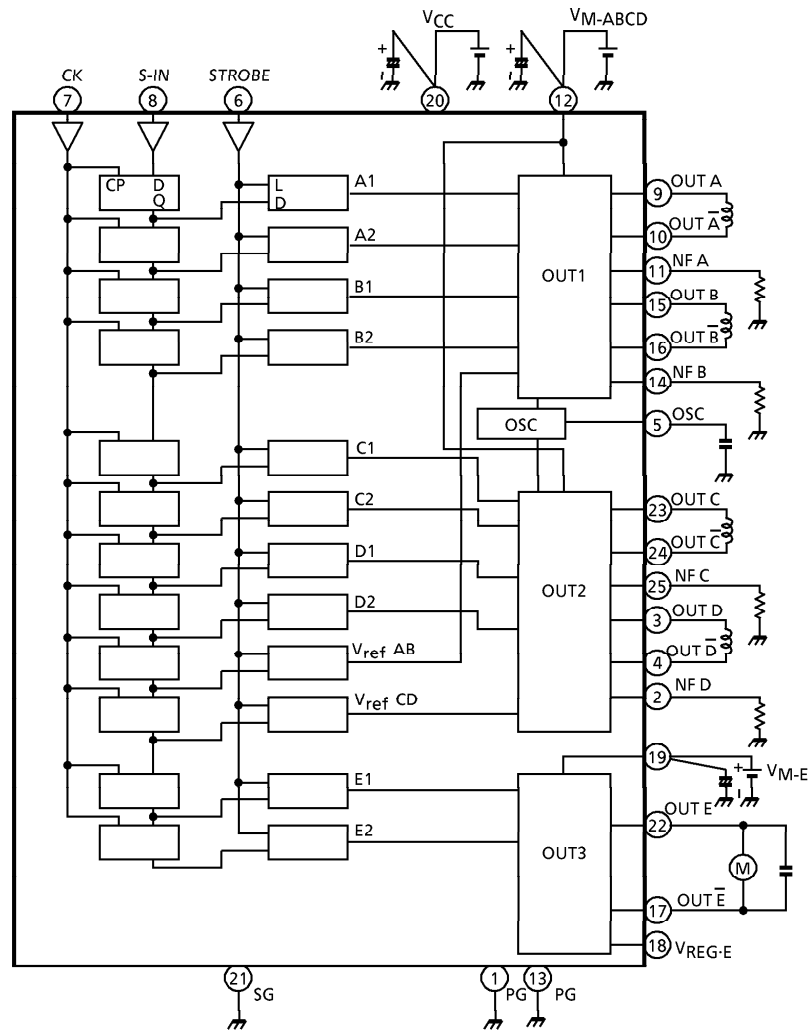


Weight : 9.86g (Typ.)

961001EBA2

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BLOCK DIAGRAM



Capacitance connect to each power supply terminal is required to change to optimum value for noise elimination and also required to connect directly to each power supply terminal (V_{CC} , V_M) and the corresponding GND terminal (see Table 1) for stable operations.

Table 1

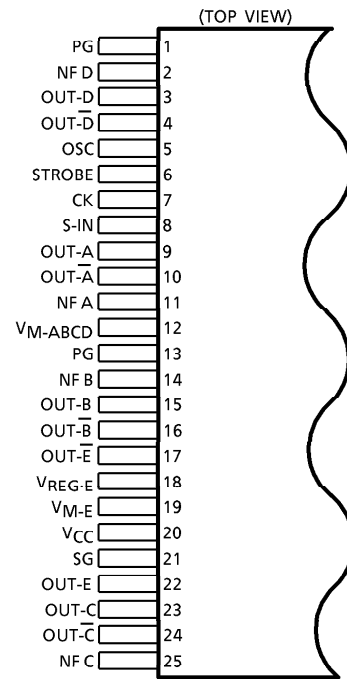
GND	POWER SUPPLY
Pin②①	Pin②① (V_{CC})
Pin①③	Pin①② (V_M -ABCD)
Pin①	Pin①⑨ (V_M -E)

Heat Fin is connect to GND terminal with Low Impedance.

PIN FUNCTION

PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION
1	PG	Power GND terminal
2	NFD	D channel current detective terminal
3	OUT-D	Output D channel
4	OUT- \bar{D}	Output \bar{D} channel
5	OSC	Internal oscillation frequency setting terminal
6	STROBE	STROBE signal input terminal
7	CK	CLOCK signal input terminal
8	S-IN	Serial signal input terminal
9	OUT-A	Output A channel
10	OUT- \bar{A}	Output \bar{A} channel
11	NFA	A channel current detective terminal
12	V _M -ABCD	Power voltage supply terminal for motor driver
13	PG	Power GND terminal
14	NFB	B channel current detective terminal
15	OUT-B	Output B terminal
16	OUT- \bar{B}	Output \bar{B} terminal
17	OUT- \bar{E}	Output \bar{E} terminal
18	V _{REG-E}	External reference voltage input terminal
19	V _{M-E}	Power voltage supply terminal for motor driver
20	V _{CC}	Power voltage supply terminal for control
21	SG	Signal GND terminal
22	OUT-E	Output E terminal
23	OUT-C	Output C terminal
24	OUT- \bar{C}	Output \bar{C} terminal
25	NFC	C channel current detective terminal

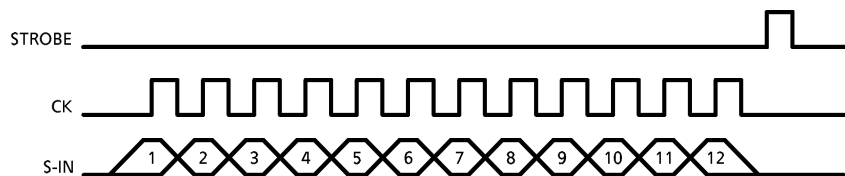
PIN CONNECTION



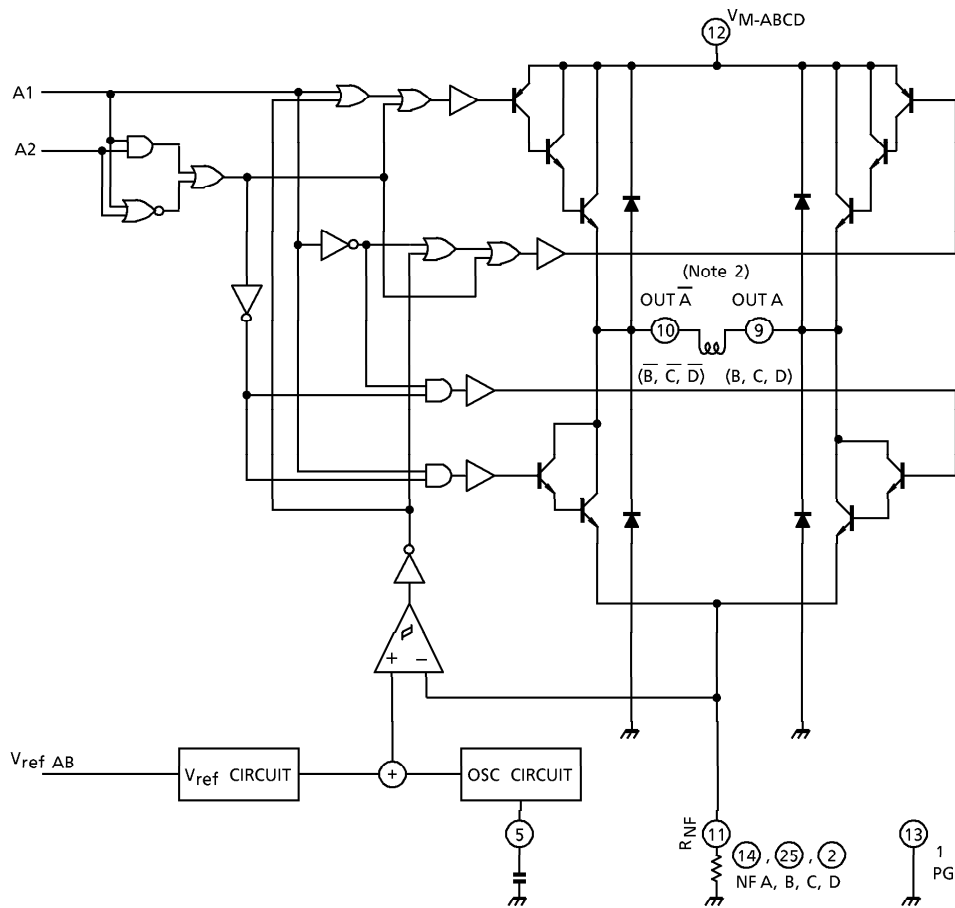
INPUT SERIAL PULSE TRAIN AND POWER OUTPUT STATES

SERIAL INPUT SIGNAL TRAIN		CONTROL	OPERATION				
1	E2	DC motor control	INPUT		OUTPUT		MODE
			E1	E2	E	\bar{E}	
L	L		∞	∞	STOP		
H	L		H	L	CW/CCW		
L	H		L	H	CCW/CW		
2	E1		H	H	L	L	BREAK
3	V _{ref} -CD	Stepping motor 2 chapping rate control (V _{ref} CD)	V _{ref} = 0.85V (Typ.) (at "H" mode)				
4	V _{ref} -AB	Stepping motor 1 chapping rate control (V _{ref} AB)	V _{ref} = 0.65V (Typ.) (at "L" mode)				
5	D2	Stepping motor 2 control (Out C, D)	INPUT		OUTPUT		MODE
6	D1		A1	A2	A	\bar{A}	
7	C2		L	L	∞	∞	STOP
8	C1		H	L	H	L	CW/CCW
9	B2	Stepping motor 1 control (Out A, B)	L	H	L	H	CCW/CW
10	B1		H	H	∞	∞	STOP
11	A2		B1, B2 → B, \bar{B} C1, C2 → C, \bar{C} D1, D2 → D, \bar{D} are all the same.				
12	A1						

INPUT SERIAL PULSE TRAIN TIMING CHART



OUTPUT STAGE 1, 2 1/2 CIRCUIT



FUNCTION (Comp. + > Comp. -) (Note 1)

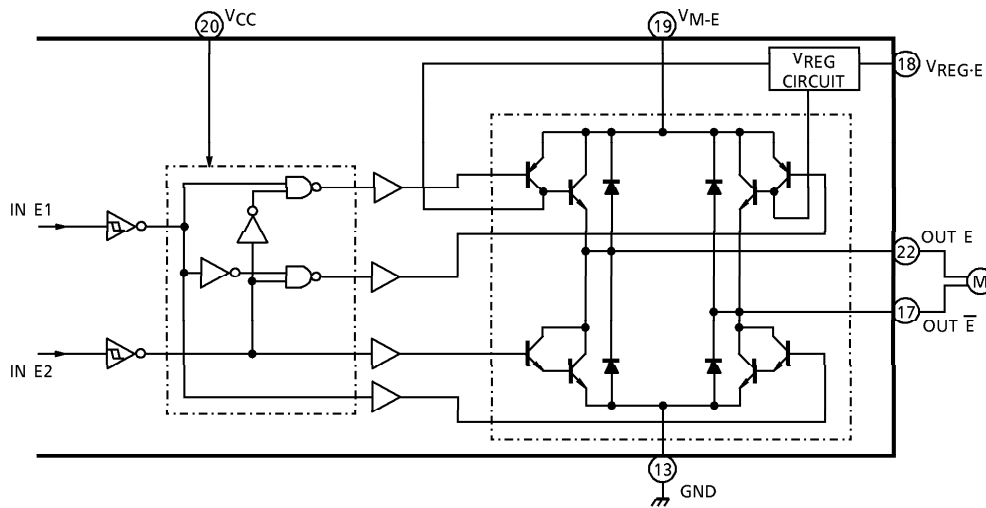
A1	A2	OUT A	OUT Ā	MODE
L	L	∞	∞	STOP
H	L	H	L	CW / CCW
L	H	L	H	CCW / CW
H	H	∞	∞	STOP

(Note 1) In case of Comp. + < Comp. -, Upper side power transistor turned off.

(Note 2) Free wheeling diode connects between output A terminal and GND is required for stable operating.

And also recommend to connect free wheeling diodes other output terminals for reliable operations.

OUTPUT STAGE 3

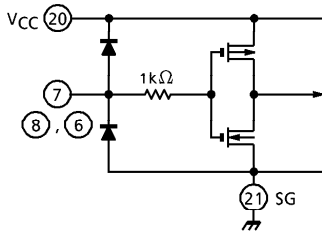


FUNCTION

INPUT		OUTPUT		MODE
IN E1	IN E2	OUT E	OUT E-bar	
L	L	∞	∞	STOP
H	L	H	L	CW / CCW
L	H	L	H	CCW / CW
H	H	L	L	BREAK

∞ : High Impedance
 (Note) : Inputs are all high active type

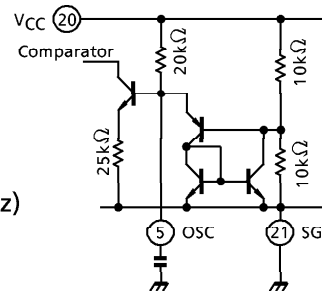
INPUT STAGE (CK, S-IN, STROBE terminal)



$$f_{OSC} = \frac{1}{21.4 \cdot C_{OSC}} \text{ (kHz)}$$

(C_{OSC} μF)

OSC STAGE (OSC terminal)



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage (Motor)	V _M	30	V
Supply Voltage (Control)	V _{CC}	7.0	V
Input Voltage	V _{IN}	7.0	V
Output Current	I _O ABCD	±0.8	A
	I _O E	±0.6	
Power Dissipation	P _D	(Note) 43	W
		5	
Operating Temperature	T _{opr}	-40~85	°C
Storage Temperature	T _{stg}	-55~150	°C

(Note) T_c = 85°C

RECOMMENDED OPERATING CONDITION (Ta = -20~75°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage (Control)		V _{CC}		4.5	5.0	5.5	V
Supply Voltage (Motor)		V _M		21.6	24	26.4	V
Input Voltage		V _{IN}		0	—	V _{CC}	V
Output Current	I _{OUT} ABCD	I _{OUT}		—	—	0.7	A
	I _{OUT} E			—	—	0.6	
Clock Frequency		f _{CK}		—	—	1.0	MHz
		f _{STROBE}		—	—	1.0	
Clock Pulse Width		tw _{CK}		500	—	—	ns
		tw _{STROBE}		500	—	—	
Data Set Up Time		ts _{uCK-S-IN}		250	—	—	ns
		ts _{uST-CK}		250	—	—	
Data Hold Time		th _{CK-S-IN}		250	—	—	ns
		th _{ST-CK}		250	—	—	
PWM Oscillation Frequency		fp _{WPM}		20	—	100	kHz

ELECTRICAL CHARACTERISTICS

Output stage (Ta = 25°C, V_{CC} = 5V, V_M = 24V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Operation Power Supply Voltage		V _M (opr.)			0	—	27	V	
Saturation Voltage	AB CD	V _{SATU-1}	1	I _{OUT} = 0.7A	Output-V _M	—	2.2	2.7	V
				I _{OUT} = 0.5A		—	2.0	2.5	
	AB CD	V _{SATL-1}		I _{OUT} = 0.7A	Output-N _F	—	1.5	2.0	
				I _{OUT} = 0.5A		—	1.3	1.8	
	E	V _{SATU-2}		I _{OUT} = 0.5A	Output-V _M	—	2.2	2.7	
				I _{OUT} = 0.3A		—	2.0	2.5	
E	V _{SATL-2}	I _{OUT} = 0.5A	Output-PG	—	1.5	2.0			
		I _{OUT} = 0.3A		—	1.2	1.7			
E-ch Output Voltage		V _{OE}	1	I _{OUT} = 0.5A I _{OUT} = 0.3A	V _{REG-E} = 15V	— —	15 15	— —	V
Reference Current		I _{REG}	1	V _{REG-E} = 15V	—	50	100	μA	
Reference Voltage		V _{REG-E} (opr.)	1		0	—	22	V	
Output Leak Current		I _{OL-H}	2	V _{CE} = 30V	—	—	50	μA	
		I _{OL-L}			—	—	50		
Clamp Diode Forward Voltage	AB CD	V _{F-U1}	3	I _F = 0.7A, Output A-D	—	1.6	2.0	V	
		V _{F-L1}			—	1.2	1.6		
	E	V _{F-U2}		I _F = 0.5A, Output E	—	1.5	1.9		
		V _{F-L2}			—	1.3	1.7		

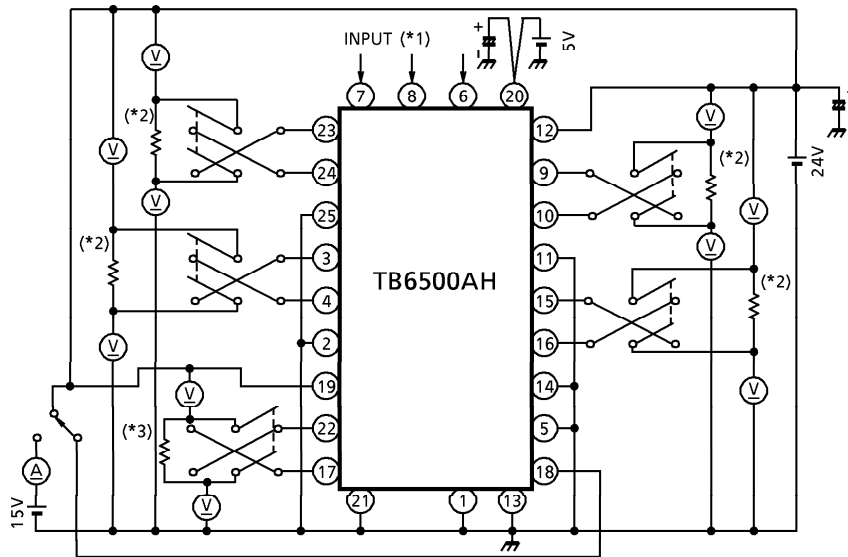
Small signal stage (Ta = 25°C, VCC = 5V, VM = 24V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT		
Operation Supply Voltage	VCC (opr.)			4.5	—	5.5	V		
Quiescent Current	ICC1	4	CK, ST, S-IN : Open	—	30	50	mA		
	ICC2		CK : 1MHz, DATA : 1/2fCLK Output ON	—	30	50			
	ICC3		CK : 1MHz, DATA : 1/2fCLK Output OFF	—	30	50			
	IM-ABCD		4	Output open, Input serial signal (A1, B1, C1, D1 = "H" A2, B2, C2, D2 = "H") Output ON	—	30	40	μA	
				Output open Output OFF	—	—	50		
	IM-E		4	CW, CCW, BREAK Output ON, Output open	—	5	12	mA	
				Output open Output OFF	—	—	50	μA	
Input Voltage	VIN (H)	5	CK, S-IN, ST	3.5	—	VCC +0.4	V		
	VIN (L)			GND -0.4	—	1.5			
Input Current	IIN (H)	5	VINH = 5.4V	-3	—	3	μA		
	IIN (L)		VINL = 0.4V	-3	—	3			
Chopping Voltage Level	Vref (H)	6	Tj = -40~125°C COSC = 3300pF RNF = 3.3Ω L = 19.5mH	Vref IN = H	0.75	0.85	0.95	V	
	Vref (L)			Vref IN = L	0.55	0.65	0.75		
Vref Level Differential Voltage	ΔVchop		Vref (H) - Vref (L)	—	0.2	—	V		
Reset Voltage	VCCR	7		3.6	3.8	4.1	V		
Min. Reset Pulse	tVCCR				—	—	1	μs	
Min. PWM Frequency	fPWML	4		—	—	10	kHz		
Max. PWM Frequency	fPWMH				200	—		—	
Thermal Shut Down	TSD (ON)	—	Tj		120	140	160	°C	
Thermal Shut Down	TSD (OFF)					110	130		150
Differential Temperature	ΔTSD				TSD (ON) - TSD (OFF)	—	10		—

AC characteristics (Ta = 25°C, VCC = 5V)

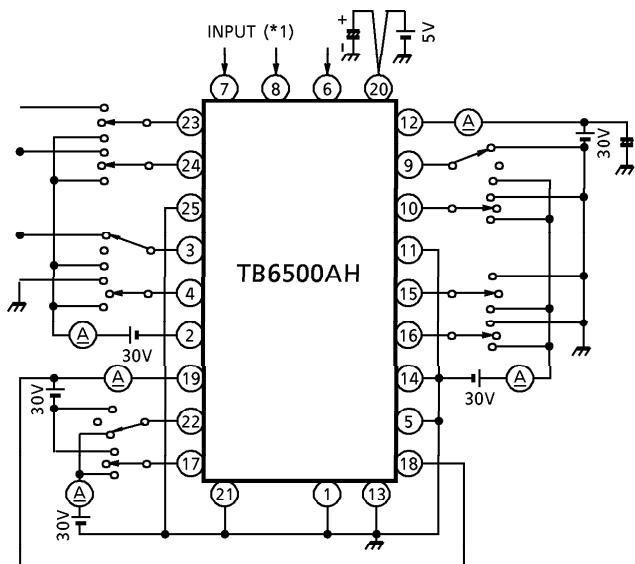
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
CLOCK Frequency	f _{CK}	7		—	—	1.5	MHz	
	f _{STROBE}			—	—	1.5		
Min. Clock Pulse Width	t _{CK}	7		340	—	—	ns	
	t _{STROBE}			340	—	—		
Data Set Up Time	t _{suCK-SIN}	7		170	—	—	ns	
	t _{suST-CK}			170	—	—		
Data Hold Up Time	t _{hCK-SIN}			170	—	—		
	t _{hST-CK}			170	—	—		
Output Propagation Time	t _{pLH}	7	CK-OUT	R _L = 40Ω C _L = 15pF	—	2	—	μs
	t _{pHL}				—	2	—	
	t _{pLH}		STROBE-OUT		—	2	—	
	t _{pHL}				—	2	—	
	t _{pON-Z}		V _{CC} -R-OUT		—	2	—	
	t _{pZ-ON}				—	2	—	
Max. Clock Rise Time	t _{rMAX}	7		—	—	1	μs	
Max. Clock Fall Time	t _{fMAX}			—	—	1		
Output Rise Time	t _r			R _L = 40Ω C _L = 15pF	—	1		—
Output Fall Time	t _f			—	—	1		—
E-ch Output Dead Time	t·dead			R _L = 100Ω C _L = 15pF	—	250		—

TEST CIRCUIT 1 $V_{SATU-1\cdot2}$, $V_{SATL-1\cdot2}$



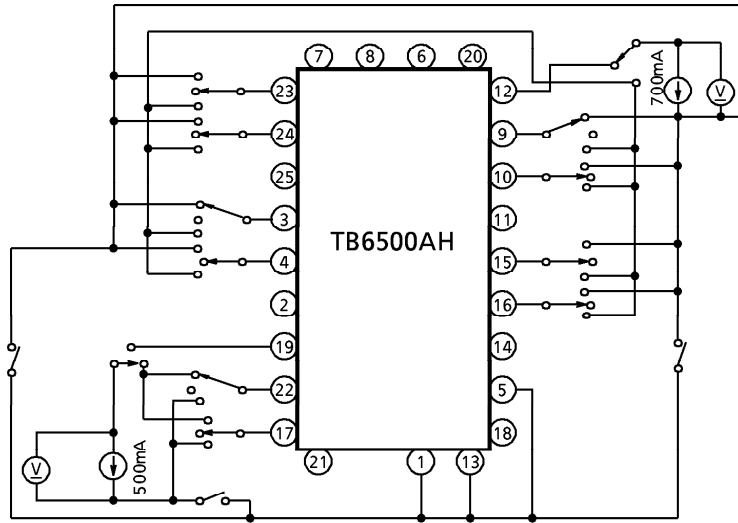
- (*1) Set output transistor active with input mode select.
- (*2) Calibrate output current becomes 0.5A (or 0.7A) with this resistor.
- (*3) Calibrate output current becomes 0.3A (or 0.5A) with this resistor.

TEST CIRCUIT 2 I_{OL-H} , I_{OL-L}



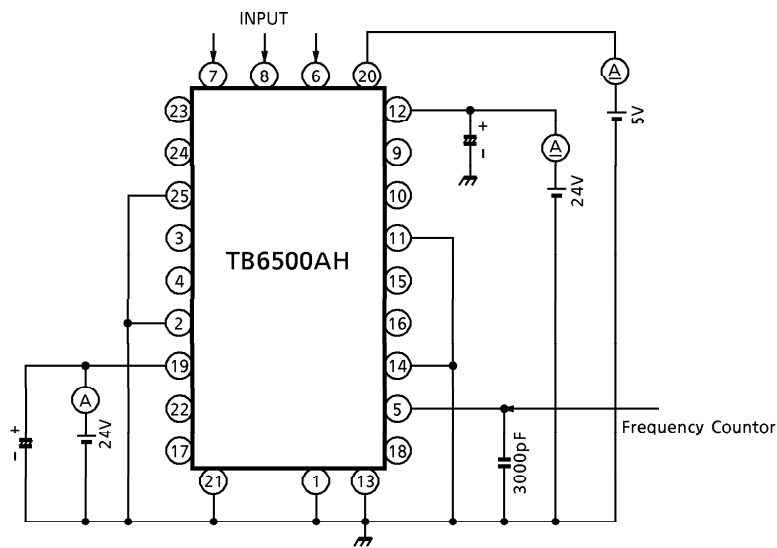
- (*1) All "L" level S-IN signal, normal CK and STROBE signals are required to measure.

TEST CIRCUIT 3 V_F -U1·2, V_F -L1·2

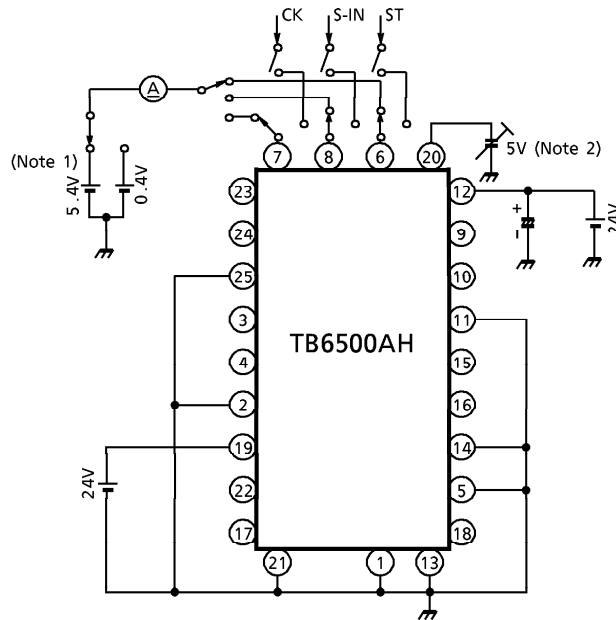


(Note) Not to take a GND with any non-connecting pins.

TEST CIRCUIT 4 I_{CC} 1·2·3, I_M : ABCD·E, f_{PWML} ·H



TEST CIRCUIT 5 I_{INH} , I_{INL} , V_{INH} , V_{INL} , V_{CCR}



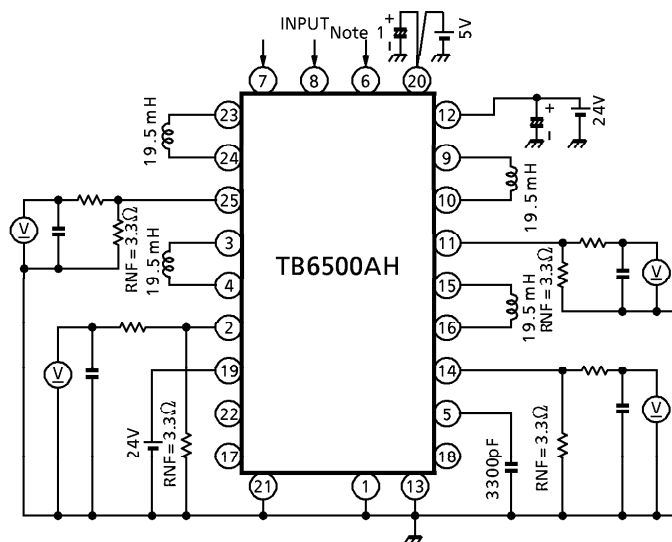
V_{IN} level

(Note 1) Apply signals to CK, S-IN, and STROBE at the levels shown in the diagram and check function.

Power supply monitor level

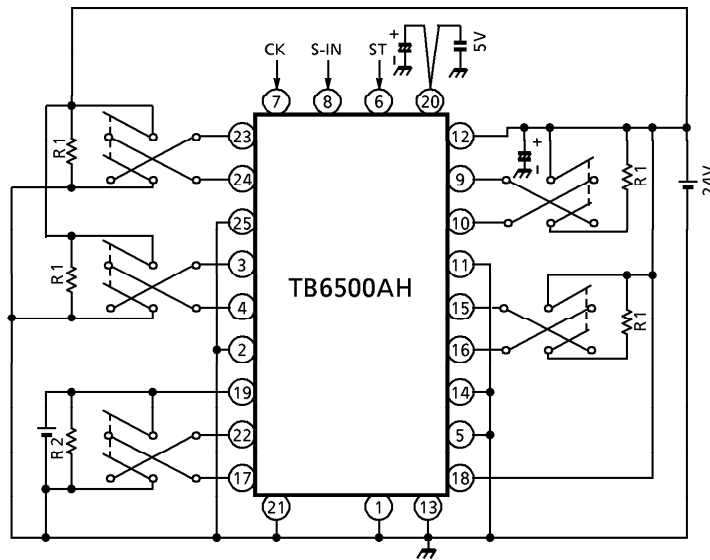
(Note 2) Change the power supply voltage and check the output operation.

TEST CIRCUIT 6 V_{refH} , V_{refL} , ΔV_{ref}



(Note 1) Hold the state (2 phase excitation mode) and measure.

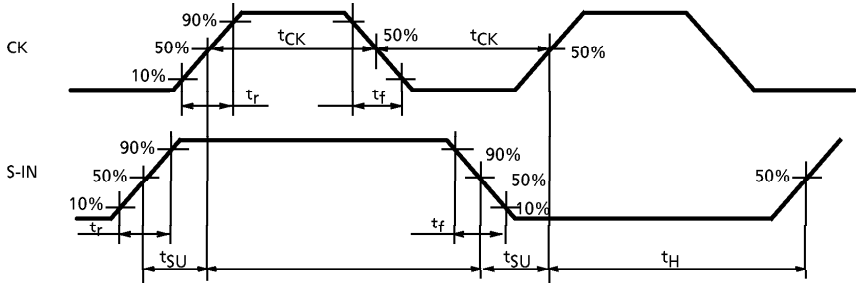
TEST CIRCUIT 7 (Calibrate I_O to 0.6A by R1, 0.5A by R2)



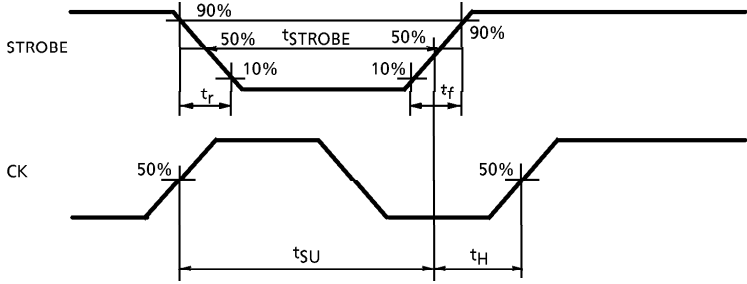
- 7-1. Set the STROBE terminal to high level and compare the output with the data in the waveform shown in Fig.7-1.
- 7-2. Check that the output is latched in the waveform as shown in Fig.7-2.
- 7-3. Check the CK or STROBE, and the output delay time in the waveform as shown in Fig.7-3.
- 7-4. Change the V_{CC} voltage, and check the delay with the output in the waveform as show in Fig.7-4.

AC ELECTRICAL CHARACTERISTICS

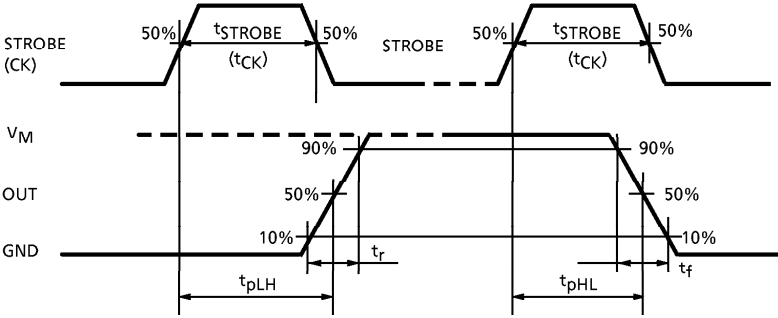
7-1 : CK-S-IN



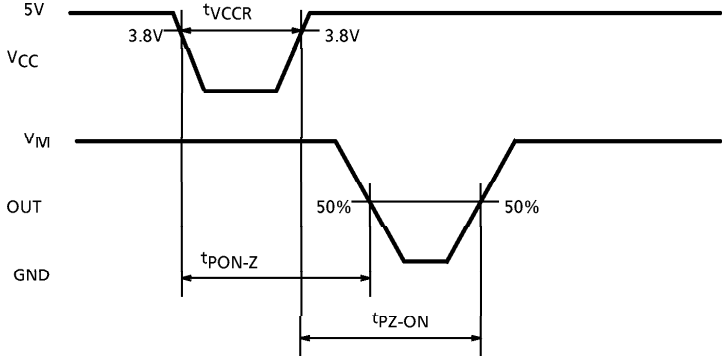
7-2 : STROBE-CK



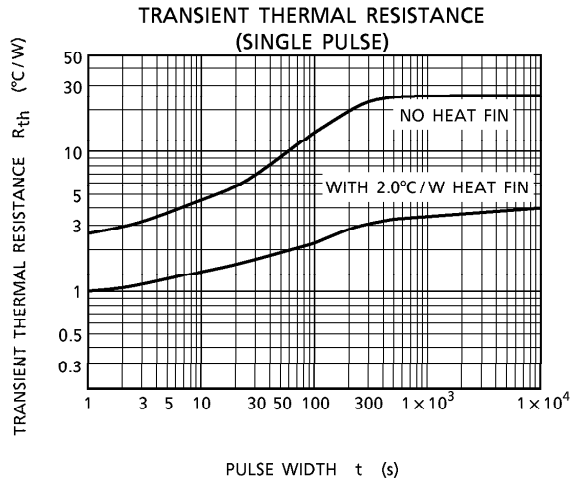
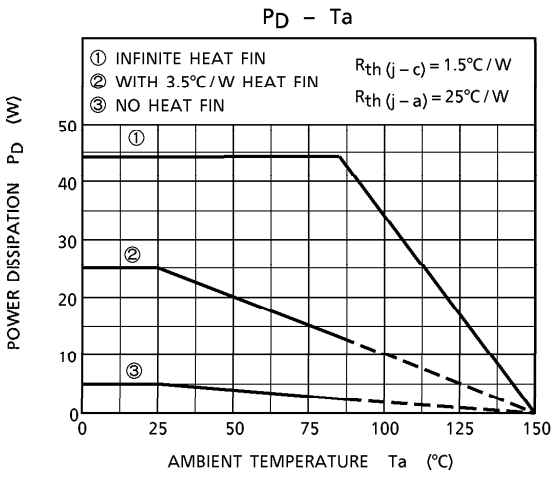
7-3 : STROBE (CK)-OUT



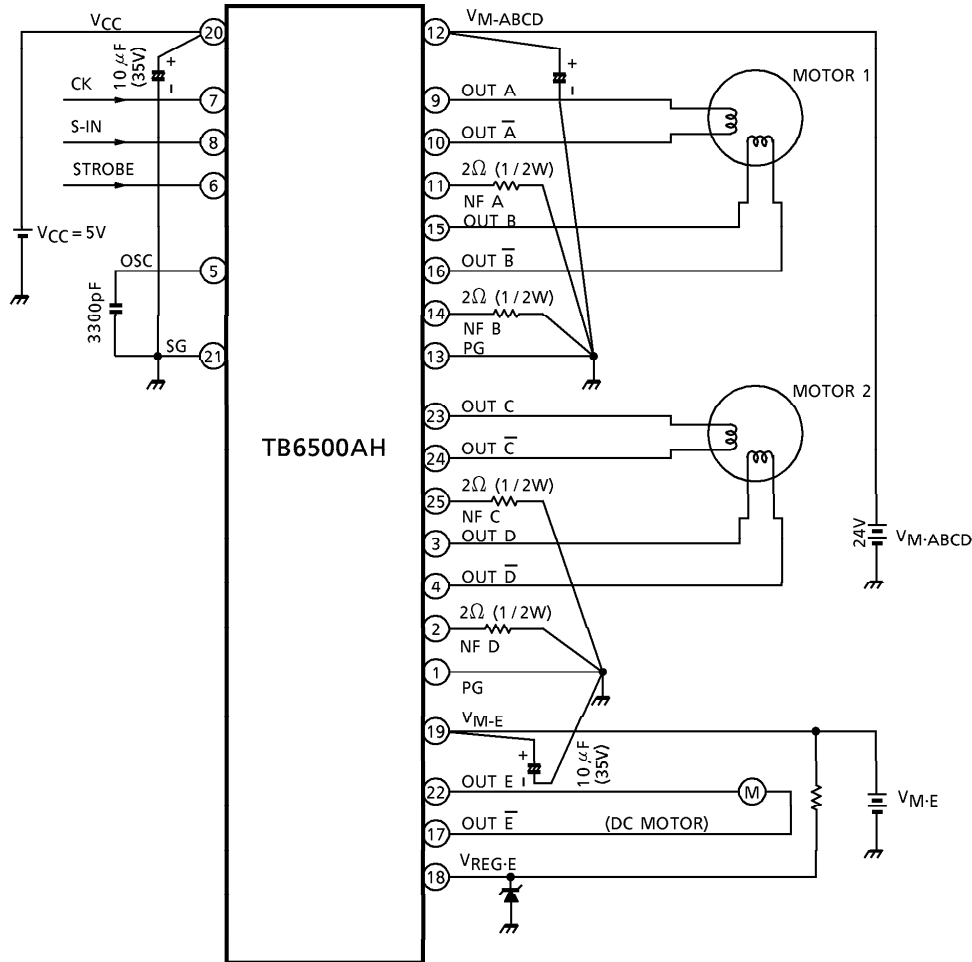
7-4 : V_{CCR}-OUT



When measuring the upper transistor, set the external load resistor between the output and GND, then measure at the output terminal.
 When measuring the lower transistor, set the external load resistor between the output and V_M then measure at the output terminal.



APPLICATION CIRCUIT



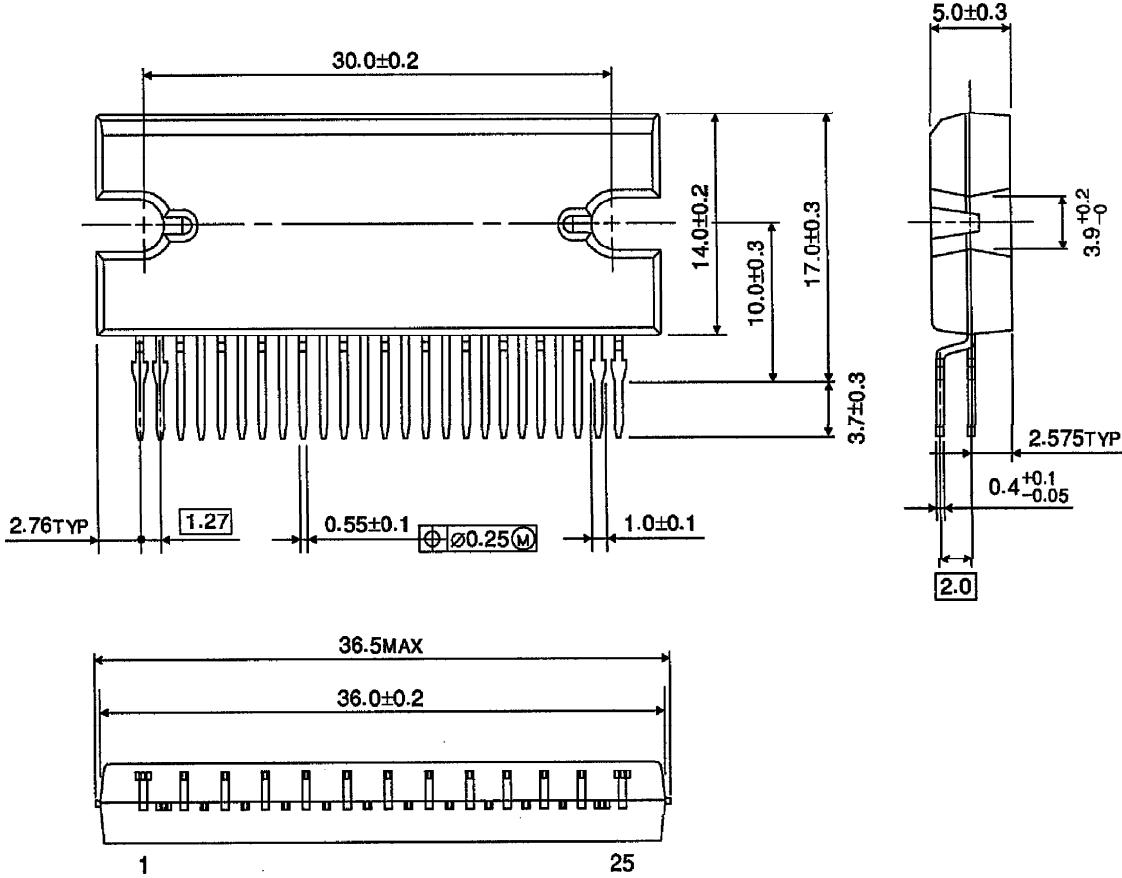
(Note 1) Care should be taken not to have a common impedance with output current pass of each motor (NF A, NF B for MOTOR 1, NF C, MOTOR 2 and PG for DC MOTOR) and any other signal lines.

And recommended to take one point GND with each output current pass and corresponding PG terminal. (see table 1 of BLOCK Diagram)

(Note 2) Utmost care is necessary in the design of the output line, V_M and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

OUTLINE DRAWING
HZIP25-P-1.27

Unit : mm



Weight : 9.86g (Typ.)