

TC514402AP/AJ/ASJ/AZ-60

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1~7	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ C$)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES	
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current (\overline{RAS} , \overline{CS} , Address Cycling: $t_{RC} = t_{RC} \text{ MIN.}$)	TC514402AP/AJ/ASJ/AZ-60	-	120	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{IH}$)		-	2	mA	
I_{CC3}	\overline{RAS} ONLY REFRESH CURRENT Average Power Supply Current, \overline{RAS} Only Mode (\overline{RAS} Cycling, $\overline{CS} = V_{IH}$; $t_{RC} = t_{RC} \text{ MIN.}$)	TC514402AP/AJ/ASJ/AZ-60	-	120	mA	3, 5
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, STATIC COLUMN Mode ($\overline{RAS} = \overline{CS} = V_{IL}$, Address Cycling: $t_{SC} = t_{SC} \text{ MIN.}$)	TC514402AP/AJ/ASJ/AZ-60	-	95	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{CC} - 0.2V$)		-	1	mA	
I_{CC6}	\overline{CS} BEFORE \overline{RAS} REFRESH CURRENT Average Power Supply Current, \overline{CS} Before \overline{RAS} Mode (\overline{RAS} , \overline{CS} Cycling: $t_{RC} = t_{RC} \text{ MIN.}$)	TC514402AP/AJ/ASJ/AZ-60	-	120	mA	3, 5
$I_{i(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test $\pm 0V$)		-10	10	μA	
$I_{o(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$)		-	0.4	V	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ\text{C}$) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514402AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	-	ns	
t_{SC}	Static Column Mode Cycle Time	35	-	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	90	-	ns	
t_{RAC}	Access Time from \overline{RAS}	-	60	ns	9,14 15
t_{CAC}	Access Time from \overline{CS}	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	ns	9,15
t_{ALW}	Access Time from Last Write	-	55	ns	9,16
t_{CLZ}	\overline{CS} to output in Low-Z	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	10
t_{AOH}	Output Data Hold Time from Column Address	5	-	ns	
t_{OW}	Output Data Enable Time from \overline{WRITE}	-	20	ns	
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	\overline{RAS} Precharge Time	40	-	ns	
t_{RAS}	\overline{RAS} Pulse Width	60	10,000	ns	
t_{RASC}	\overline{RAS} Pulse Width (Static Column Mode)	60	200,000	ns	
t_{RSH}	\overline{CS} to \overline{RAS} Hold Time	20	-	ns	
t_{CSH}	\overline{RAS} to \overline{CS} Hold Time	60	-	ns	
t_{CS}	\overline{CS} Pulse Width	20	10,000	ns	
t_{CSC}	\overline{CS} Pulse Width (Static Column Mode)	20	200,000	ns	
t_{RCD}	\overline{RAS} to \overline{CS} Delay Time	20	40	ns	14
t_{RAD}	\overline{RAS} to Column Address Delay Time	15	30	ns	15
t_{CRP}	\overline{CS} to \overline{RAS} Precharge Time	5	-	ns	
t_{CP}	\overline{CS} Precharge Time	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	ns	
t_{AR}	Column Address Hold Time referenced to \overline{RAS} (READ CYCLE)	70	-	ns	
t_{RAL}	Column Address to \overline{RAS} Lead Time	30	-	ns	
t_{AH}	Column Address Hold Time referenced to \overline{RAS} Rise	5	-	ns	17

SYMBOL	PARAMETER	TC514402AP/AJ/ASJ/AZ-60		UNITS	NOTES
		MIN.	MAX.		
t _{LWAD}	Last Write to Column Address Delay Time	20	25	ns	16
t _{AHLW}	Last Write to Column Address Hold Time	55	-	ns	
t _{RCS}	Read Command Set-up Time referenced to \overline{CS}	0	-	ns	
t _{RCH}	Read Command Hold Time referenced to \overline{CS}	0	-	ns	11
t _{RRH}	Read Command Hold Time referenced to \overline{RAS}	0	-	ns	11
t _{WCH}	Write Command Hold Time (Output Data Disable)	10	-	ns	13
t _{WP}	Write Command Pulse Width	10	-	ns	
t _{WI}	Write Command Inactive Time	10	-	ns	
t _{RWL}	Write Command to \overline{RAS} Lead Time	20	-	ns	
t _{CWL}	Write Command to \overline{CS} Lead Time	20	-	ns	
t _{DS}	Data-In Set-Up Time	0	-	ns	12
t _{DH}	Data-In Hold Time	15	-	ns	12
t _{REF}	Refresh Period	-	16	ms	
t _{WCS}	Write Command Set-UP Time (Output Data Disable)	0	-	ns	13
t _{CWD}	\overline{CS} to \overline{WRITE} Delay Time (READ-MODIFY-WRITE CYCLE)	50	-	ns	13
t _{RPWD}	\overline{RAS} to \overline{WRITE} Delay Time (READ-MODIFY-WRITE Cycle)	90	-	ns	13
t _{AWD}	Column Address to \overline{WRITE} Delay Time	60	-	ns	13
t _{CSR}	\overline{CS} Set-Up Time(\overline{CS} before \overline{RAS})	5	-	ns	
t _{CHR}	\overline{CS} Hold Time(\overline{CS} before \overline{RAS})	15	-	ns	
t _{RPC}	\overline{RAS} to \overline{CS} Precharge Time	0	-	ns	
t _{CPT}	\overline{CS} Precharge Time (\overline{CS} before \overline{RAS} Counter Test Cycle)	30	-	ns	
t _{ROH}	\overline{RAS} Hold Time referenced to \overline{OE}	10	-	ns	
t _{OEA}	\overline{OE} Access Time	-	20	ns	
t _{OED}	\overline{OE} to Data Delay	20	-	ns	
t _{OEZ}	Output Buffer turn off Delay Time from \overline{OE}	0	20	ns	10
t _{OEH}	\overline{OE} Command Hold Time	20	-	ns	

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SYMBOL	PARAMETER	TC514402AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t _{WTS}	Write Command Set-Up Time	10	-	ns	
t _{WTH}	Write Command Hold Time	10	-	ns	
t _{WRP}	WRITE to RAS Precharge Time	10	-	ns	
t _{WRH}	WRITE to RAS Hold Time	10	-	ns	

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE ($V_{CC} = 5V \pm 10\%$, $T_a = 0 \sim 70^\circ\text{C}$) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514402AP/AJ/ASJ/AZ-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	115	-	ns	
t_{SC}	Static Column Mode Cycle Time	40	-	ns	
t_{RAC}	Access Time from \overline{CS}	-	65	ns	9,14 15
t_{CAC}	Access Time from \overline{CS}	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	35	ns	9,15
t_{RAS}	\overline{RAS} Pulse Width	65	10,000	ns	
t_{RASC}	\overline{RAS} Pulse Width (Static Column Mode)	65	200,000	ns	
t_{RSH}	\overline{RAS} Hold Time	25	-	ns	
t_{CSH}	\overline{CS} Hold Time	65	-	ns	
t_{CS}	\overline{CS} Pulse Width	25	10,000	ns	
t_{CSC}	\overline{CS} Pulse Width (Static Column Mode)	25	200,000	ns	
t_{RAL}	Column Address to \overline{RAS} Lead Time	35	-	ns	

CAPACITANCE ($V_{CC} = 5V \pm 10\%$, $f = 1\text{MHz}$, $T_a = 0 \sim 70^\circ\text{C}$)

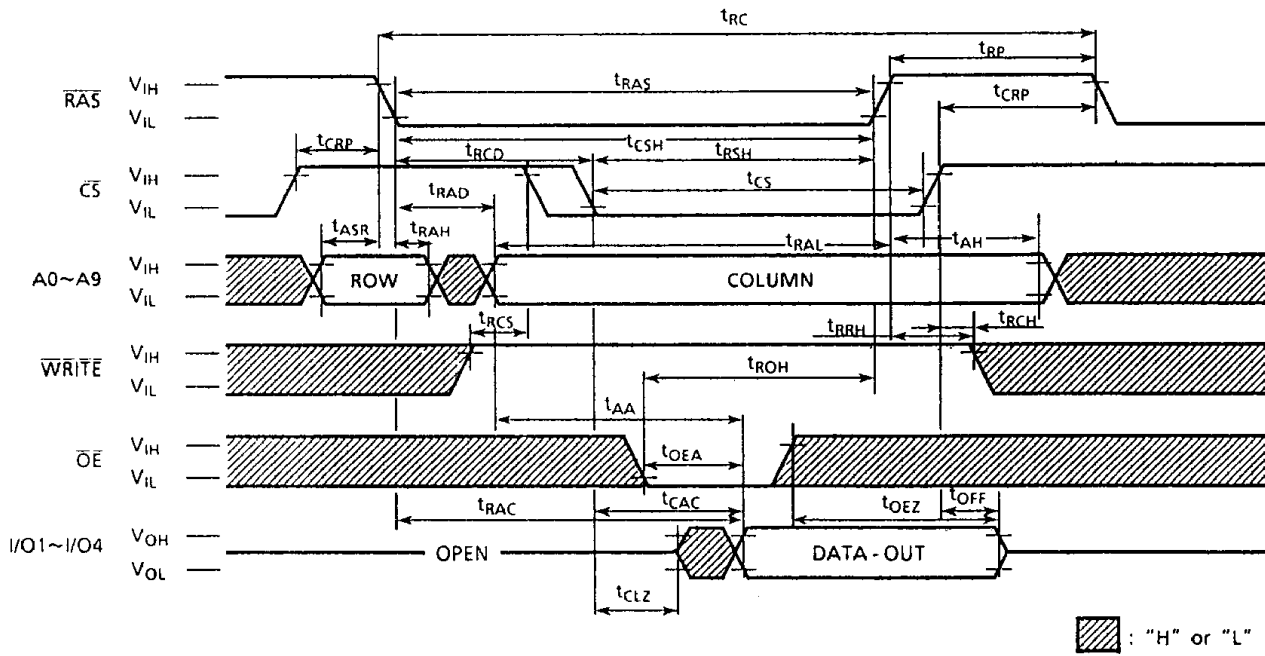
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9)	-	5	pF
C_{I2}	Input Capacitance (\overline{RAS} , \overline{CS} , \overline{WRITE} , \overline{OE})	-	7	pF
C_O	Input/Output Capacitance (I/O1~I/O4)	-	7	pF

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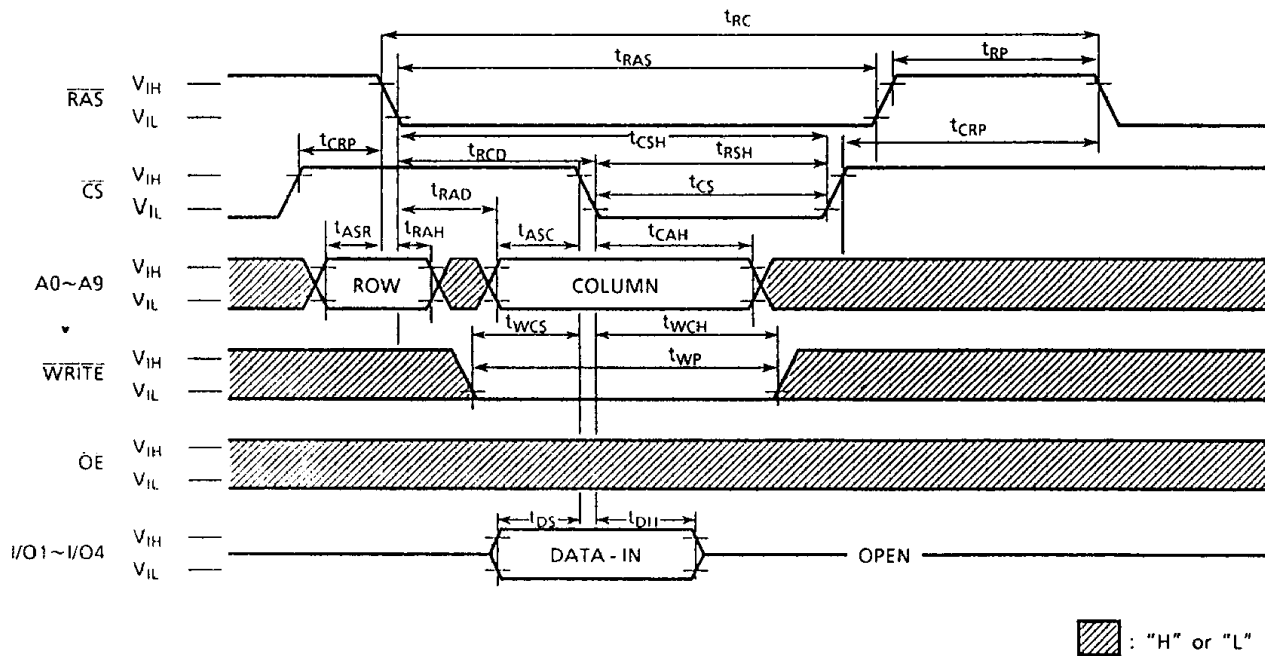
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS} .
3. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC6} depend on cycle rate.
4. I_{CC1} , I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS} = V_{IL}$.
6. An initial pause of 200 μ s is required after power-up followed by 8 \overline{RAS} only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 \overline{CS} before \overline{RAS} refresh cycles instead of 8 \overline{RAS} refresh cycles are required.
7. AC measurements assume $t_T = 5$ ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to \overline{CS} leading edge in early write cycles and to \overline{WRITE} leading edge in Read-Modify-Write cycles.
13. t_{WCS} , t_{RWd} , t_{CWD} and t_{AWd} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWd} \geq t_{RWd}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$ and $t_{AWd} \geq t_{AWd}(\text{min.})$ the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met.
 $t_{RCD}(\text{max.})$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
15. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met.
 $t_{RAD}(\text{max.})$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
16. Operation within the $t_{LWAD}(\text{max.})$ limit insures that $t_{ALW}(\text{max.})$ can be met.
 $t_{LWAD}(\text{max.})$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{LWAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
17. t_{AH} is the condition to latch column address ewhen \overline{RAS} has rised up.

READ CYCLE

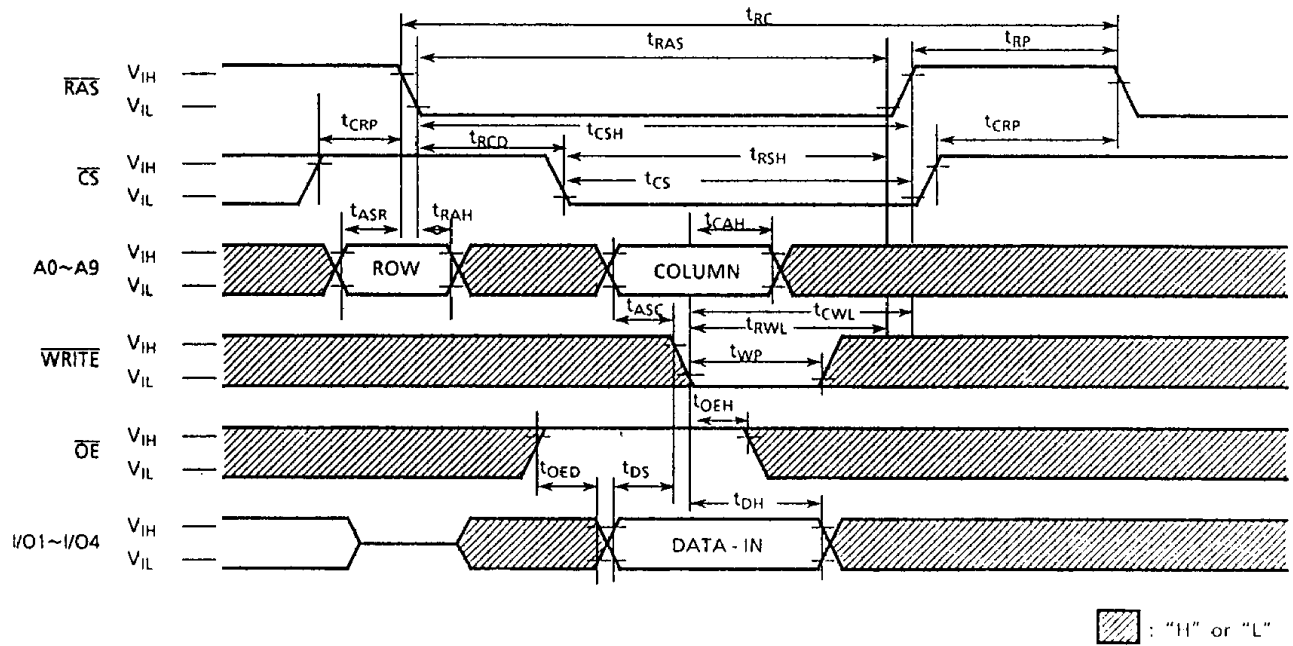


WRITE CYCLE (EARLY WRITE)

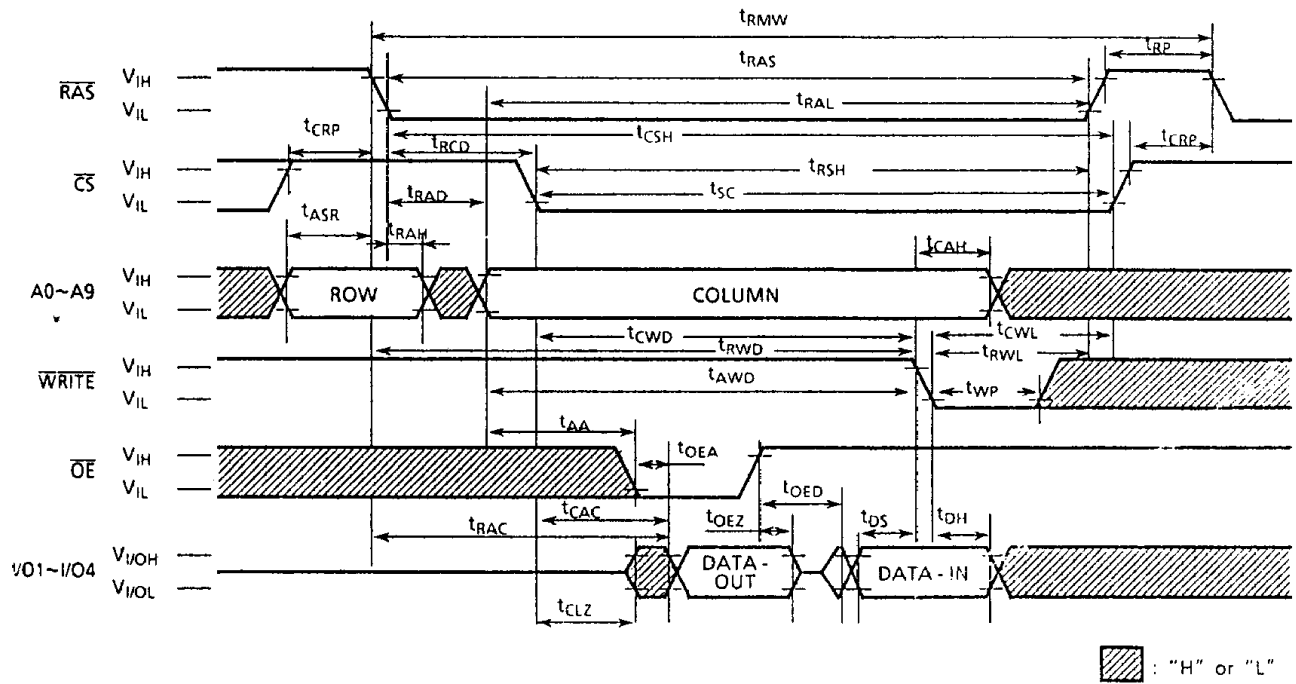


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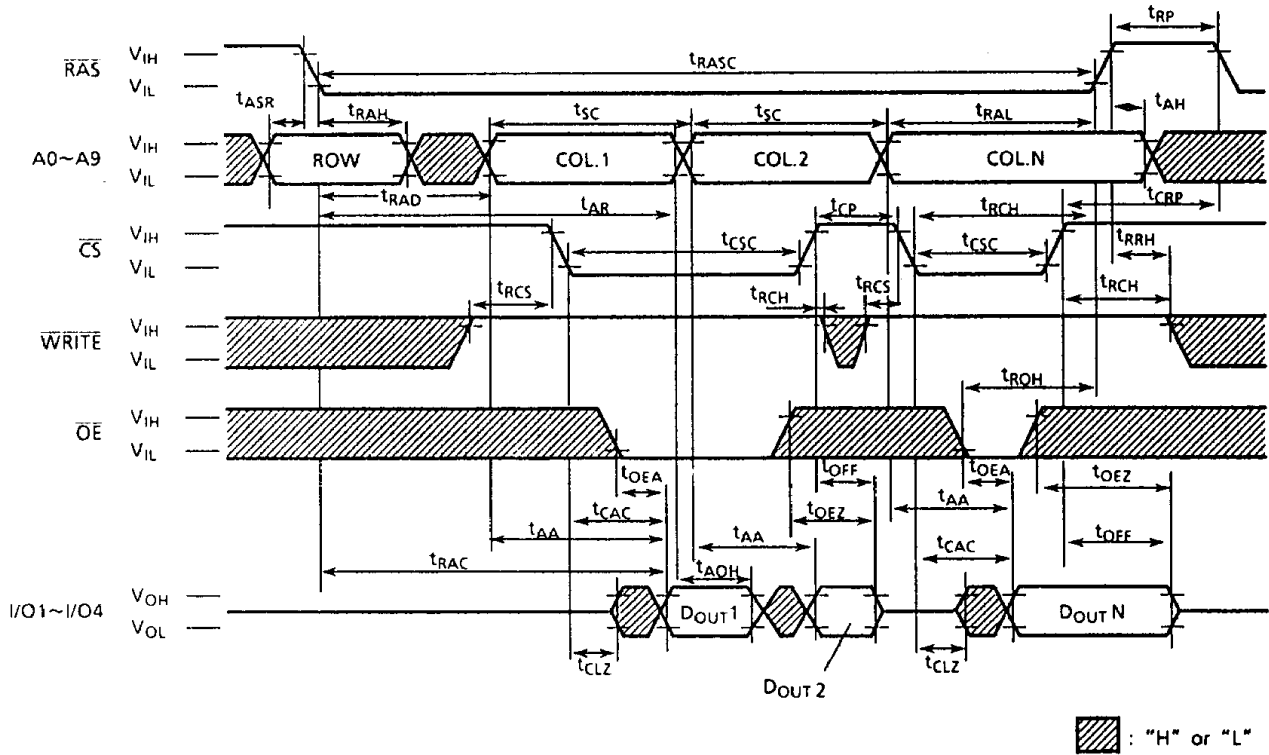
WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)



READ - MODIFY - WRITE CYCLE

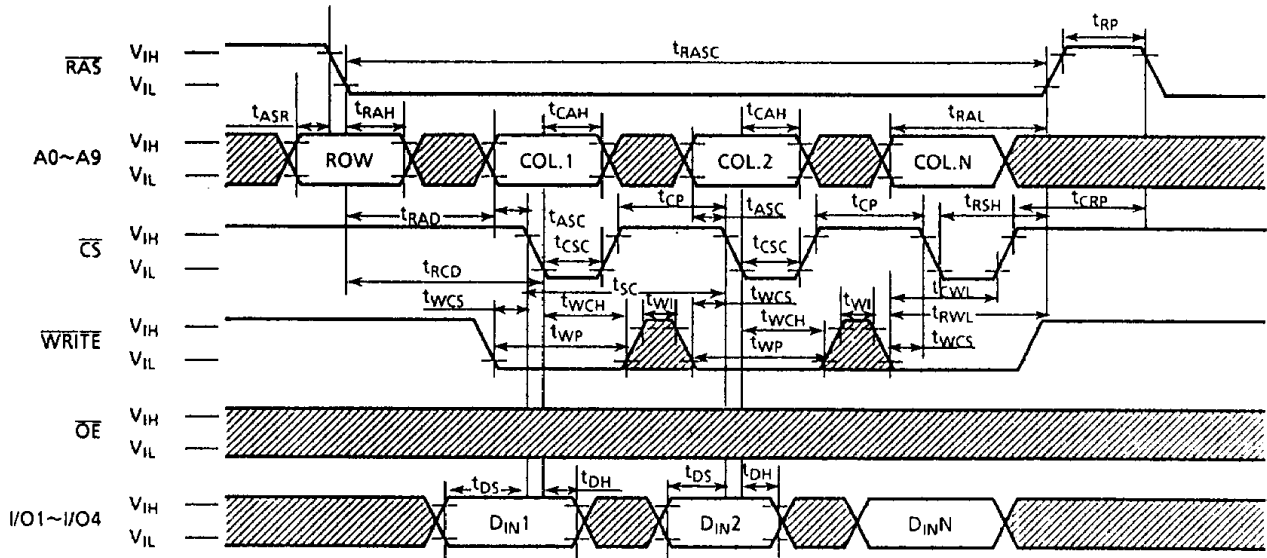


STATIC COLUMN MODE READ CYCLE

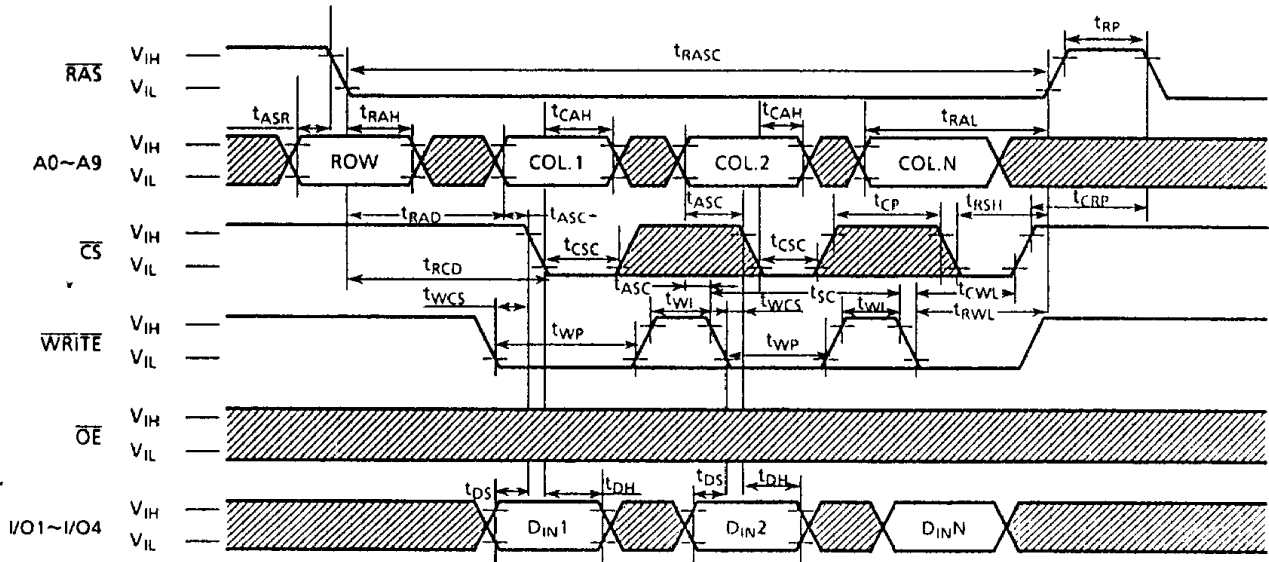


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STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)

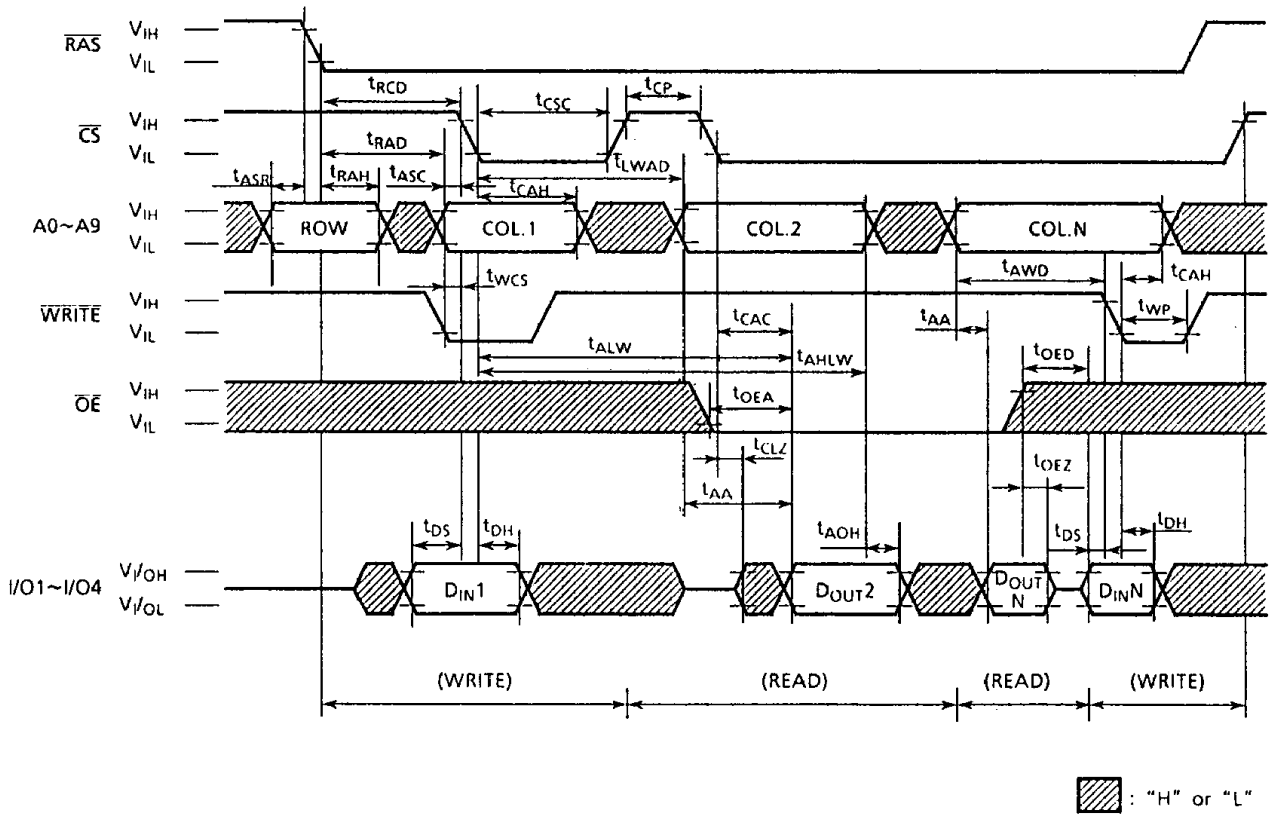


STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)

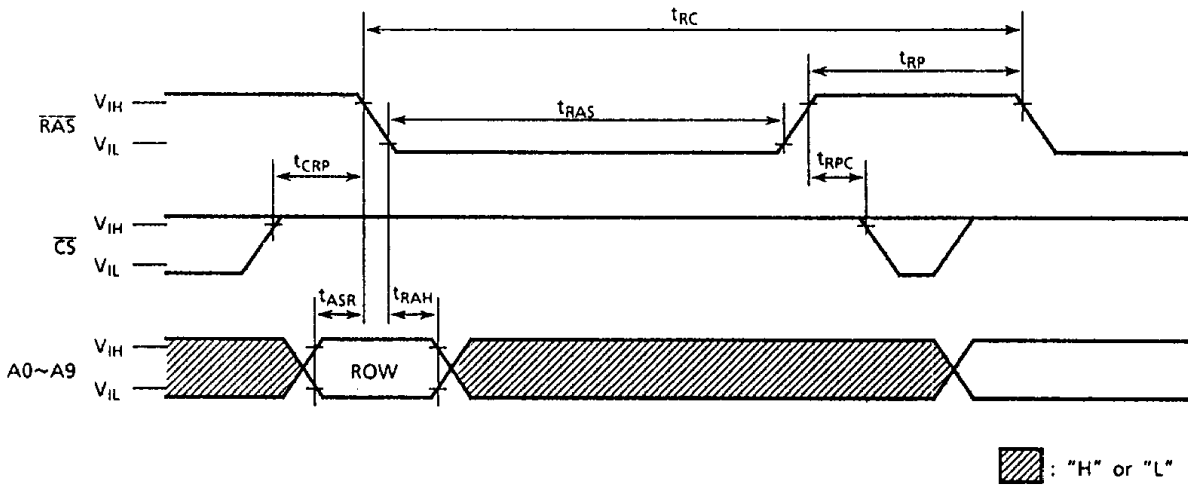


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STATIC COLUMN MODE READ/WRITE MIXED CYCLE



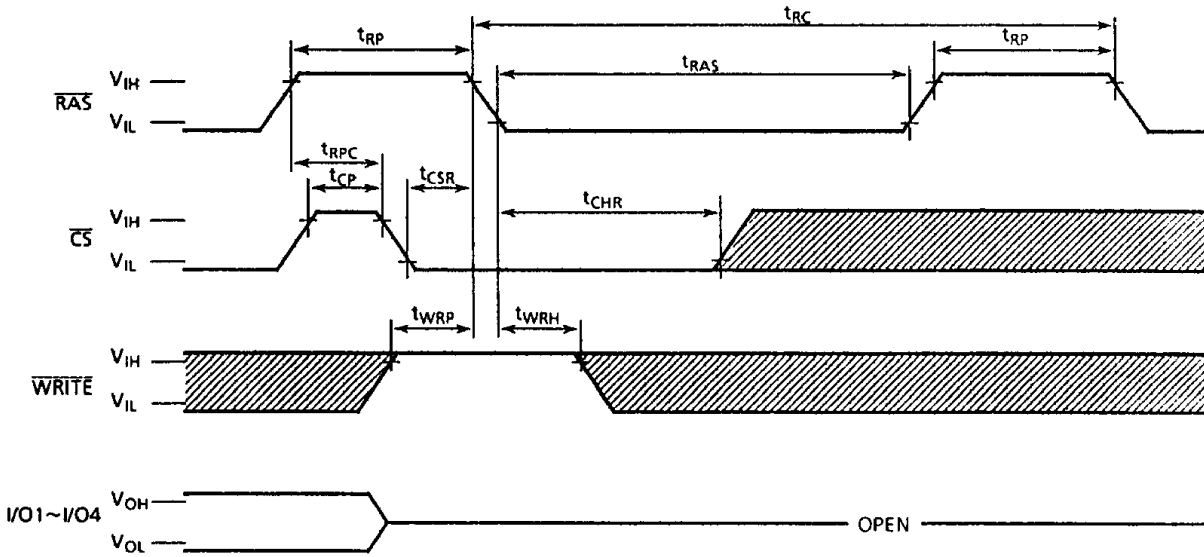
RAS ONLY REFRESH CYCLE




Note: WRITE, \overline{OE} = "H" or "L"

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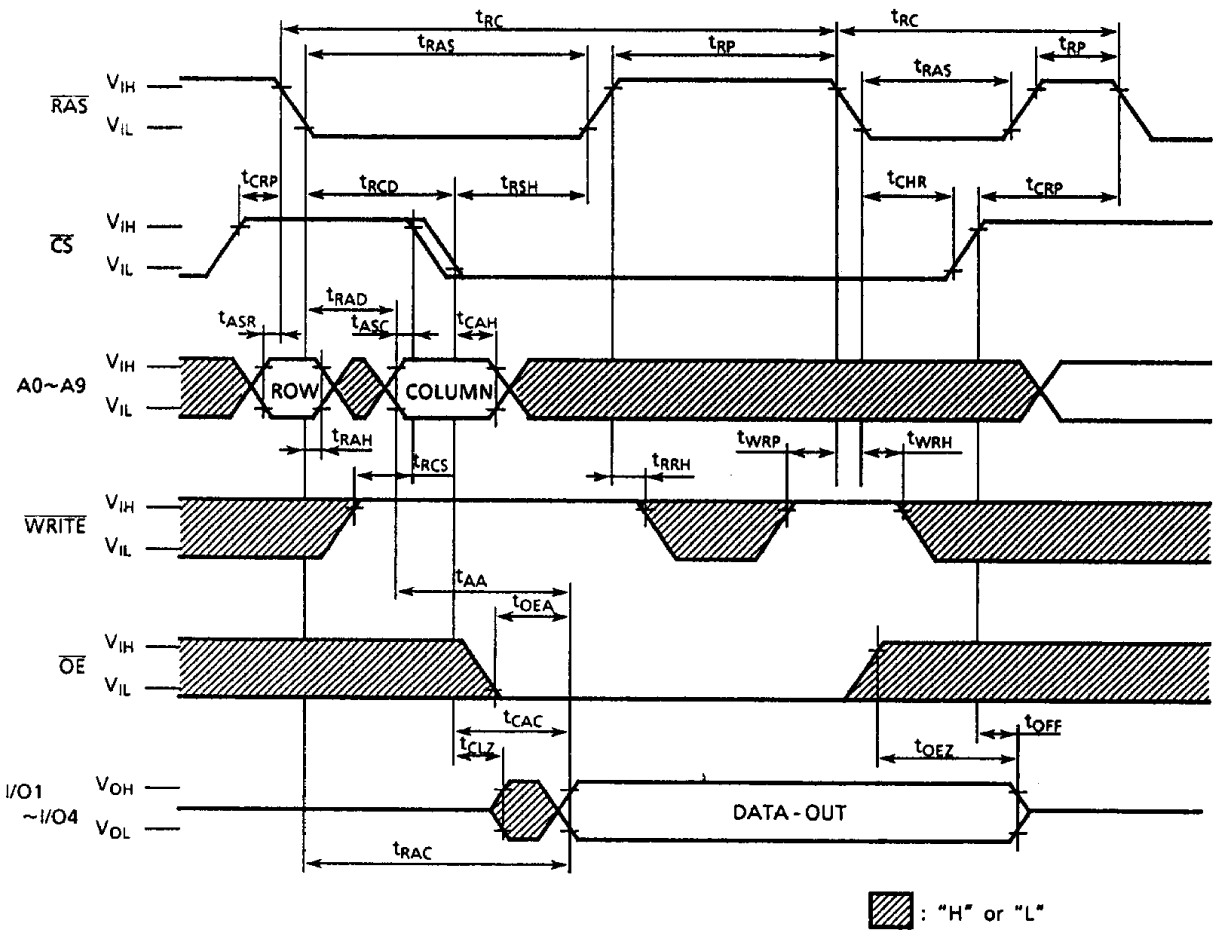
CS BEFORE RAS REFRESH CYCLE



Note: \overline{OE} , A0~A9 = "H" or "L"

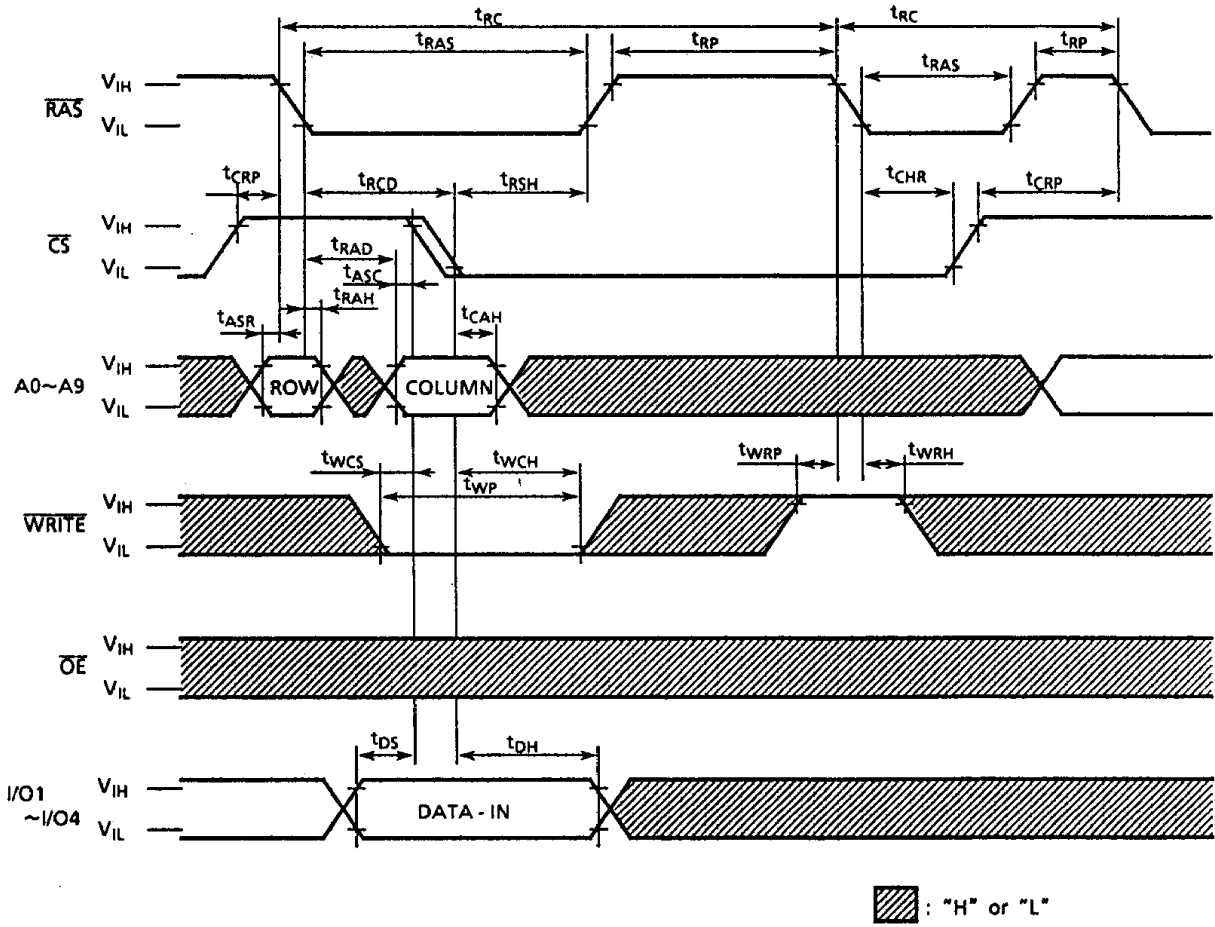
 : "H" or "L"

HIDDEN REFRESH CYCLE (READ)



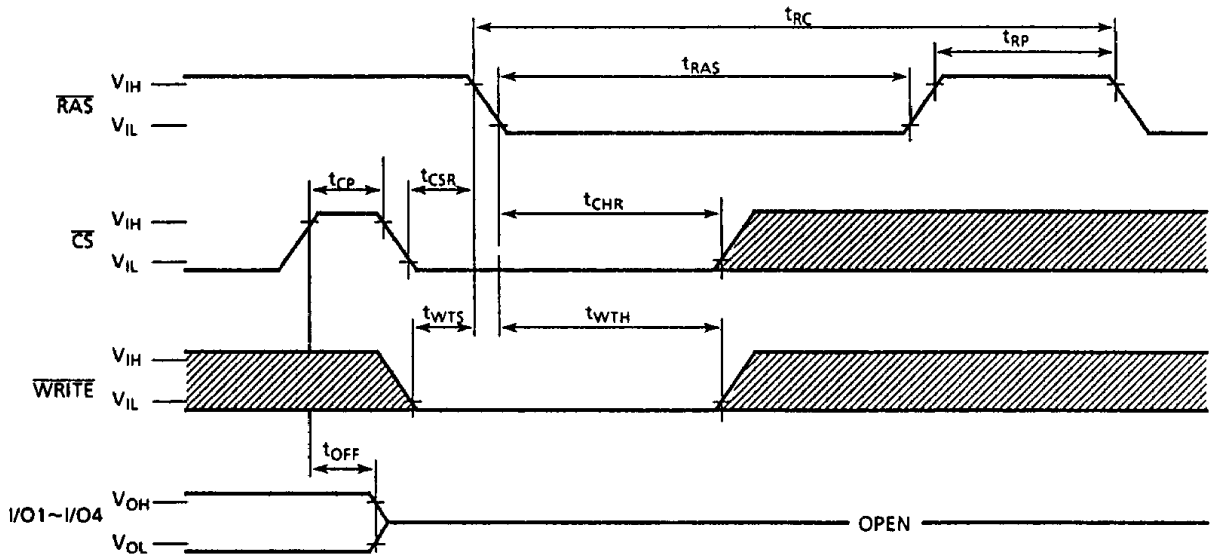
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HIDDEN REFRESH CYCLE (WRITE)



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WRITE, CS BEFORE RAS REFRESH CYCLE



**TC514402AP/AJ/ASJ/AZ-70, TC514402AP/AJ/ASJ/AZ-80
TC514402AP/AJ/ASJ/AZ-10**

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1~7	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

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BLOCK DIAGRAM IN THE TEST MODE

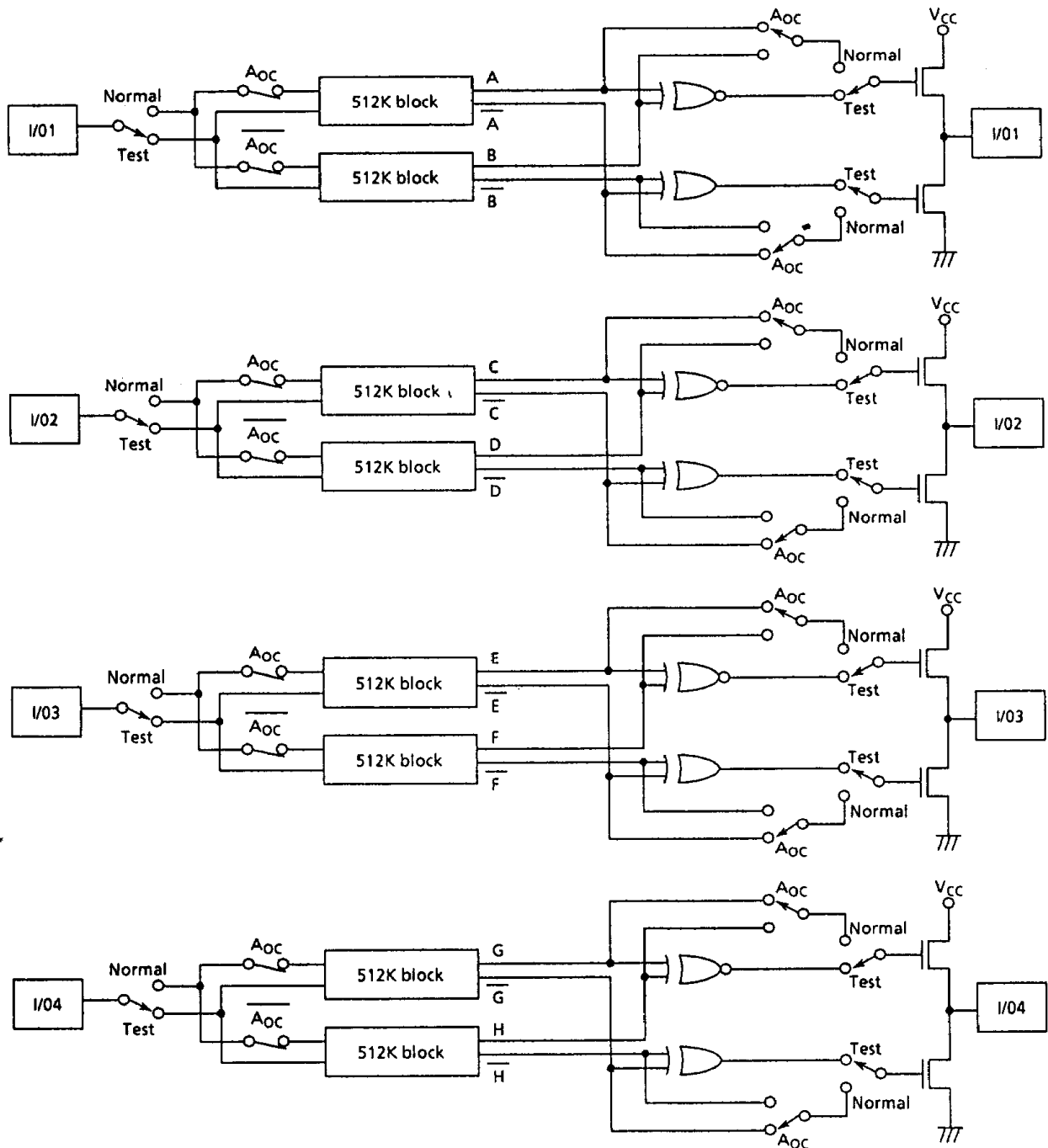


Fig. 1