

Six Pair N- and P-Channel Enhancement-Mode MOSFET

Features

- Six N- and P-channel MOSFET pairs
- Integrated gate-source resistor
- Integrated gate-source zener diode
- Low threshold
- Low on-resistance
- Low input capacitance
- Fast switching speeds
- Free from secondary breakdowns
- Low input and output leakage

Application

- High voltage pulsers
- Amplifiers
- Buffers
- Piezoelectric transducer drivers
- General purpose line drivers
- Logic level interfaces

General Description

The Supertex TC7320FG consists of a six pairs of high voltage low threshold N-channel and P-channel MOSFETs in a 32-lead LQFP package. All the MOSFETs have integrated gate-source resistors and gate-source zener diode clamps which are desired for high voltage pulser applications. These low threshold enhancement-mode (normally-off) transistors utilize an advanced lateral DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex's lateral DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Absolute Maximum Ratings*

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6mm from case for 10 seconds.

Ordering Information

Order Number / Package	BV_{DSS} / BV_{DGS}		$R_{DS(ON)}$ (max)	
	N-Channel	P-Channel	N-Channel	P-Channel
TC7320FG	200V	-200V	20Ω	20Ω
TC7320FG-G*	200V	-200V	20Ω	20Ω

**"Green" certified package



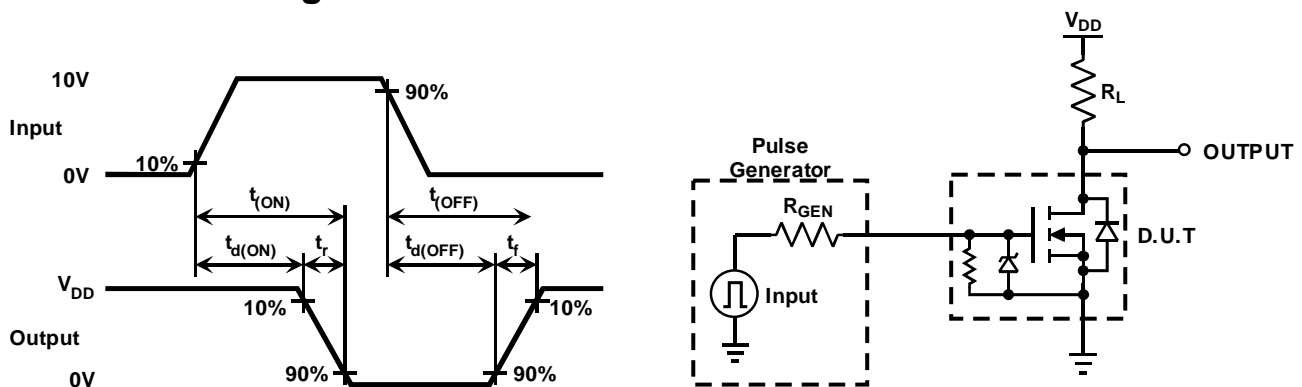
N-Channel Electrical Characteristics (at $T_A=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200			V	$V_{GS}=0V, I_D=1mA$
$V_{GS(th)}$	Gate Threshold Voltage		0.4		V	$V_{GS}=V_{DS}, I_D=1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.5	mV/°C	$V_{GS}=V_{DS}, I_D=1mA$
R_{GS}	Gate-Source Shunt Resistor	0.9		8.0	K Ω	$I_{GS}=100\mu A$
ΔR_{GS}	Change in R_{GS} with Temperature			TBD	%/°C	$I_{GS}=100\mu A$
V_{ZGS}	Gate-Source Zener Voltage	10		18	V	$I_{GS}=2.0mA$
ΔV_{ZGS}	Change in V_{ZGS} with Temperature			TBD	mV/°C	$I_{GS}=2.0mA$
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	$V_{GS}=0V, V_{DS}=\text{Max Rating}$
				1.0	mA	$V_{GS}=0V, V_{DS}=0.8 \text{ Max Rating}, T_A=125^\circ\text{C}$
$I_{D(ON)}$	On-State Drain Current	1.0			A	$V_{GS}=10V, V_{DS}=25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			20	Ω	$V_{GS}=10V, I_D=150mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.0	%/°C	$V_{GS}=10V, I_D=150mA$
G_{FS}	Forward Transconductance		150		mmho	$V_{DS}=25V, I_D=200mA$
C_{ISS}	Input Capacitance			150	pF	$V_{GS}=0V, V_{DS}=25V$ $f=1MHz$
C_{OSS}	Common Source Output Capacitance			75		
C_{RSS}	Reverse Transfer Capacitance			25		
$t_{d(ON)}$	Turn-ON Delay Time			12	ns	$V_{DD}=25V,$ $I_D=500mA$ $R_{GEN}=25\Omega$
t_r	Rise Time			15		
$t_{d(OFF)}$	Turn-Off Delay Time			25		
t_f	Fall Time			40		
V_{SD}	Diode Forward Voltage Drop			1.8	V	$V_{GS}=0V, I_{SD}=0.5A$
t_{rr}	Reverse Recovery Time		300		ns	$V_{GS}=0V, I_{SD}=0.5A$

Notes:

- 1) All DC parameters 100% tested at 25°C unless otherwise stated. (Pulsed test: 300 μs pulse at 2% duty cycle.)
- 2) All AC parameters sample tested.

N-Channel Switching Waveforms and Test Circuit



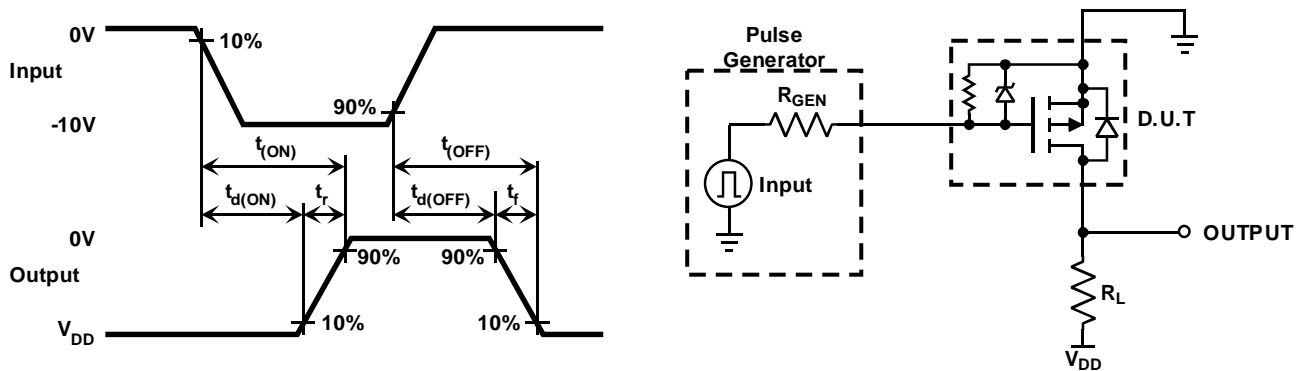
P-Channel Electrical Characteristics (at $T_A=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-200			V	$V_{GS}=0V, I_D=-1mA$
$V_{GS(th)}$	Gate Threshold Voltage		-2.3		V	$V_{GS}=V_{DS}, I_D=-1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			4.5	mV/°C	$V_{GS}=V_{DS}, I_D=-1mA$
R_{GS}	Gate-Source Shunt Resistor	0.9		8.0	K Ω	$I_{GS}=-100\mu A$
ΔR_{GS}	Change in R_{GS} with Temperature			TBD	%/°C	$I_{GS}=-100\mu A$
V_{ZGS}	Gate-Source Zener Voltage	10		18	V	$I_{GS}=-2.0mA$
$\Delta V_{ZGS(th)}$	Change in V_{ZGS} with Temperature			TBD	mV/°C	$I_{GS}=-2.0mA$
I_{DSS}	Zero Gate Voltage Drain Current			-10	μA	$V_{GS}=0V, V_{DS}=\text{Max Rating}$
				-1.0	mA	$V_{GS}=0V, V_{DS}=0.8 \text{ Max Rating}, T_A=125^\circ\text{C}$
$I_{D(ON)}$	On-State Drain Current	-1.0			A	$V_{GS}=-10V, V_{DS}=-25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			20	Ω	$V_{GS}=-10V, I_D=-150mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.0	%/°C	$V_{GS}=-10V, I_D=-150mA$
G_{FS}	Forward Transconductance		150		mmho	$V_{DS}=-25V, I_D=-200mA$
C_{ISS}	Input Capacitance			200	pF	$V_{GS}=0V, V_{DS}=-25V$ $f=1MHz$
C_{OSS}	Common Source Output Capacitance			100		
C_{RSS}	Reverse Transfer Capacitance			35		
$t_{d(ON)}$	Turn-ON Delay Time			15	ns	$V_{DD}=-25V,$ $I_D=-500mA$ $R_{GEN}=25\ \Omega$
t_r	Rise Time			20		
$t_{d(OFF)}$	Turn-Off Delay Time			35		
t_f	Fall Time			30		
V_{SD}	Diode Forward Voltage Drop			-1.8	V	$V_{GS}=0V, I_{SD}=-0.5A$
t_{rr}	Reverse Recovery Time		300		ns	$V_{GS}=0V, I_{SD}=-0.5A$

Notes:

- 1) All DC parameters 100% tested at 25°C unless otherwise stated. (Pulsed test: 300 μs pulse at 2% duty cycle.)
- 2) All AC parameters sample tested.

P-Channel Switching Waveforms and Test Circuit



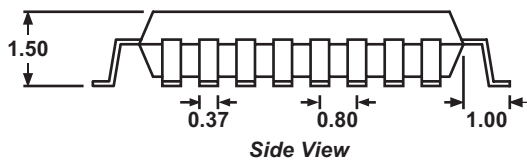
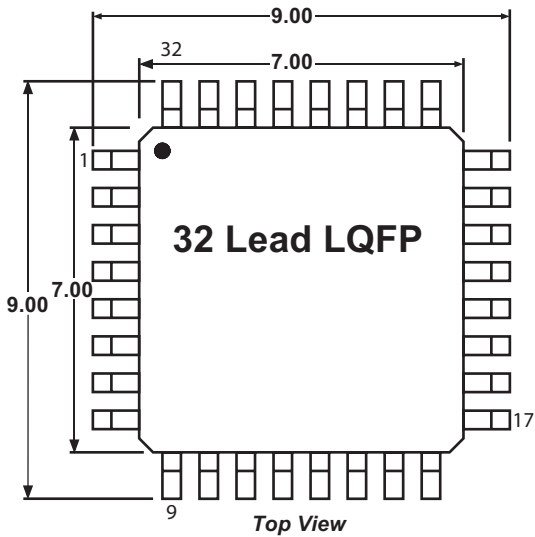
Pin Configuration

Pin	Function	Pin	Function
1	GP1	17	DN6
2	GN1	18	DN3
3	GN2	19	DN5
4	GN3	20	N/C
5	GN6	21	V _{NN2}
6	GN5	22	DN2
7	GN4	23	DN4
8	GP4	24	DN1
9	GP5	25	V _{NN1}
10	GP6	26	V _{PP1}
11	DP6	27	DP1
12	V _{PP2}	28	DP2
13	DP5	29	V _{PP3}
14	DP4	30	DP3
15	V _{SUB}	31	GP3
16	V _{NN3}	32	GP2

The V_{SUB} pin needs to be connected to the most positive supply

32 Lead Low Quad Flat Pack (LQFP)* Package Outline

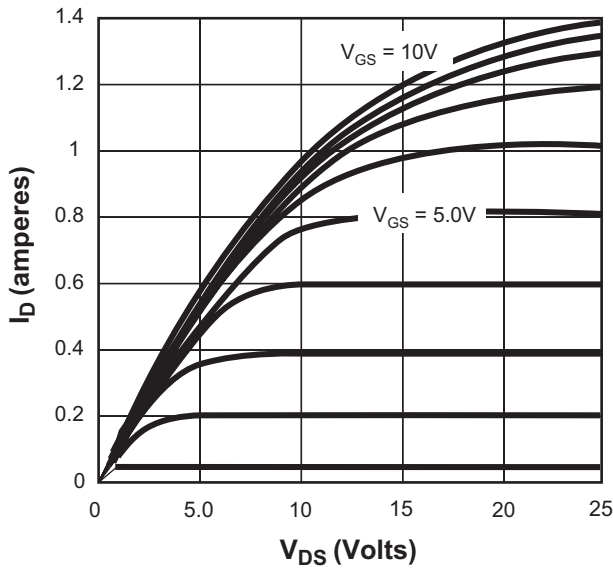
All dimensions are in millimeters



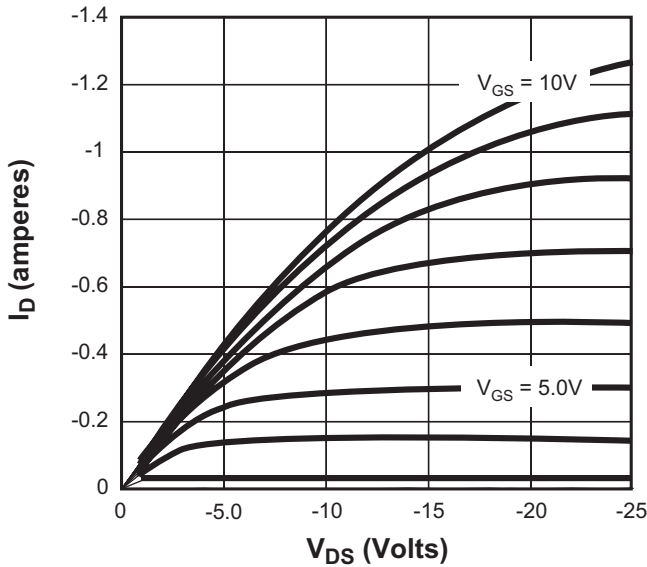
**Green* certified package

Typical I-V Characteristics

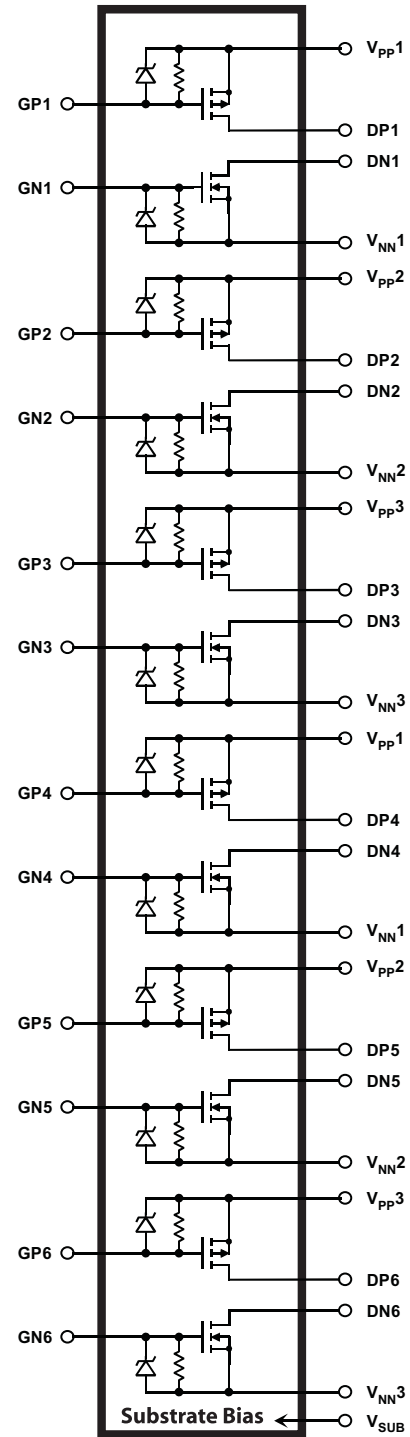
N-Channel



P-Channel



Block Diagram



Supertex Inc. does not recommend the use of its products in life support applications and will not knowingly sell its products for use in such applications unless it receives an adequate "products liability indemnification insurance agreement." Supertex does not assume responsibility for use of devices described and limits its liability to the replacement of devices determined to be defective due to workmanship. No responsibility is assumed for possible omissions or inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications, refer to the Supertex website: <http://www.supertex.com>. For complete liability information on all Supertex products, refer to the most current databook or to the Legal/Disclaimer page on the Supertex website.