TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

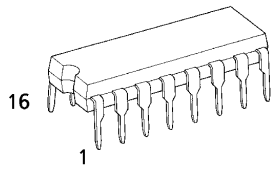
TC74HC592AP, TC74HC592AF

8 – BIT BINARY COUNTER WITH INPUT REGISTER

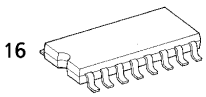
The TC74HC592A is high speed CMOS 8-BIT REGISTER COUNTER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaing the CMOS low power dissipation.
The internal counter counts at positive edge of Counter Clock (CCK) when Counter Clock Enable ($\overline{CCKEN}$) is held "L" level. If Counter clear ($\overline{CCLR}$) is held "L", the internal counter is cleared asynchronously to clock.
Input A~H are loaded to register at positive edge of Register Clock (RCK), and the register outputs are loaded to Counter when Counter Load ($\overline{CLOAD}$) is held "L" level.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX} = 35MHz(typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr.) = 2V~6V
- Pin and Function Compatible with 74LS592

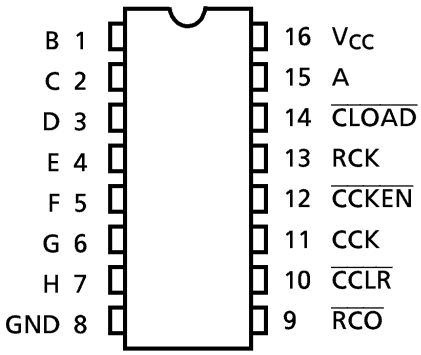


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

INPUT					FUNCTION
RCK	$\overline{CLOAD}$	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
X	L	H	X	X	REGISTER DATA IS LOADED INTO COUNTER
X	H	L	X	X	COUNTER CLEAR
↑	H	H	X	X	THE DATA OF A THRU H INPUTS IS STORED INTO REGISTER
↓	H	H	X	X	REGISTER STATE IS NOT CHANGED
X	H	H	L	↑	COUNTER ADVANCES THE COUNT
X	H	H	L	↓	NO COUNT
X	H	H	H	X	NO COUNT

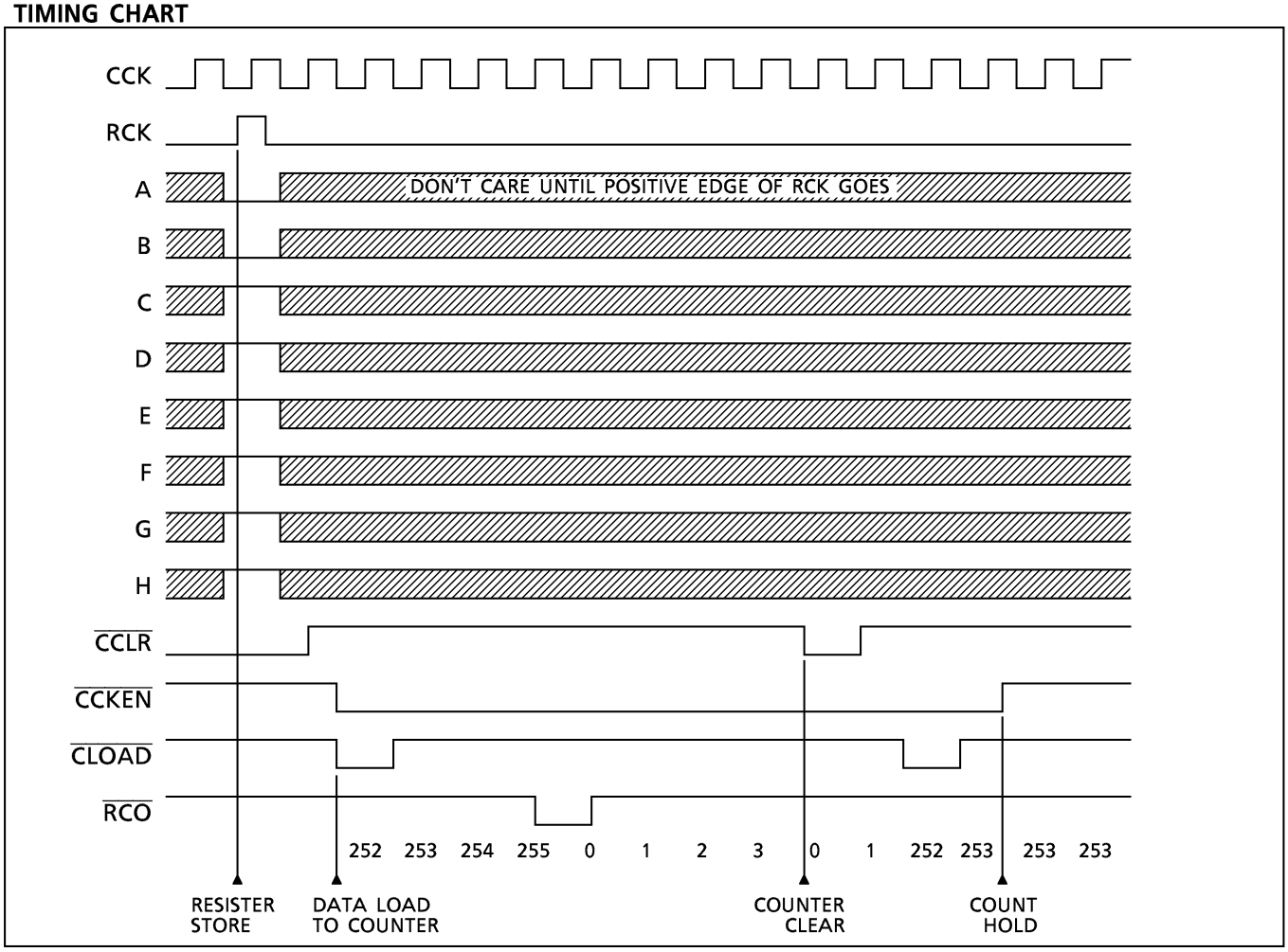
X : Don't care

$\overline{RCO} = \overline{QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH'}$

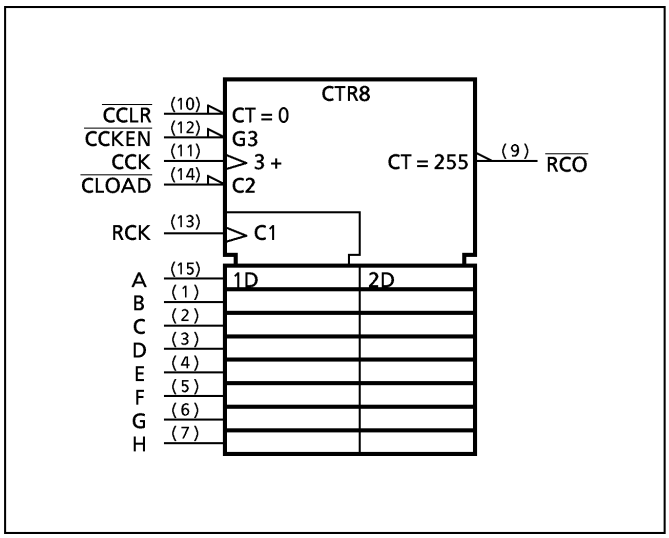
(QA'~QH' : Internal outputs of the counter)

980508EBA2

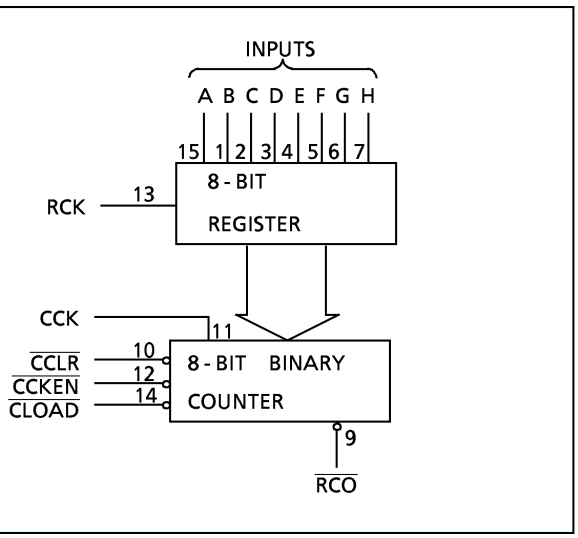
TIMING CHART



IEC LOGIC CHART

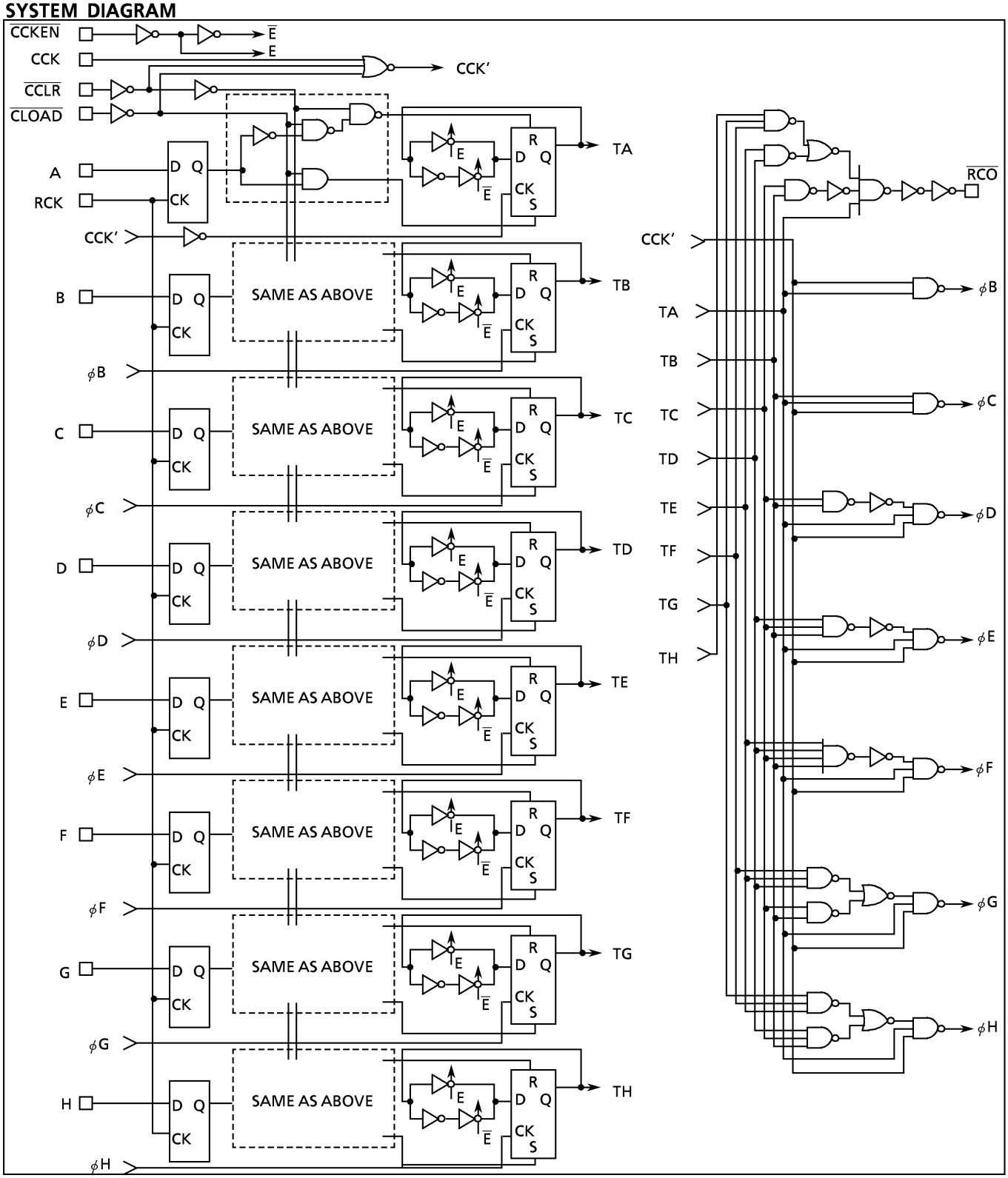


BLOCK DIAGRAM



980508EBA2'

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta= −40°C~65°C. From Ta=65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~ 1000 (V_{CC} = 2.0V) 0~ 500 (V_{CC} = 4.5V) 0~ 400 (V_{CC} = 6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
			I_{OH} = −4 mA I_{OH} = −5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		Ta = −40~85°C	UNIT
			V_{CC} (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CCK, RCK)	$t_{W(H)}$ $t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width ($\overline{CCLR}$)	$t_{W(L)}$		2.0	—	100	125	
			4.5	—	20	25	
			6.0	—	16	21	
Minimum Pulse Width ($\overline{CLOAD}$)	$t_{W(L)}$		2.0	—	175	220	
			4.5	—	35	44	
			6.0	—	30	37	
Minimum Set−up Time ($\overline{CCKEN}$ − CCK)	t_s		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set−up Time (RCK − $\overline{CLOAD}$)	t_s		2.0	—	150	190	
			4.5	—	30	38	
			6.0	—	26	32	
Minimum Set−up Time (A~H − RCK)	t_s		2.0	—	100	125	
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Hold Time	t_h		2.0	—	5	5	
			4.5	—	5	5	
			6.0	—	5	5	
Minimum Removal Time ($\overline{CCLR}$)	t_{rem}		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Removal Time ($\overline{CLOAD}$)	t_{rem}		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Clock Frequency	f		2.0	—	4	3.5	MHz
			4.5	—	22	18	
			6.0	—	26	21	

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	6	12	ns
Propagation Delay Time (CCK − $\overline{RCO}$)	t_{pLH} t_{pHL}		—	25	38	
Propagation Delay Time (RCK − $\overline{RCO}$)	t_{pLH} t_{pHL}		—	39	60	
Propagation Delay Time ($\overline{CCLR}$ − $\overline{RCO}$)	t_{pLH}		—	24	36	
Propagation Delay Time ($\overline{CLOAD}$ − $\overline{RCO}$)	t_{pLH} t_{pHL}		—	35	53	
Maximum Clock Frequency	f_{MAX}		25	35	—	MHz

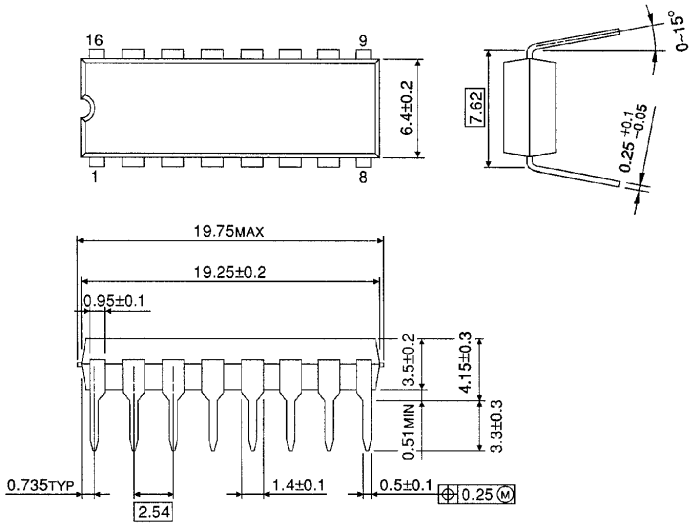
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation Delay Time (CCK − $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	—	94	220	—	275	
			4.5	—	29	44	—	55	
			6.0	—	24	37	—	47	
Propagation Delay Time (RCK − $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	—	160	340	—	425	
			4.5	—	45	68	—	85	
			6.0	—	34	58	—	73	
Propagation Delay Time ($\overline{CCLR}$ − $\overline{RCO}$)	t_{pLH}		2.0	—	89	215	—	270	
			4.5	—	28	43	—	54	
			6.0	—	22	37	—	46	
Propagation Delay Time ($\overline{CLOAD}$ − $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	—	140	300	—	375	
			4.5	—	40	60	—	75	
			6.0	—	30	51	—	64	
Maximum Clock Frequency	f_{MAX}		2.0	4	20	—	3.5	—	MHz
			4.5	22	33	—	18	—	
			6.0	26	49	—	21	—	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} (1)			—	31	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

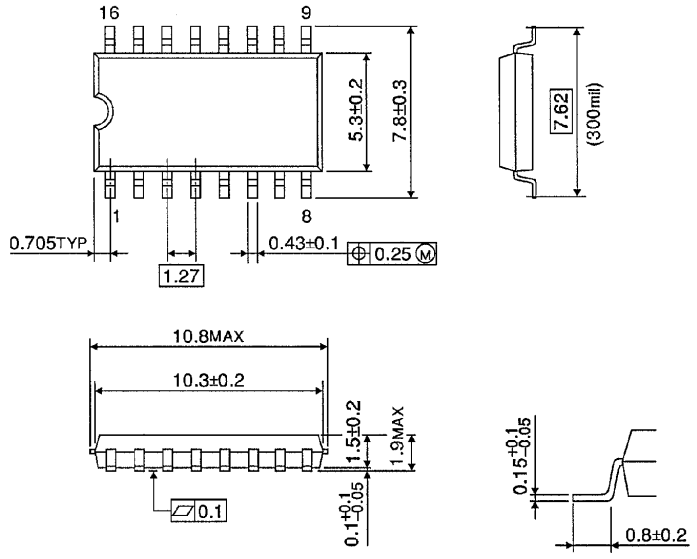
$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)