

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC74VHC123AF, TC74VHC123AFN, TC74VHC123AFT**  
**TC74VHC221AF, TC74VHC221AFN, TC74VHC221AFT**

**DUAL MONOSTABLE MULTIVIBRATOR**  
**TC74VHC123AF / AFN / AFT RETRIGGERBLE**  
**TC74VHC221AF / AFN / AFT NON - RETRIGGERBLE**

(Note) : The JEDEC SOP (FN) is not available in Japan.

The TC74VHC123A / 221A are high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C<sup>2</sup>MOS technology.

There are two trigger inputs,  $\overline{A}$  input (Negative edge), and B input (Positive edge). These inputs are valid for a slow rise/fall time signal ( $t_r = t_f = 1$  s) as they are schmitt trigger inputs. This device may also be triggered by using  $\overline{CLR}$  input (Positive edge).

After triggering, the output stays in a MONOSTABLE state for a time period determined by the external resistor and capacitor ( $R_x, C_x$ ). A low level at the  $\overline{CLR}$  input breaks this state.

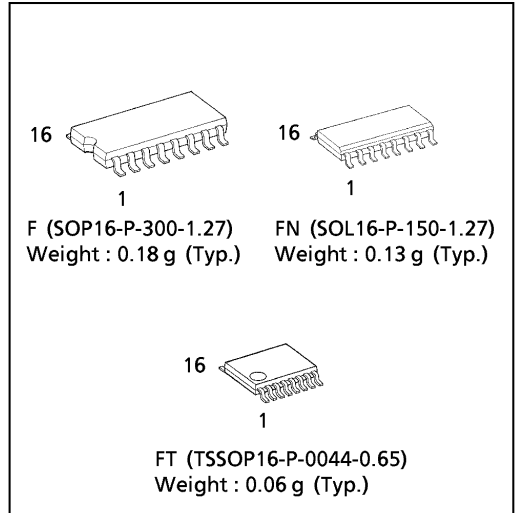
Limits for  $C_x$  and  $R_x$  are :

- External capacitor,  $C_x$  ..... No limit
- External resistor,  $R_x$  .....  $V_{CC} = 2.0$  V more than  $5\text{ k}\Omega$   
 $V_{CC} \geq 3.0$  V more than  $1\text{ k}\Omega$

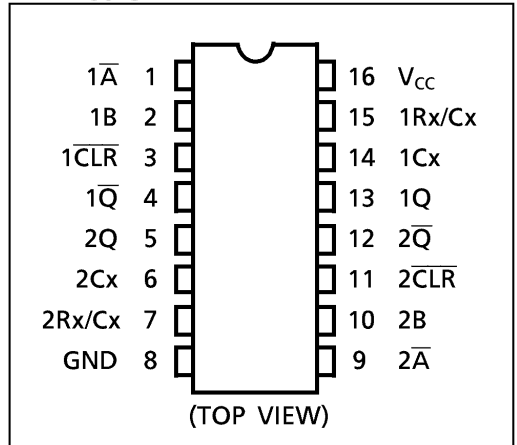
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

**FEATURES :**

- High Speed.....  $t_{pd} = 8.1$  ns (typ.) at  $V_{CC} = 5$  V
- Low Power Dissipation
  - Standby State.....  $4\ \mu\text{A}$  (Max.) at  $T_a = 25^\circ\text{C}$
  - Active State.....  $600\ \mu\text{A}$  (Max.) at  $T_a = 25^\circ\text{C}$
- High Noise Immunity.....  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (Min.)
- Power Down Protection is equipped with all inputs.
- Balanced Propagation Delays .....  $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range....  $V_{CC}$  (opr) = 2 V~5.5 V
- Pin and Function Compatible with 74HC123A / 221A



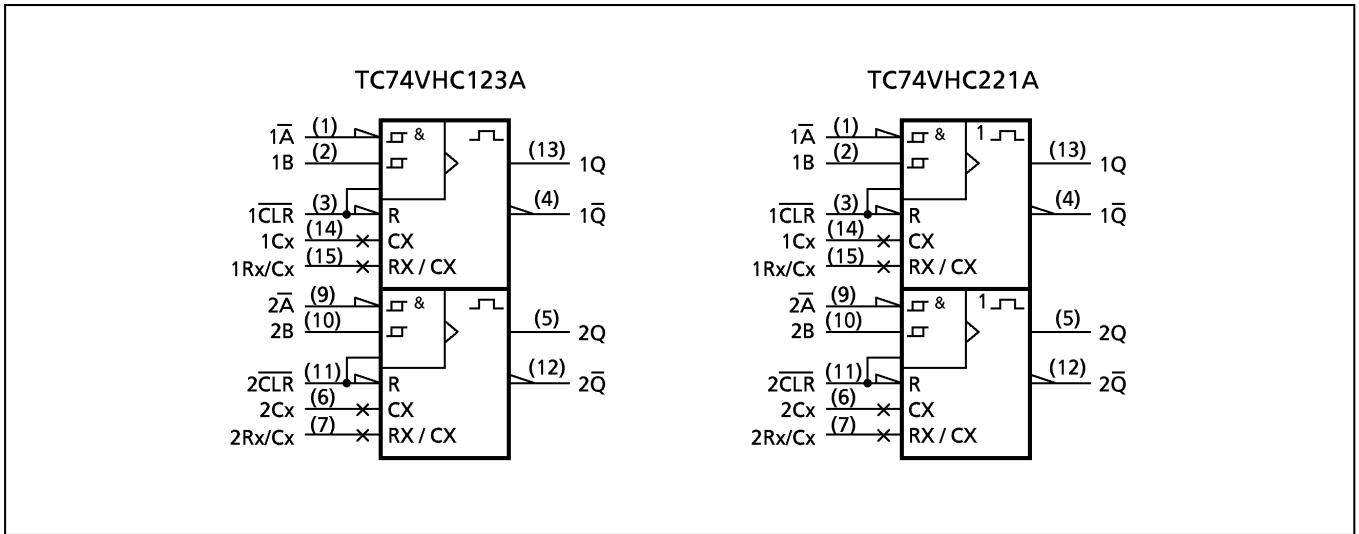
**PIN ASSIGNMENT**



980910EBA2

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**IEC LOGIC SYMBOL**



**TRUTH TABLE**

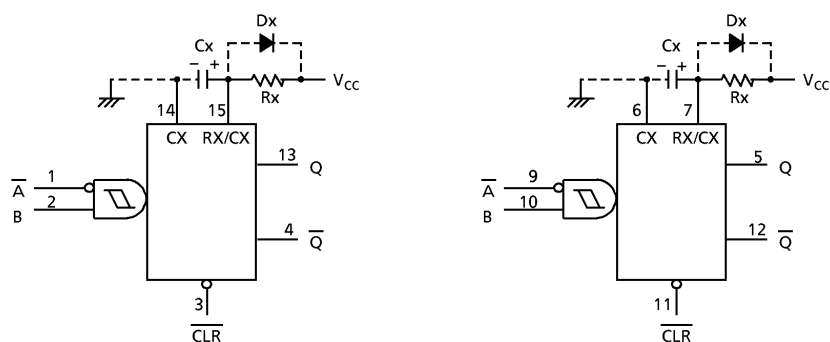
INPUTS			OUTPUTS		FUNCTION
A	B	CLR	Q	Q-bar	
	H	H			OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L		H			OUTPUT ENABLE
L	H				OUTPUT ENABLE
X	X	L	L	H	RESET

X : Don't Care

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## BLOCK DIAGRAM



Notes : (1) Cx, Rx, Dx are external  
Capacitor, Resistor, and Diode, respectively.

(2) External clamping diode, Dx ;

The external capacitor is charged to  $V_{CC}$  level in the wait state, i.e. when no trigger is applied.

If the supply voltage is turned off, Cx is discharged mainly through the internal (parasitic) diode. If Cx is sufficiently large and  $V_{CC}$  drops rapidly, there will be some possibility of damaging the IC through inrush current or latch-up. If the capacitance of the supply voltage filter is large enough and  $V_{CC}$  drops slowly, the inrush current is automatically limited and damage to the IC is avoided.

The maximum value of forward current through the parasitic diode is  $\pm 20$  mA.

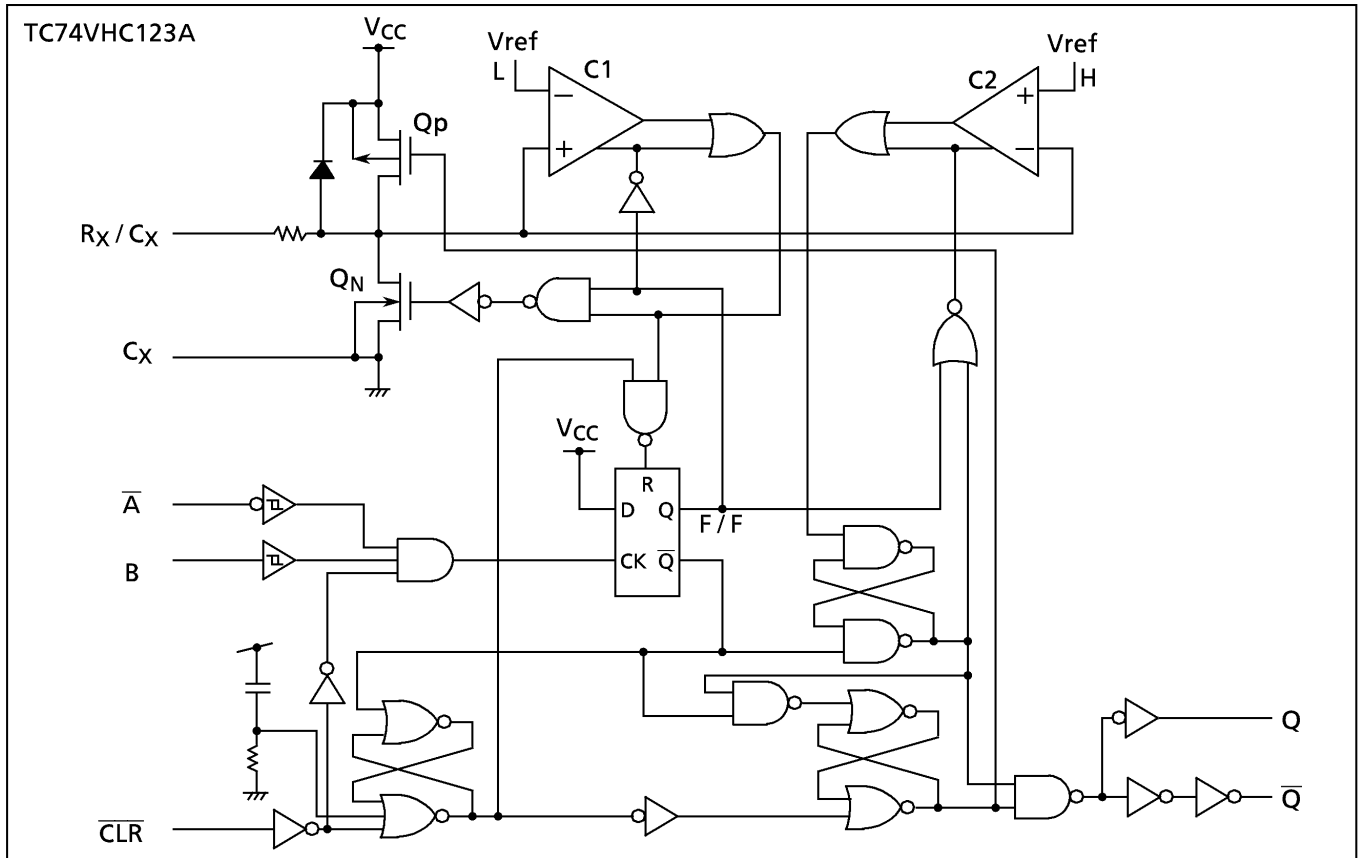
In the case of a large Cx, the limit of fall time of the supply voltage is determined as follows:

$$t_f \geq (V_{CC} - 0.7) \cdot C_x / 20 \text{ mA}$$

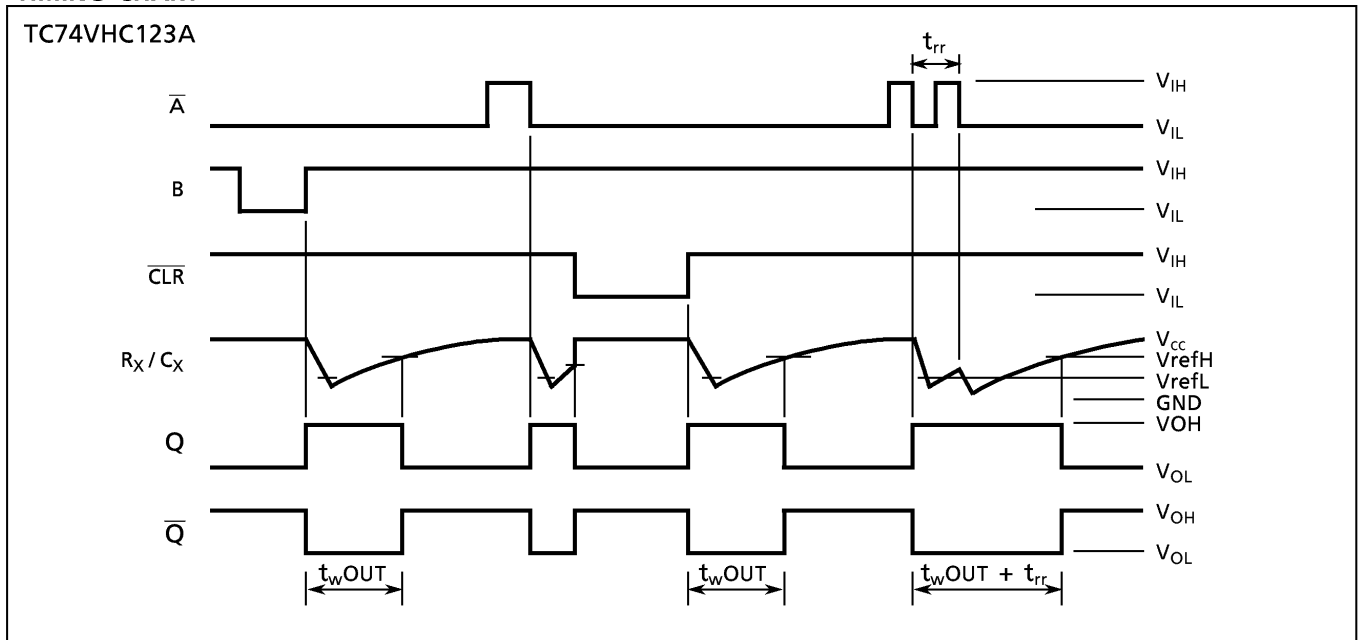
( $t_f$  is the time between the supply voltage turn off  
and the supply voltage reaching  $0.4 V_{CC}$ .)

In the even a system does not satisfy the above condition, an external clamping diode (Dx) is needed to protect the IC from rush current.

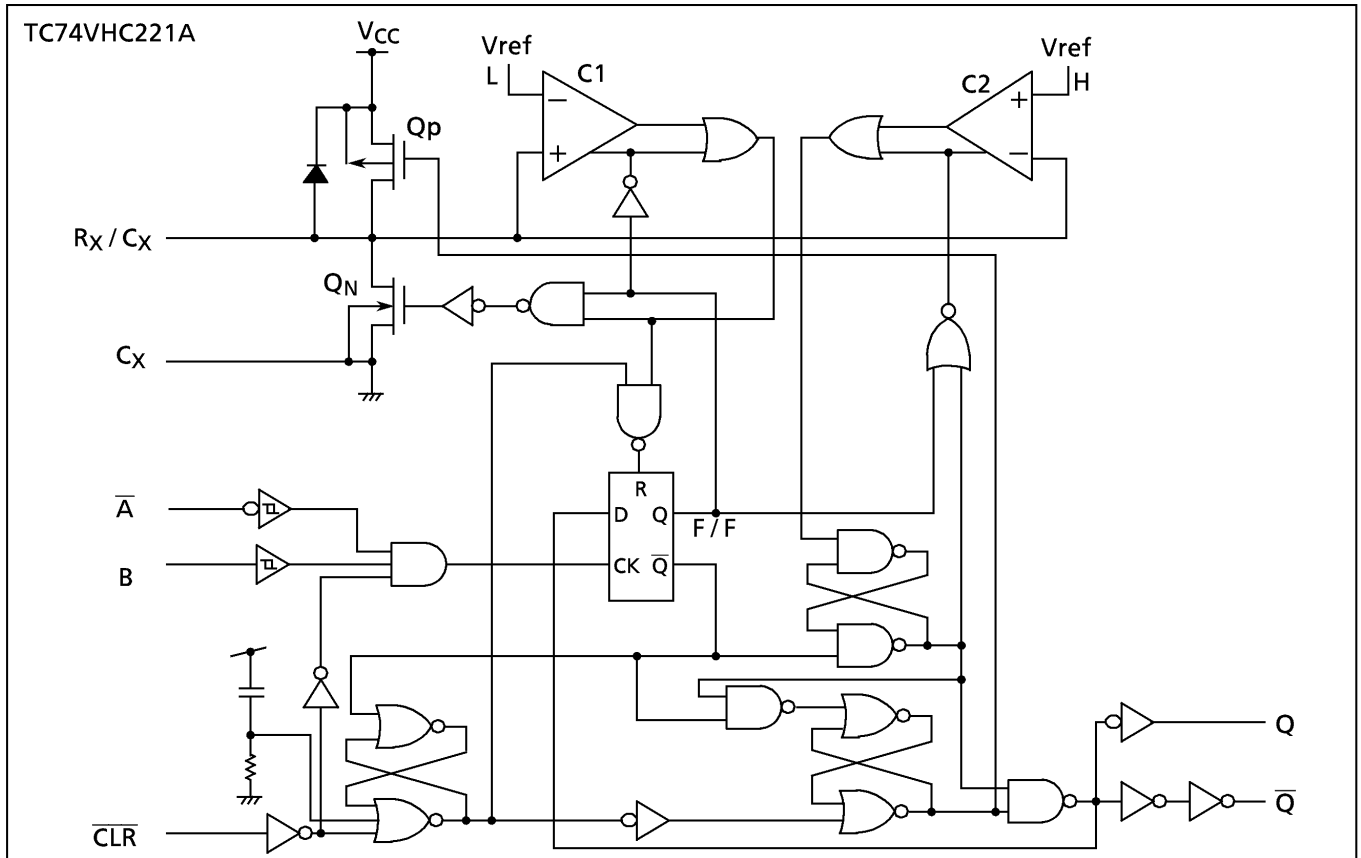
**SYSTEM DIAGRAM**



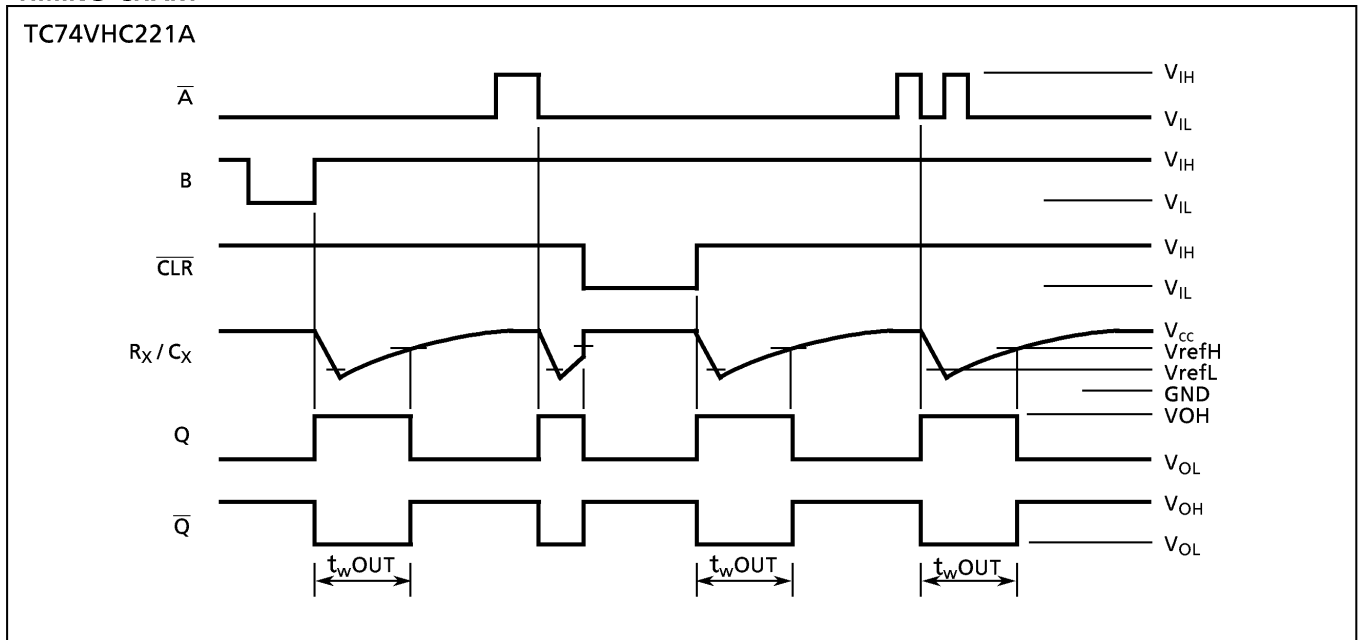
**TIMING CHART**



**SYSTEM DIAGRAM**



**TIMING CHART**



## FUNCTIONAL DESCRIPTION

## (1)Stand-by State

The external capacitor (Cx) is fully charged to  $V_{CC}$  in the stand-by state. That means, before triggering, the  $Q_P$  and  $Q_N$  transistors which are connected to the Rx/Cx node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

## (2)Trigger operation

Trigger operation is effective in any of the following three cases. First, the condition where the  $\overline{A}$  input is low, and the B input has a rising signal; second, where the B input is high, and the  $\overline{A}$  input has a falling signal; and third, where the  $\overline{A}$  input is low and the B input is high, and the  $\overline{CLR}$  input has a rising signal.

After a trigger becomes effective, comparators C1 and C2 start operating, and  $Q_N$  is turned on. The external capacitor discharges through  $Q_N$ . The voltage level at the Rx/Cx node drops. If the Rx/Cx voltage level falls to the internal reference voltage  $V_{refL}$ , the output of C1 becomes low. The flip-flop is then reset and  $Q_N$  turns off. At that moment C1 stops but C2 continues operating.

After  $Q_N$  turns off, the voltage at the Rx/Cx node starts rising at a rate determined by the time constant of external capacitor Cx and resistor Rx.

Upon triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of Rx/Cx changes from falling to rising. When Rx/Cx reaches the internal reference voltage  $V_{refH}$ , the output of C2 becomes low, the output Q goes low and C2 stops its operation. That means, after triggering, when the voltage level of the Rx/Cx node reaches  $V_{refH}$ , the IC returns to its MONOSTABLE state.

With large values of Cx and Rx, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse,  $t_w$  (OUT), is as follows:

$$t_w(\text{OUT}) = 1.0 C_x R_x$$

## (3)Retrigger operation ( TC74VHC123A )

When a new trigger is applied to either input  $\overline{A}$  or B while in the MONOSTABLE state, it is effective only if the IC is charging Cx. The voltage level of the Rx/Cx node then falls to  $V_{refL}$  level again. Therefore the Q output stays high if the next trigger comes in before the time period set by Cx and Rx.

If the new trigger is very close to previous trigger, such as an occurrence during the discharge cycle, it will have no effect.

The minimum time for a trigger to be effective 2nd trigger,  $t_{rr}$  (Min.), depends on  $V_{CC}$  and Cx.

## (4)Reset operation

In normal operation, the  $\overline{CLR}$  input is held high. If  $\overline{CLR}$  is low, a trigger has no effect because the Q output is held low and the trigger control F/F is reset. Also,  $Q_P$  turns on and Cx is charged rapidly to  $V_{CC}$ .

This means if  $\overline{CLR}$  is set low, the IC goes into a wait state.

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current	$I_{OK}$	±20	mA
DC Output Current	$I_{OUT}$	±25	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	±50	mA
Power Dissipation	$P_D$	180	mW
Storage Temperature	$T_{stg}$	-65~150	°C

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2.0~5.5	V
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	dt/dv	0~100 ( $V_{CC} = 3.3 \pm 0.3$ V) 0~20 ( $V_{CC} = 5 \pm 0.5$ V)	ns/V
External Capacitor	$C_x$	No Limitation *	F
External Resistor	$R_x$	≥ 5 K* ( $V_{CC} = 2.0$ V) ≥ 1 K* ( $V_{CC} \geq 3.0$ V)	Ω

\* The maximum allowable values of  $C_x$  and  $R_x$  are a function of leakage of capacitor  $C_x$ , the leakage of TC74VHC123A / 221A, and leakage due to board layout and surface resistance.  
Susceptibility to externally induced noise signals may occur for  $R_x > 1$  MΩ.

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V <sub>IH</sub>			2.0 3.0~ 5.5	1.50 V <sub>CC</sub> × 0.7	— —	— —	1.50 V <sub>CC</sub> × 0.7	— —	V
Low - Level Input Voltage	V <sub>IL</sub>			2.0 3.0~ 5.5	— —	— —	0.50 V <sub>CC</sub> × 0.3	— —	0.50 V <sub>CC</sub> × 0.3	V
High - Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -8 mA	3.0 4.5	2.58 3.94	— —	— —	2.48 3.80	— —	
Low - Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 8 mA	3.0 4.5	— —	— —	0.36 0.36	— —	0.44 0.44	
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Rx / Cx Terminal Off - State Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.25	—	±2.5	
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	4.0	—	40.0	
Active - State * Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND Rx / Cx = 0.5 V <sub>CC</sub>		3.0	—	160	250	—	280	μA
				4.5	—	380	500	—	650	
				5.5	—	560	750	—	975	

\*: Per circuit

TIMING REQUIREMENTS (Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

PARAMETER	SYMBOL	TEST CONDITION		V <sub>CC</sub> (V)	Ta = 25°C		Ta = -40~85°C	UNIT
					TYP.	LIMIT	LIMIT	
Minimum Pulse Width	t <sub>W(L)</sub> t <sub>W(H)</sub>			3.3 ± 0.3	—	5.0	5.0	
				5.0 ± 0.5	—	5.0	5.0	
Minimum Clear Width (CLR)	t <sub>W(L)</sub>			3.3 ± 0.3 5.0 ± 0.5	— —	5.0 5.0	5.0 5.0	ns
Minimum Retrigger Time **	t <sub>rr</sub>	Rx = 1 kΩ Cx = 100 pF		3.3 ± 0.3 5.0 ± 0.5	60 39	— —	— —	
		Rx = 1 kΩ Cx = 0.01 μF		3.3 ± 0.3 5.0 ± 0.5	1.5 1.2	— —	— —	μs

\*\*: for TC74VHC123A only



AC ELECTRICAL CHARACTERISTICS (Input  $t_r = t_f = 3 \text{ ns}$ )

PARAMETER	SYM-BOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT		
		V <sub>CC</sub> (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.			
Propagation Delay Time (A, B - Q, $\bar{Q}$ )	$t_{pLH}$ $t_{pHL}$	3.3 ± 0.3	15	—	13.4	20.6	1.0	24.0	ns		
			50	—	15.9	24.1	1.0	27.5			
		5.0 ± 0.5	15	—	8.1	12.0	1.0	14.0			
			50	—	9.6	14.0	1.0	16.0			
Propagation Delay Time (CLR trigger - Q, $\bar{Q}$ )	$t_{pLH}$ $t_{pHL}$	3.3 ± 0.3	15	—	14.5	22.4	1.0	26.0			
			50	—	17.0	25.9	1.0	29.5			
		5.0 ± 0.5	15	—	8.7	12.9	1.0	15.0			
			50	—	10.2	14.9	1.0	17.0			
Propagation Delay Time (CLR - Q, $\bar{Q}$ )	$t_{pLH}$ $t_{pHL}$	3.3 ± 0.3	15	—	10.3	15.8	1.0	18.5			
			50	—	12.8	19.3	1.0	22.0			
		5.0 ± 0.5	15	—	6.3	9.4	1.0	11.0			
			50	—	7.8	11.4	1.0	13.0			
Output Pulse Width	$t_{wOUT}$	Cx = 28 pF Rx = 2 kΩ	3.3 ± 0.3	50	—	160	240	—	300	μs	
			5.0 ± 0.5		—	133	200	—	240		
		Cx = 0.01 μF Rx = 10 kΩ	3.3 ± 0.3	50	90	100	110	90	110		
			5.0 ± 0.5		90	100	110	90	110		
		Cx = 0.1 μF Rx = 10 kΩ	3.3 ± 0.3	50	0.9	1.0	1.1	0.9	1.1		ms
			5.0 ± 0.5		0.9	1.0	1.1	0.9	1.1		
Output Pulse Width Error Between Circuits (In same Package)	$\Delta t_{wOUT}$				—	± 1	—	—	—	%	
Input Capacitance	C <sub>IN</sub>					4	10	—	10	pF	
Power Dissipation Capacitance	C <sub>PD</sub>	(Note 1)			—	73	—	—	—		

(Note 1) : C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

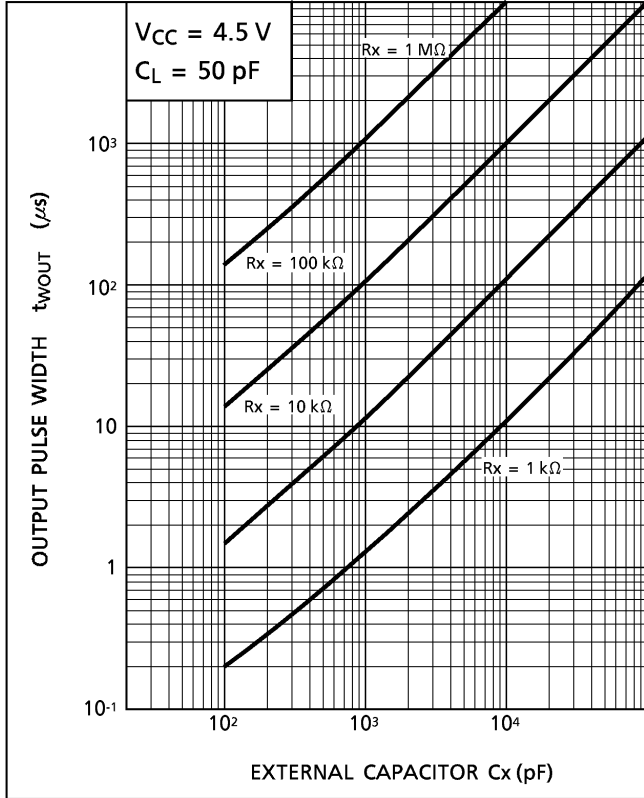
Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot \text{Duty} / 100 + I_{CC} / 2 \text{ (per circuit)}$$

(I<sub>CC</sub>' : Active Supply Current)

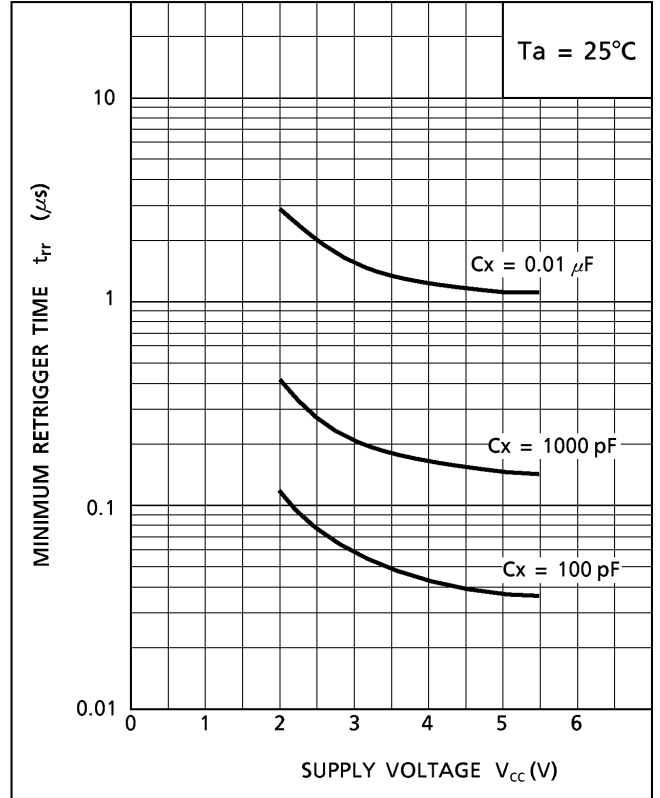
(Duty : %)

$t_{WOUT}-C_x$  CHARACTERISTICS (typ.)

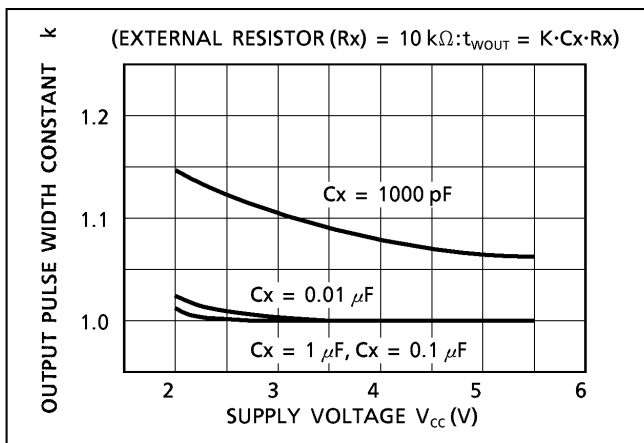


$t_{rr}-V_{CC}$  CHARACTERISTICS (TYP.)

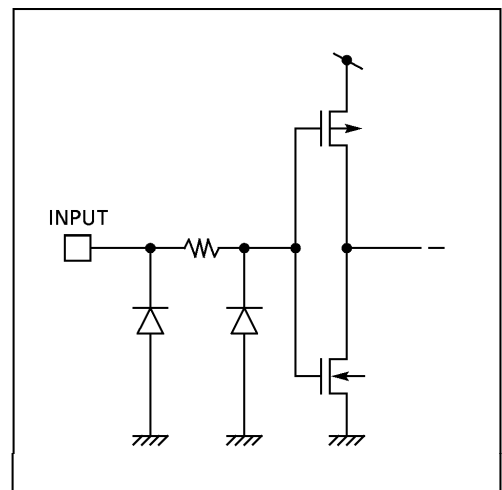
(TC74VHC123A)



OUTPUT PULSE WIDTH CONSTANT K-SUPPLY VOLTAGE (TYPICAL)

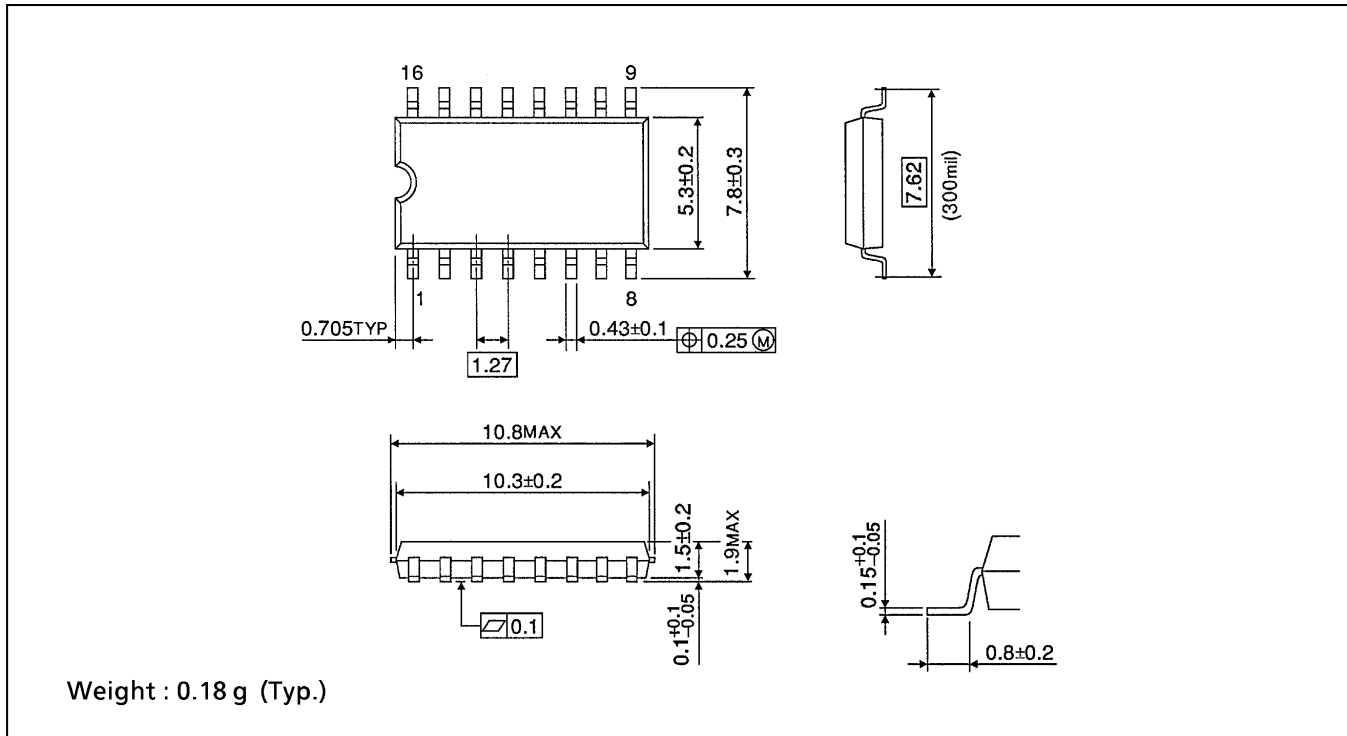


INPUT EQUIVALENT CIRCUIT



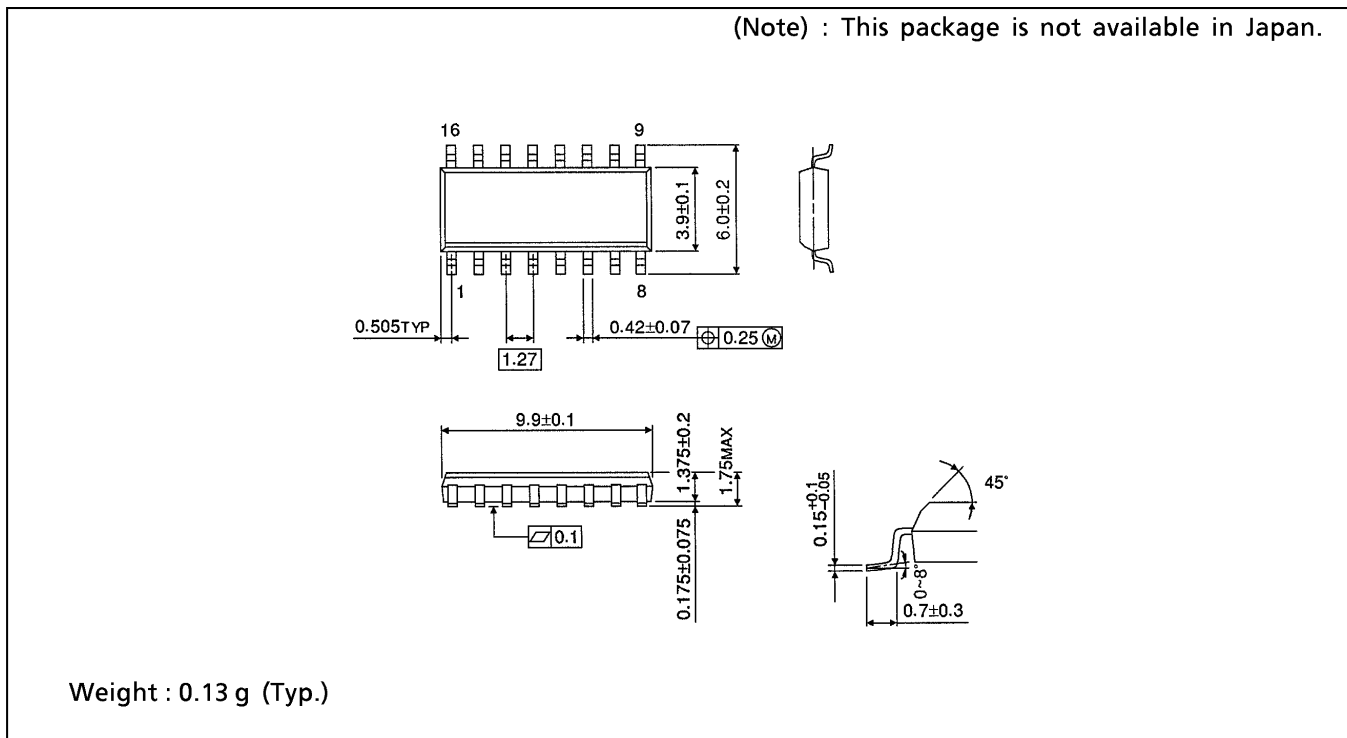
**SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)**

Unit in mm



**SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOP16-P-150-1.27)**

Unit in mm



**TSSOP 16PIN PACKAGE DIMENSIONS (TSSOP16-P-0044-0.65)**

Unit in mm

