

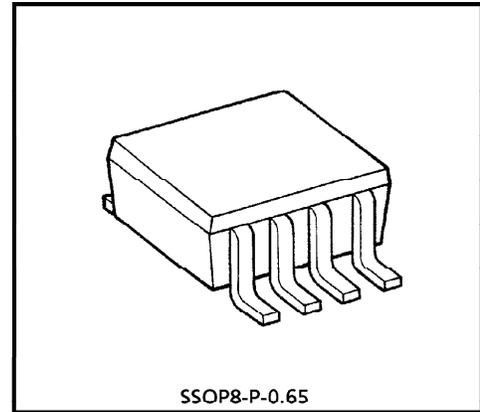
TC7W126FU

DUAL BUS BUFFER

The TC7W126FU is a high speed C²MOS DUAL BUS BUFFERS fabricated with silicon gate C²MOS technology. It achieve the high speed operation similar to equivalent LSTTL while maintaining the C²MOS low power dissipation.

The require 3-state control input G to be set low to place the output into the high impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight : 0.02g (Typ.)

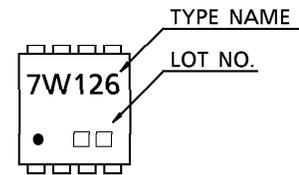
FEATURES

- High Speed $t_{pd} = 10ns$ (Typ.) at $V_{CC} = 5V$
- Low Power Dissipation $I_{CC} = 2\mu A$ (Max.) at $T_a = 25^\circ C$
- High Noise Immunity $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output Drive Capability 15 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL} = 6mA$ (Min.)
- Balanced Propagation Delays $t_{pLH} \cong t_{pHL}$
- Wide Operating Voltage Range ... $V_{CC} (opr) = 2\sim 6V$

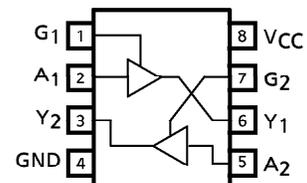
MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	- 0.5~7	V
DC Input Voltage	V_{IN}	- 0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	- 0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC} / Ground Current	I_{CC}	± 37.5	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	- 65~150	$^\circ C$
Lead Temperature (10s)	T_L	260	$^\circ C$

MARKING



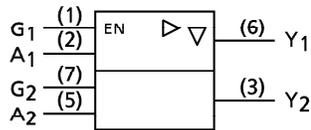
PIN ASSIGNMENT (TOP VIEW)



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LOGIC DIAGRAM



TRUTH TABLE

INPUTS		OUTPUTS
G	A	Y
L	X	Z
H	L	L
H	H	H

X : Don't Care
Z : High Impedance

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{CC}	2~6	V
Input Voltage	V _{IN}	0~V _{CC}	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	-40~85	°C
Input Rise and Fall Time	t _r , t _f	0~1000 (V _{CC} =2.0V) 0~500 (V _{CC} =4.5V) 0~400 (V _{CC} =6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT		
				V _{CC}	MIN.	TYP.	MAX.	MIN.		MAX.	
High-Level Input Voltage	V _{IH}	—	—	2.0	1.5	—	—	1.5	—	V	
				4.5	3.15	—	—	3.15	—		
				6.0	4.2	—	—	4.2	—		
Low-Level Input Voltage	V _{IL}	—	—	2.0	—	—	0.5	—	0.5	V	
				4.5	—	—	1.35	—	1.35		
				6.0	—	—	1.8	—	1.8		
High-Level Output Voltage	V _{OH}	—	V _{IN} = V _{IH}	I _{OH} = -20μA	2.0	1.9	2.0	—	1.9	—	V
					4.5	4.4	4.5	—	4.4	—	
					6.0	5.9	6.0	—	5.9	—	
					4.5	4.18	4.31	—	4.13	—	
Low-Level Output Voltage	V _{OL}	—	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μA	2.0	—	0.0	0.1	—	0.1	V
					4.5	—	0.0	0.1	—	0.1	
					6.0	—	0.0	0.1	—	0.1	
					4.5	—	0.17	0.26	—	0.33	
3-State Output Off-State Current	I _{OZ}	—	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	6.0	—	—	±0.5	—	±5.0	μA	
				6.0	—	—	±0.1	—	±1.0		
											6.0
6.0	—	—	±0.1	—	±1.0	μA					
Quiescent Supply Current	I _{CC}	—	V _{IN} = V _{CC} or GND	6.0	—	—	2.0	—	20.0	μA	

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITION			Ta = 25°C			Ta = -40~85°C		UNIT
				CL	VCC	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t _{TLH} t _{THL}	—	—	50	2.0	—	20	60	—	75	ns
					4.5	—	6	12	—	15	
					6.0	—	5	10	—	13	
Propagation Delay Time	t _{PLH} t _{pHL}	—	—	50	2.0	—	30	90	—	115	
					4.5	—	11	18	—	23	
					6.0	—	10	15	—	20	
				150	2.0	—	42	130	—	165	
					4.5	—	14	26	—	33	
					6.0	—	12	22	—	28	
Output Enable Time	t _{pZL} t _{pZH}	—	R _L = 1kΩ	50	2.0	—	30	90	—	115	
					4.5	—	11	18	—	23	
					6.0	—	10	15	—	20	
				150	2.0	—	42	130	—	165	
					4.5	—	14	26	—	33	
					6.0	—	12	22	—	28	
Output Disable Time	t _{pLZ} t _{pHZ}	—	R _L = 1kΩ	50	2.0	—	24	100	—	125	
					4.5	—	12	20	—	25	
					6.0	—	10	17	—	21	
Input Capacitance	C _{IN}	—	—	—	—	—	5	10	—	10	pF
Output Capacitance	C _{OUT}	—	—	—	—	—	10	—	—	—	
Power Dissipation Capacitance	C _{PD}	—	Note (1)	—	—	—	32	—	—	—	

Note (1) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
 Average operating current can be obtained by the equation :
 $I_{CC} (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2$ (per Gate)

