TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC90A53N,TC90A53F

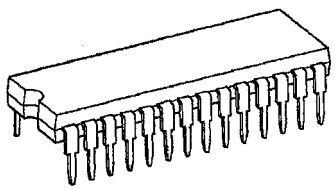
3-LINE DIGITAL Y / C SEPARATOR IC

TC90A53N / F is a 3-line digital Y / C separator IC which separates luminance signal Y and chroma signal C from composite video signals. Toshiba's logical comb filter realizes good Y / C separation at low cost.

FEATURES

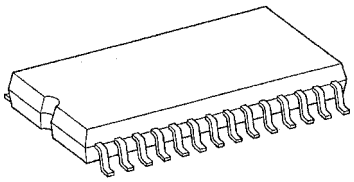
- TV format : NTSC (3.58)
- Dynamic comb filter
- Vertical edge enhancement circuit
- PLL 4 × multiplier circuit
- Internal 8-bit 4 fsc AD converter
- Internal 8-bit 4 fsc DA converter (2 ch)
- 1-line color dot interference reducer circuit
- Sync tip clamp circuit
- Internal 2H-line memory
- Color killer mode (Y / C separation off)
- Chroma signal C output wide band mode
- Package : SDIP 28-pin and SOP 28-pin
- 5 V single power supply

TC90A53N



SDIP28-P-400-1.78

TC90A53F

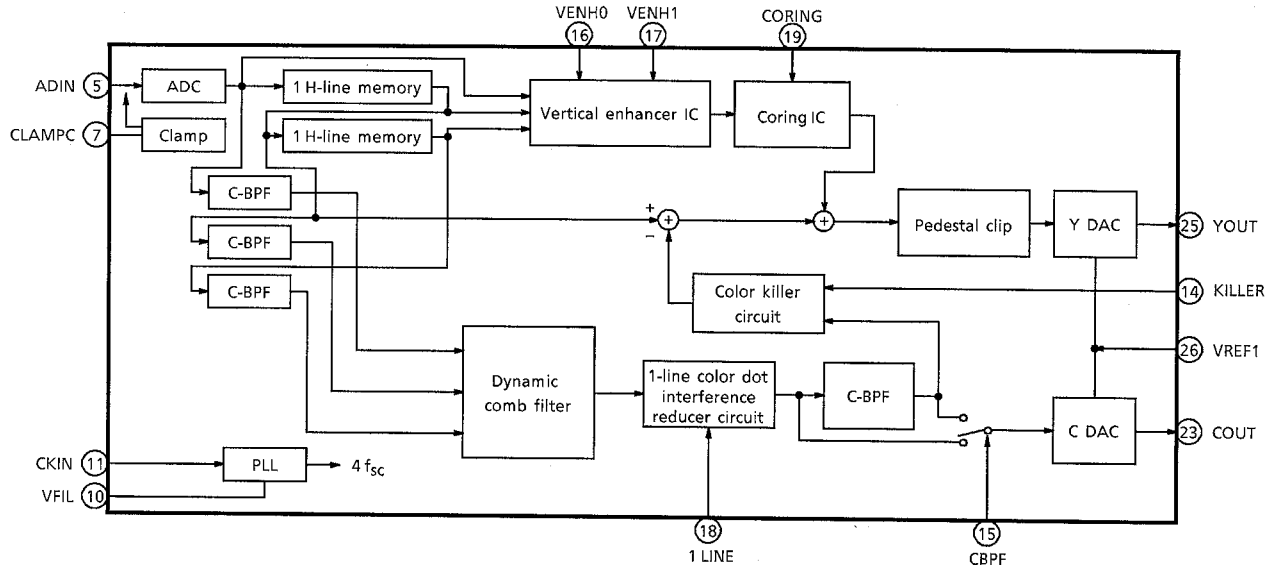


SOP28-P-450-1.27

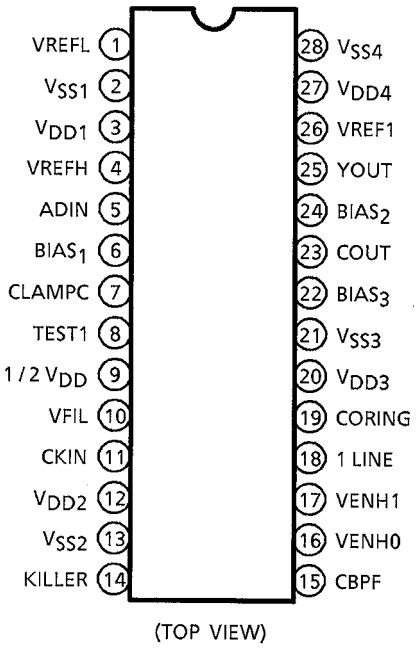
Weight:
SDIP28-P-400-1.78: 1.7 g (Typ.)
SOP28-P-450-1.27: 0.8 g (Typ.)

000707EBA1

BLOCK DIAGRAM



PIN CONNECTION



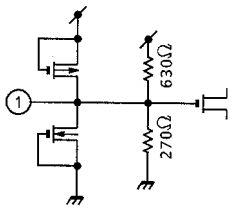
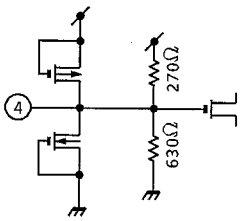
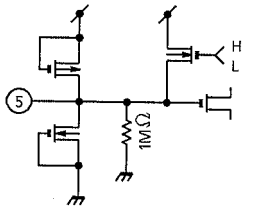
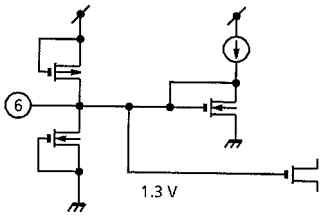
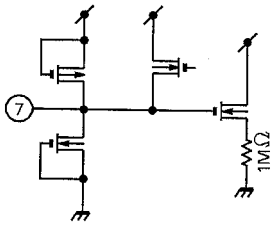
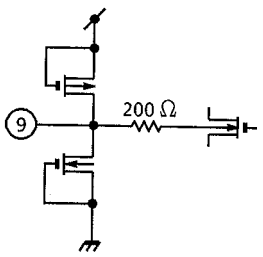
(TOP VIEW)

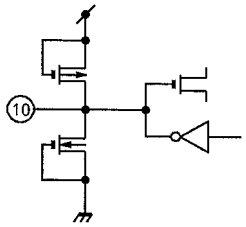
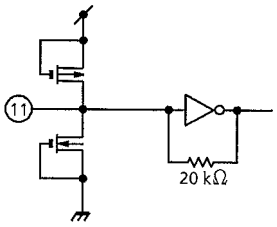
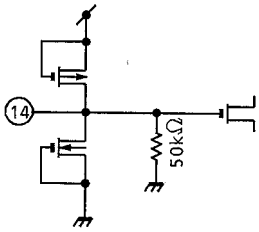
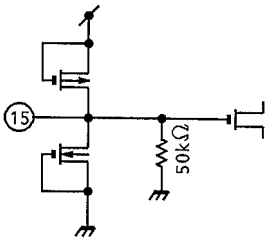
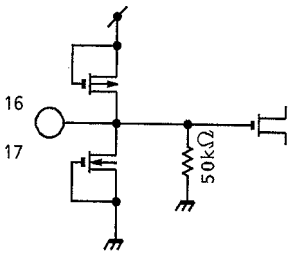
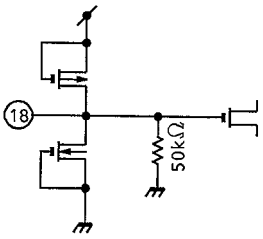
PIN FUNCTION

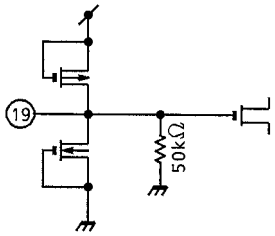
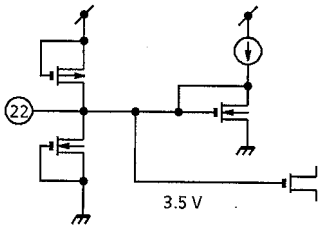
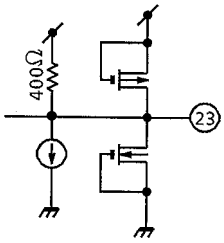
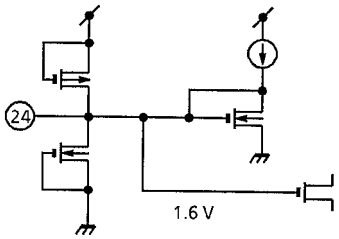
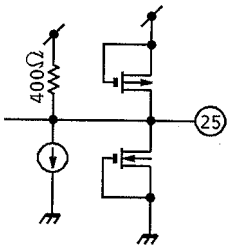
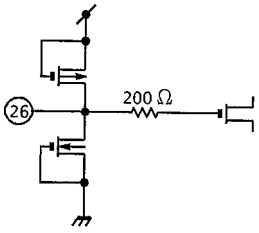
PIN No.	PIN NAME	FUNCTION	PIN No.	PIN NAME	FUNCTION
1	VREFL	ADC Bias	15	CBPF	L : C-BPF = Wide Band H : Narrow Band
2	V_{SS1}	ADC GND	16	VENH0	Sets Vertical Enhance Amount. (VENH0, VENH1) = (L, L) = Small (H, L) = Small (L, H) = Medium, (H, H) = Large
3	V_{DD1}	ADC Power Supply	17	VENH1	
4	VREFH	ADC Bias	18	1LINE	L : 1-line Color ON H : 1-line Color OFF
5	ADIN	Video Signal Input	19	CORING	L : Coring ON (2LSB) H : Coring OFF (0LSB)
6	$BIAS_1$	ADC Bias	20	V_{DD3}	Digital Power Supply
7	CLAMPC	Clamp Circuit Filter	21	V_{SS3}	Digital GND
8	TEST1	Test Pin	22	$BIAS_3$	DAC Bias
9	1 / 2 V_{DD}	Line Memory Bias	23	COUT	C Output
10	VFIL	VCO Filter	24	$BIAS_2$	DAC Bias
11	CKIN	Clock Input	25	YOUT	Y Output
12	V_{DD2}	PLL Power Supply	26	VREF1	DAC Bias
13	V_{SS2}	PLL GND	27	V_{DD4}	DAC Power Supply
14	KILLER	L : Color Mode H : Black And White Mode	28	V_{SS4}	DAC GND

(Note) : Pins 9 and 26 need external bias.

PIN FUNCTION

PIN No.	PIN NAME	FUNCTION	I / O	INTERFACE
1	V_{REFL}	ADC bias pin. Sets lower limit of range D for ADC. Fixed internally to 1.5 V (typ.). Connect 0.01 μF capacitor between this pin and GND.	—	
2	V_{SS1}	ADC GND	—	—
3	V_{DD1}	ADC power supply (+5 V)	—	—
4	V_{REFH}	ADC bias pin. Sets upper limit of range D for ADC. Fixed internally to 3.5 V (typ.). Connect 0.01 μF capacitor between this pin and GND.	—	
5	ADIN	Composite video signal input pin.	I	
6	BIAS1	ADC bias pin. Fixed internally to 1.3 V (typ.). Connect 0.01 μF capacitor between this pin and GND.	—	
7	CLAMPC	External filter used for Sync tip clamping the input composite video signal. Connect 510 kΩ and 4700 pF between this pin and GND.	—	
8	TEST	Test pin. Connect GND.	—	—
9	1 / 2 V_{DD}	Line-memory bias. Supply 1 / 2 V_{DD} by dividing digital power supply using a resistor. Connect 0.01 μF capacitor between this pin and GND.	I	

PIN No.	PIN NAME	FUNCTION	I / O	INTERFACE
10	V_{FIL}	Connect a VCO filter.	—	
11	CKIN	Inputs clock. First DC-cut f_{sc} clock in sync with color burst using a capacitor, then input the result.	I	
12	V_{DD2}	PLL power supply (+5 V)	—	—
13	V_{SS2}	PLL GND	—	—
14	KILLER	Selects color killer mode. L : Color mode H : Black and white mode (Y / C sep off)	I	
15	CBPF	Selects color signal horizontal band. L : Wide band (does not pass BPF) H : Narrow band (passes BPF)	I	
16 17	VENH0 VENH1	Select vertical enhance amount. VENH0 VENH1 L L : Small (+0.25) H L : Small (+0.25) L H : Medium (+0.75) H H : Large (+1.25)	I	
18	1 LINE	1-line color dot interference reducer ON / OFF L : 1-line color dot interference reducer ON H : 1-line color dot interference reducer OFF	I	

PIN No.	PIN NAME	FUNCTION	I / O	INTERFACE
19	CORING	Selects coring. L : Coring ON (2LSB) H : Coring OFF (0LSB)	I	
20	V_{DD3}	Digital power supply (+5 V)	—	—
21	V_{SS3}	Digital GND	—	—
22	BIAS3	DAC bias pin. Fixed internally to 3.5 V (typ.). Connect a 0.01 μF capacitor between this pin and GND.	—	
23	COUT	Outputs C signal.	O	
24	BIAS2	DAC bias pin. Fixed internally to 1.6 V (typ.). Connect a 0.01 μF capacitor between this pin and GND.	—	
25	YOUT	Outputs Y signal.	O	
26	V_{REF1}	DAC bias pin. Sets lower limit of range D for DAC. Supply power by dividing power for DAC using a resistor. Recommended value : 3.0 V	I	
27	V_{DD4}	DAC power supply (+5 V)	—	—
28	V_{SS4}	DAC GND	—	—

DESCRIPTION OF FUNCTIONS

(1) CLAMP (Input clamp)
Circuit used to Sync tip clamp composite signal.
Apply feedback clamp so that at Y / C separation, the minimum data value after A / D conversion is the internally-fixed level.

(2) ADC (A / D converter)
High-speed series-parallel 8-bit A / D converter (Dynamic Range: 2.0V).
Input composite video signal with amplitude of 1.5 V_{p-p} (sync to white 100%).

(3) 1 H memory
Line memory consisting of DRAM for 1 H delay. Two line memories configure a 3-line comb filter.
Because the system clock is 4 f_{sc} (14.3 MHz), 910 clocks / 1 H is set.

(4) VENH (Vertical enhancer circuit)
After coring (2LSB) the non-correlation component among the three lines of the luminance signal, this block enhances the vertical outline. The enhance amount can be selected from three settings : large (+1.25), medium (+0.75), and small (+0.25).
The vertical enhance amount is added to the luminous signal obtained by subtracting the color signal from the composite signal, then the luminous signal is output via the D / A converter. Note that if the luminous signal is lower than the pedestal level (internally-fixed value), the vertical enhance amount is not added to.

(5) BPF (Horizontal bandpass filter)
Uses f_{sc} as the center frequency. Filters the composite signal delayed by 0 H, 1 H, or 2 H and extracts the color signal.
The bandpass filter for outputting the color signal at a later stage can be switched on or off to select output of a narrow- or wide-band color signal.

(6) DCF (Vertical dynamic comb filter)
Vertical bandpass filter which extracts the color signal by detecting vertical non-correlation. Using Toshiba logic, determines the correlation among three lines. If no correlation, determines as the luminous signal and suppresses output of the color signal.

(7) 1-line color dot interference reducer circuit
Improves color dot interference on a screen where only 1 line has color so that the C signal is processed as the Y signal.
Extracts 1-line color dot component and the result is added to the output from the dynamic comb filter.

(8) RTIM (Clock / memory timing generator)
This block supplies × 4 f_{sc} (14.3 MHz) obtained using the VCO via a buffer to the blocks and generates the timing signal necessary for memory.

(9) PLL (× 4 clock generator)
Multiplies f_{sc} (3.58 MHz) by 4 and generates system clock 4 f_{sc} (14.3 MHz).

(10) DAC (D / A converter)
High-speed 8-bit D / A converter. The output amplitudes are : Y output of 1.5 V_{p-p} (typ.) and C output at burst level of 572 mV_{p-p} (typ.).

(11) Color killer circuit
When the input video signal is a monochrome image, this circuit enables effective use of the luminance signal information regardless of whether there is a burst signal. It does this by preventing the chroma signal output from the comb filter from being subtracted from the luminance signal.
While the VBI signal is active it is better not to use the comb function. Setting the KILLER pin to High at this time enables the use of character multiplex and other signals from the Y output unchanged.
But since Vertical edge enhancement does not become OFF, be careful when using with Vertical edge enhancement.

MODE LIST

PIN14 KILLER	PIN15 CBPF	PIN16 VENH0	PIN17 VENH1	PIN18 1 LINE	PIN19 CORING	MODE	OPERATION
L	—	—	—	—	—	Y / C separation ON	Color mode
H	—	—	—	—	—	Y / C separation OFF	Black and white mode (killer)
—	L	—	—	—	—	Color signal horizontal band, wide	Does not pass BPF for color signal output.
—	H	—	—	—	—	Color signal horizontal band, narrow	Passes BPF for color signal output.
—	—	L	L	—	—	Vertical enhance small	Enhance amount : (+0.25)
—	—	H	L	—	—	Vertical enhance small	Enhance amount : (+0.25)
—	—	L	H	—	—	Vertical enhance medium	Enhance amount : (+0.75)
—	—	H	H	—	—	Vertical enhance large	Enhance amount : (+1.25)
—	—	—	—	L	—	1-line color ON	1-line color dot interference reducer circuit ON
—	—	—	—	H	—	1-line color OFF	1-line color dot interference reducer circuit OFF
—	—	—	—	—	L	Coring ON	Coring circuit ON (2LSB)
—	—	—	—	—	H	Coring OFF	Coring circuit OFF (0LSB)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Power Supply Voltage		V_{DD}	V_{SS}~V_{SS} + 6.0	V
Input Voltage		V_{IN}	−0.3~V_{DD} + 0.3	V
Power Dissipation	TC90A53N	P_D (Note)	900	mW
	TC90A53F		600	
Storage Temperature		T_{stg}	−55~125	°C

(Note) : Ta = 75°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Power Supply Voltage	V_{DD}	—	4.75	5.0	5.25	V
Input Voltage	V_{IN}	—	0	—	V_{DD}	V
Operating Temperature	T_{opr}	—	−10	—	75	°C

ELECTRICAL CHARACTERISTICS
DC CHARACTERISTICS (Ta = 25°C, V_{DD} = 5 V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Voltage		V_{DD}	1	CLOCK = 3.579545 MHz 500 mV_{p-p} VREF1 = 3.0 V 1 / 2 V_{DD} = 2.5 V V_{IN} = No input (Note 1)	4.75	5.0	5.25	V
Operating Current		I_{DD}	1		40	60	80	mA
Output Voltage Level		Y_{OUT}	1		3.0	3.15	3.3	V
		C_{OUT}			3.9	4.0	4.1	
Pin Voltage Level		VREFL	1		1.4	1.5	1.6	V
		VREFH			3.4	3.5	3.6	
		ADIN			1.5	1.6	1.8	
		$BIAS_1$			0.8	1.4	2.4	
		$BIAS_2$			0.8	1.6	2.6	
		$BIAS_3$			2.4	3.4	4.4	
		CLAMPC			2.0	3.0	4.0	
		VFIL			0.9	1.9	2.9	
		CKIN			1.5	2.2	3.0	
Input Voltage	High Level	V_{IH}	1		4	—	—	V
	Low Level	V_{IL}	1		—	—	1	V
ADIN Pin Input Capacitance		C_{IN}	1		—	50	—	pF
Pull-Down Resistance		R_{PD}	1		25	50	100	kΩ

(Note 1) : Pins 9 and 26 need external bias.

AC CHARACTERISTICS

Y output (Ta = 25°C, V_{DD} = 5 V, clock frequency = 3.579545 MHz, 0.5 Vp-p, S1 = 2, VREF1 = 3.0 V)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN	TYP.	MAX	UNIT
Input Level	V_{IN}	1	0~140 IRE (Figure 2)		—	1.5	1.6	V_{p-p}
Low-Frequency Gain	GV	1	S2 = 2, S3 = 2, S4 = 1, S5 = 2 V_{IN} = 15.734 kHz, 1.5 V_{p-p} Vdc = 2.5 V		−0.5	0.0	0.5	dB
Frequency Characteristics	MTF1	1	S2 = 2, S3 = 2, S4 = 1, S5 = 2 V_{IN} = 1.5 V_{p-p} Vdc = 2.5 V	f2 / f1	−2.0	−1.2	−0.5	dB
	MTF2	1		f4 / f1	−3.0	−2.0	−1.5	
Comb Characteristics	Comb	1	S2 = 2, S3 = 2, S4 = 1, S5 = 2 V_{IN} = 1.5 V_{p-p} Vdc = 2.5 V	f2 / f3	40	45	—	dB
Linearity (Figure 1)	L_s	1	S2 = 1, S3 = 1, S4 = 1, S5 = 2 V_{IN} = 5-stage staircase waveform, 1.5V_{p-p} (Figure 2)	Y1 / Y2	35	40	43	%
	L_y	1		S / Y2	57	60	63	
Output Impedance	Z_o	1	S2 = 1, S3 = 1, S5 = 2 V_{IN} = 15.734 kHz, 1.5 V_{p-p} Vdc = 2.5 V $Zo = \frac{V1-V2}{V2} \times 400$ V1 : S4 = 1, V2 : S4 = 2		250	400	700	Ω
Clock Leakage (4 f_{sc} component)	L_{ck}	1	S2 = 2, S3 = 2, S4 = 1, S5 = 1 V_{IN} = No input		—	5.0	20	mV_{rms}
Clock Dominant Wave Leakag (f_{sc} component)	L_{sc}	1	S2 = 2, S3 = 2, S4 = 1, S5 = 1 V_{IN} = No input		—	1.0	2.0	mV_{rms}

C output (Ta = 25°C, V_{DD} = 5 V, clock frequency = 3.579545 MHz, 0.5 V_{p-p}, S1 = 1, VREF1 = 3.0 V)

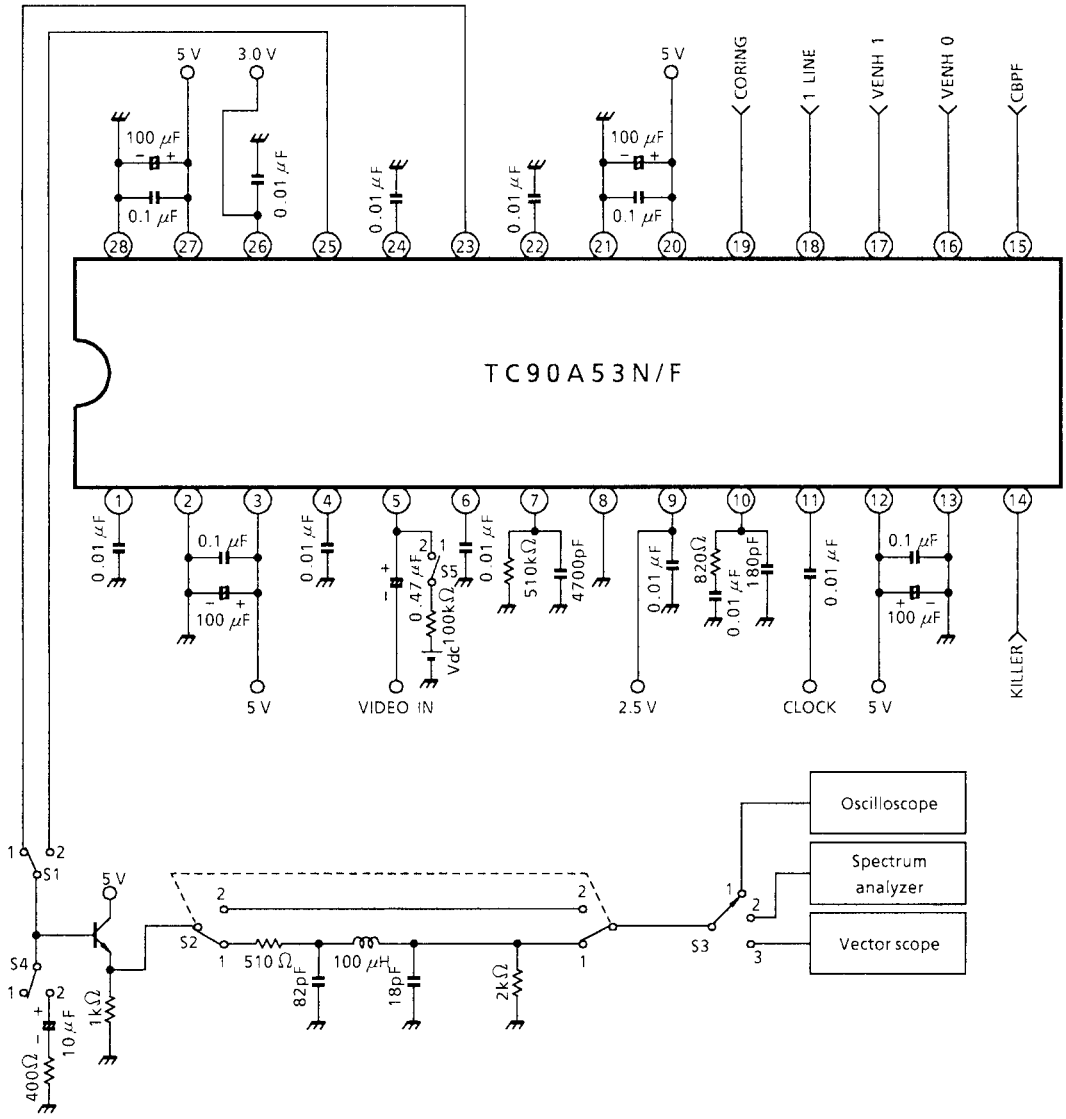
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
BPF Characteristics	Wide Band	BWCW	1	Amplitude difference between f_{sc} where S2 = 2, S3 = 2, S4 = 1, S5 = 2 and f_{sc} − 503496 Hz V_{IN} = 1.5 V_{p-p}, Vdc = 2.5 V	−0.5	−0.2	—	dB
	Narrow Band	BWCN	1	Amplitude difference between f_{sc} where S2 = 2, S3 = 2, S4 = 1, S5 = 2 and f_{sc} − 503496 Hz VIN = 1.5 V_{p-p}, Vdc = 2.5 V	−1.0	−0.5	—	
Gain		CV	1	S2 = 2, S3 = 2, S4 = 1, S5 = 1, V_{IN} = f_{sc}, 430 mV_{p-p}	−2	−0.9	−0.6	dB
Comb Characteristics		Comb	1	S2 = 2, S3 = 2, S4 = 1, S5 = 2, V_{IN} = 430 mV_{p-p}, Vdc = 2.5 V — f3 / f2	30	35	—	dB
Differential Gain		DG	1	S2 = 2, S3 = 3, S4 = 1, S5 = 1, V_{IN} = 5-stage staircase waveform, Y = 140 IRE = 1.5 V_{p-p}, C = 40 IRE (Figure 2), DG = (Comax−Comin) / Comax (Figure 3)	0	2	5	%
Differential Phase		DP	1		0	2	5	°
Output Impedance		Z_o	1	S2 = 2, S3 = 2, S5 = 2, V_{IN} = 15.734 kHz, 1.5 V_{p-p}, Vdc = 2.5 V, $Zo = \frac{V1-V2}{V2} \times 400$, V1:S4 = 1, V2:S4 = 2	250	400	700	Ω
Clock Leakage (4 f_{sc} Component)		L_{ck}	1	S2 = 2, S3 = 2, S4 = 1, S5 = 1, V_{IN} = No input	—	5.0	20	mV_{rms}
Clock Dominant Wave Leakag (f_{sc} Component)		L_{sc}	1	S2 = 2, S3 = 2, S4 = 1, S5 = 1, V_{IN} = No input	—	0.3	1.0	mV_{rms}

f1 = 15.734 kHz f2 = 3.587412 MHz f3 = 3.595279 MHz f4 = 4.783216 MHz

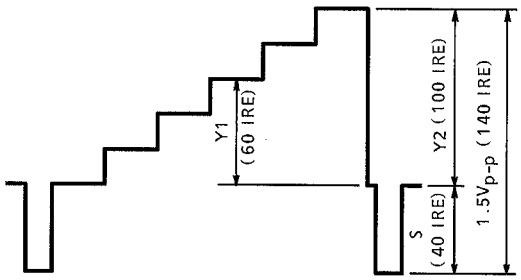
CLOCK PLL CIRCUIT CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Pull-in Frequency Range (4 f_{sc} Component)	f_{ck}	1	—	3.57	3.58	3.59	MHz
Input Amplitude (f_{sc} Component)	V_{ck}	1	—	0.4	—	—	V_{p-p}

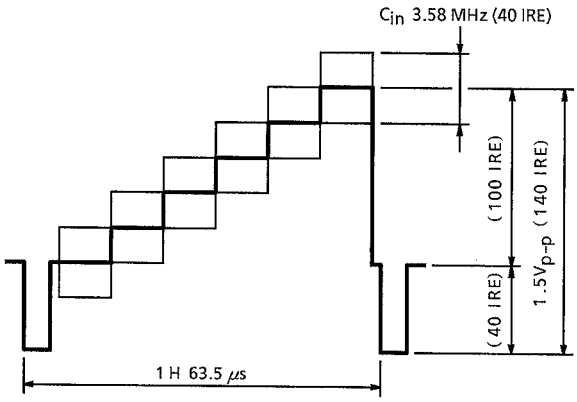
TEST CIRCUIT 1



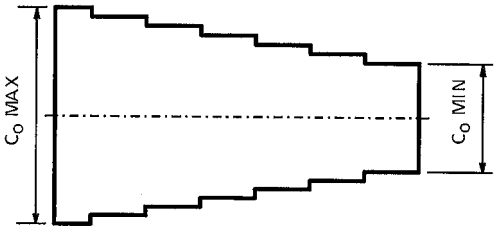
LINEARITY TEST (Figure 1)



5-STAGE STAIRCASE SIGNAL (Figure 2)

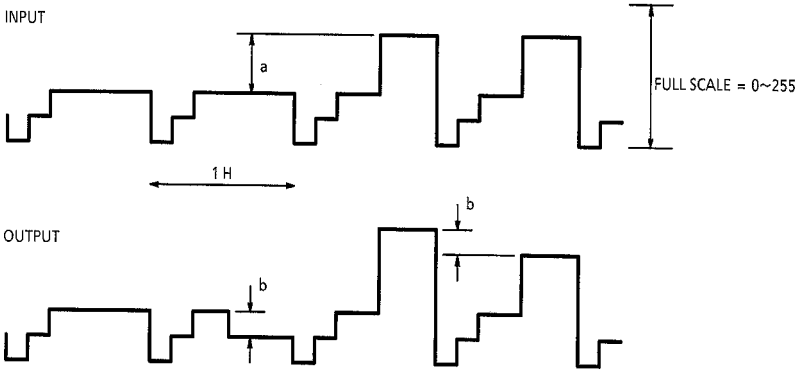


CHROMA DIFFERENTIAL GAIN (Figure 3)



REFERENCE DATA

(Figure 4-a) DEFINITION OF VERTICAL ENHANCE

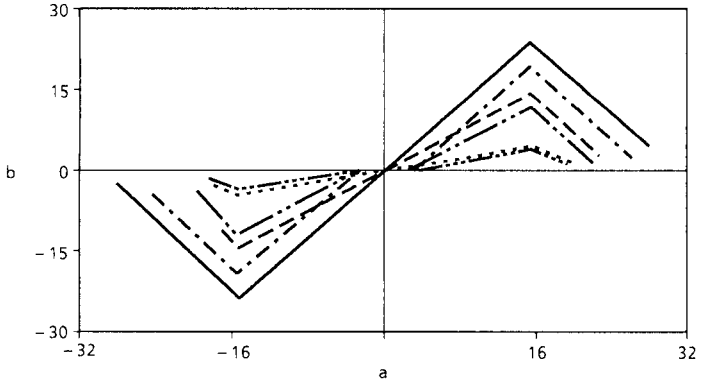


a : Vertical edge level

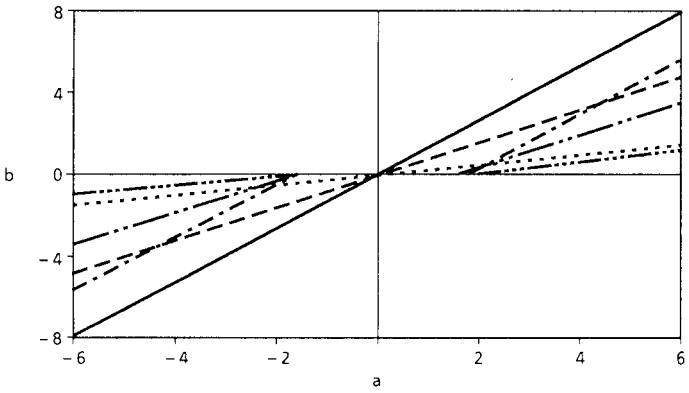
b : enhancement level

Note that output does not drop below the pedestal level (64 / 256) due to vertical outline enhance.

(Flgure 4-b) VERTICAL ENHANCE CHARACTERISTICS



(Figure 4-c) VERTICAL ENHANCE CHARACTERISTICS(ENLARGED)



Relation between difference (a) in luminous signal to be enhanced during 1 H and applied enhance amount (b) (see Figure 4-a)
Both a and b are digital amounts.

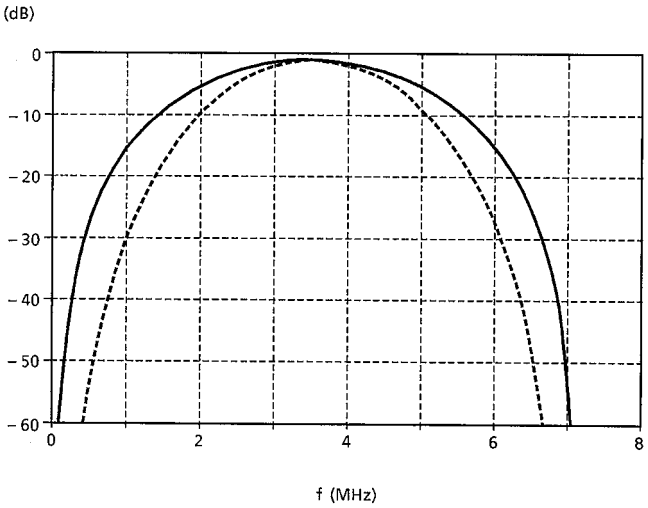
(A) Enhance amount : large (B) Medium

(C) Small (D) Enhance amount : large

(E) Medium (F) Small

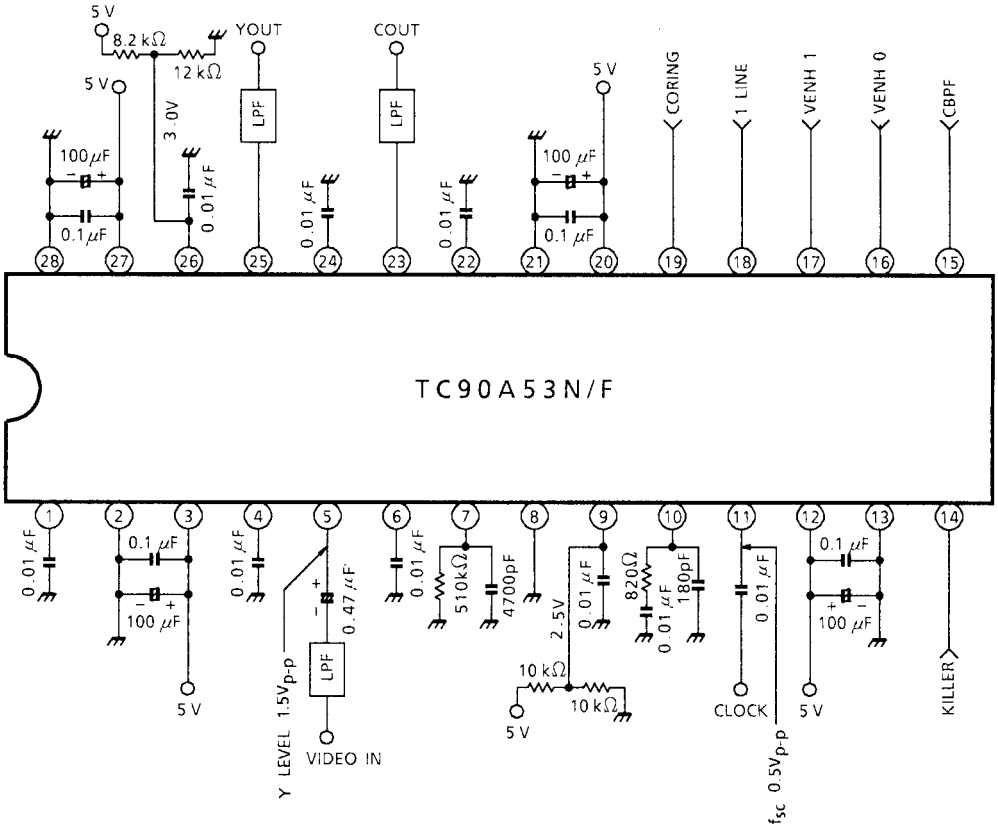
A, B, C : coring = OFF D, E, F : coring = ON

(Figure 5) FREQUENCY CHARACTERISTICS OF COLOR SIGNAL OUTPUT



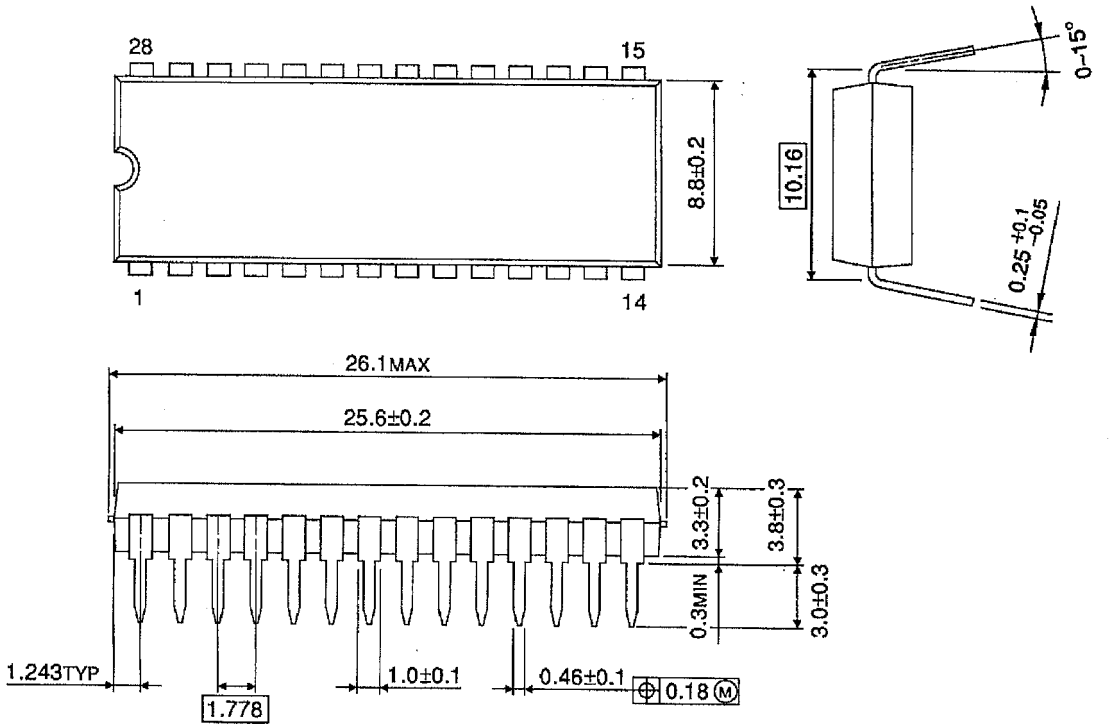
Wide band Narrow band

APPLICATION CIRCUIT



PACKAGE DIMENSIONS

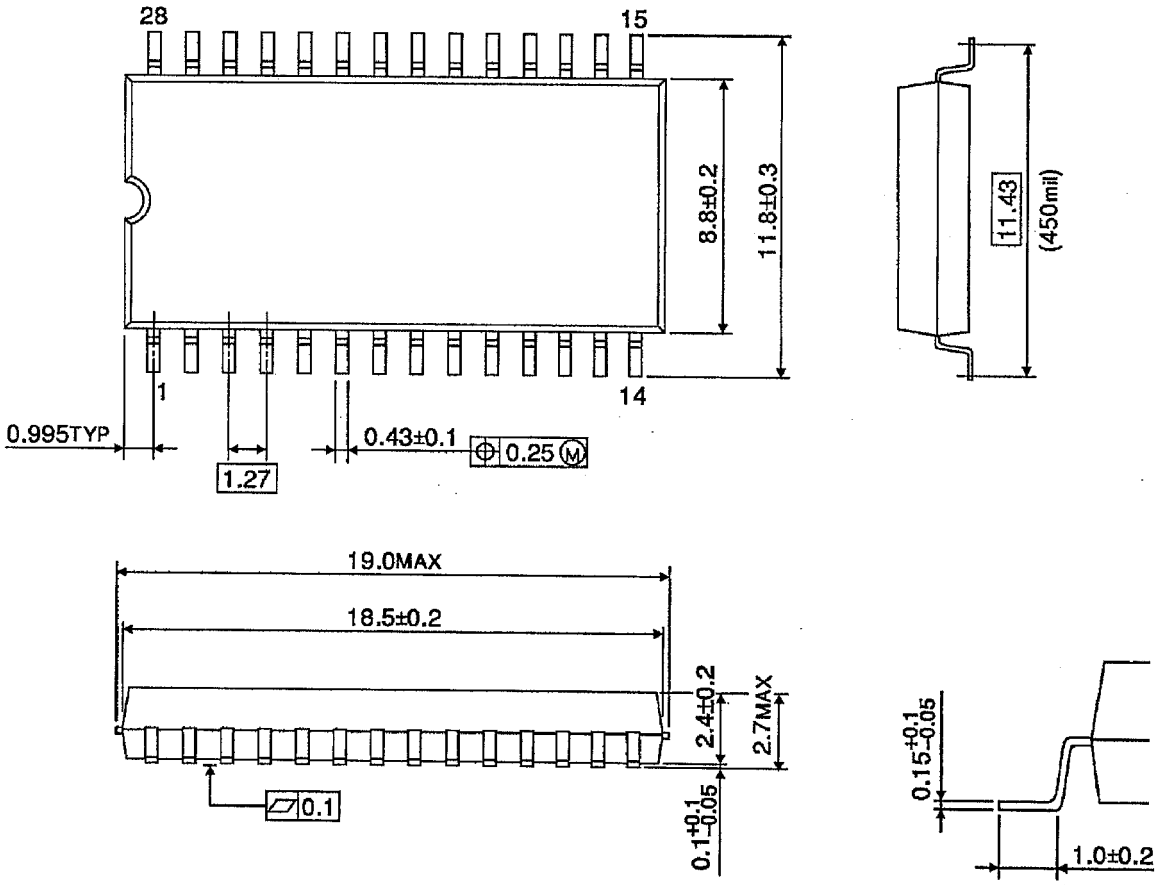
SDIP28-P-400-1.78 Unit : mm



Weight : 1.7 g (Typ.)

PACKAGE DIMENSIONS

SOP28-P-450-1.27 Unit : mm



Weight : 0.8 g (Typ.)