HIGH-VOLTAGE, AUTO-ZEROED OPERATIONAL AMPLIFIER

FEATURES

- **High-Voltage Operation ..... ±15V**
- **Low Offset Voltage ..... 10 µV Max**
- **Low Offset Voltage Drift ..... 0.2 µV/°C**
- **Low Input Bias Current ..... 200 pA Max**
- **High Open-Loop Voltage Gain ..... 140 dB**
- **Wide Common-Mode Voltage Range ..... –15V to +13V**
- **Low Input Voltage Noise (0.1 Hz to 1 Hz) ..... 0.2 μV_{p-p}**
- **Low Supply Current ..... 1 mA**
- **Single Supply Operation ..... 7V to 32V**
- **Pin Compatible With ICL7650**
- **Output Clamp Speeds Overload Recovery Time**

GENERAL DESCRIPTION

The TC915 is a high-voltage, high-performance CMOS, chopper-stabilized operational amplifier. It can operate from the same ±15V power supplies commonly used to power bipolar op amps, such as the OP07 and 741. Previous CMOS chopper-stabilized amplifiers, such as the TC7650, were limited to operating from ±7.5V power supplies.

The TC915's maximum V_{OS} specification is only 10 µV, almost a factor of 7 improvement over the industry-standard OP07E. The maximum V_{OS} drift of 0.1 µV/°C is 12 times less than the OP07E. Input bias and offset currents (both only 100 pA maximum) are factors of 20 improvements.

In addition to low initial offset errors, the nulling circuitry ensures excellent performance over time and temperature. Long-term drift, which results in periodic recalibration, is effectively eliminated. The nulling circuitry continues to operate over the full temperature range, whereas laser and "zener zap" trimming are only done at a single temperature. The result is a significant decrease in temperature-induced errors.

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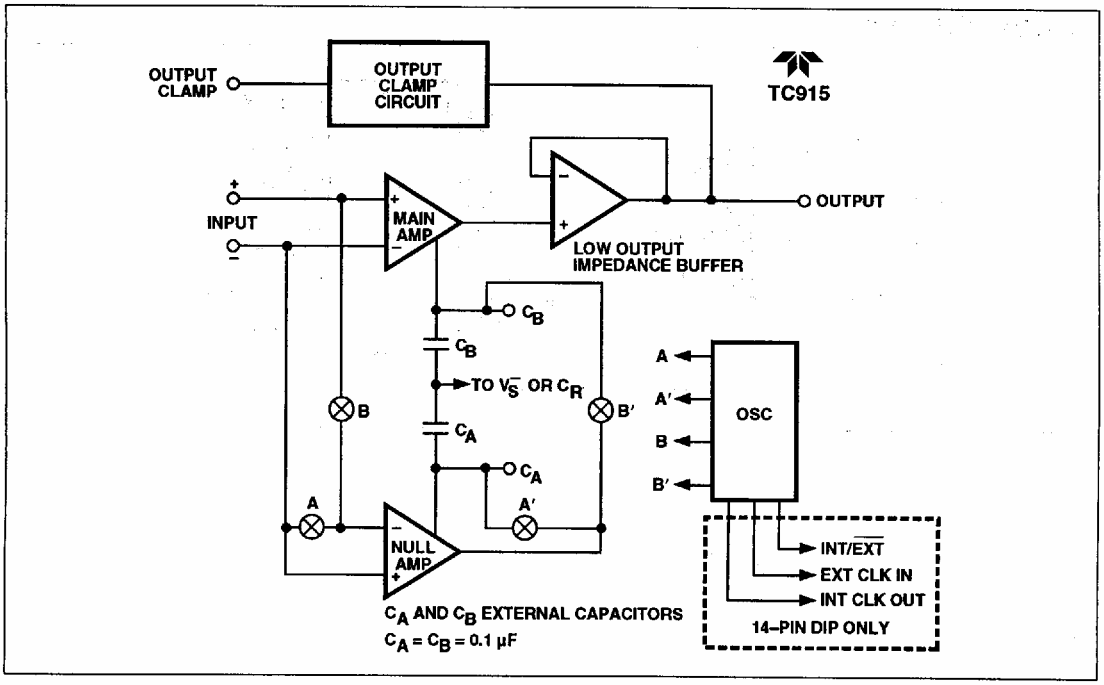
FUNCTIONAL DIAGRAM



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The TC915 operates from dual- or single-power supplies. Supply current is typically 1 mA with ±15V supplies. Single supply operation extends from +7V to +32V, and the input common-mode range extends to V_S^-. For battery operation, see the low-power TC900 data sheet.

The TC915's open-loop gain is 120 dB minimum. Unlike the TC7650, the TC915's gain is independent of load resistance. The low-impedance output will drive a 10 kΩ load to ±14V. An output clamp circuit is provided to minimize overload recovery time.

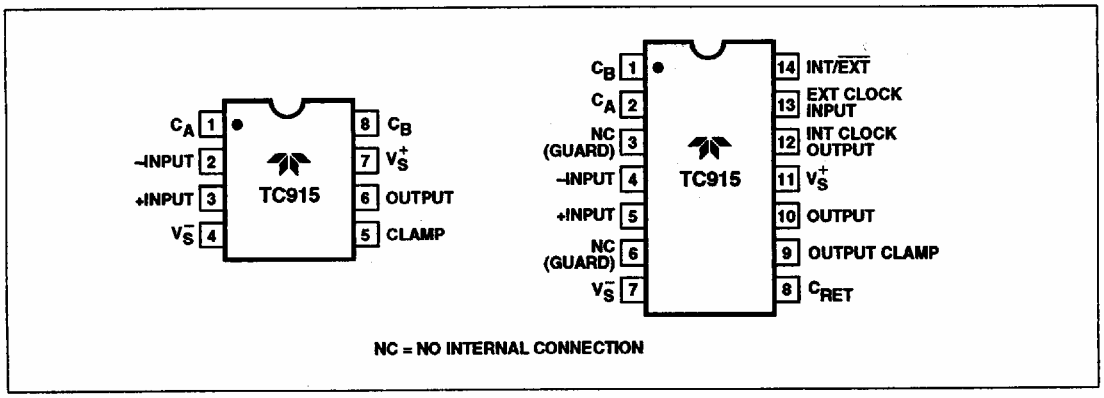
The TC915 uses two amplifiers to correct offset voltage errors. A main amplifier is always in the signal path, which prevents switching spikes at the output. A separate nulling amplifier alternately corrects its own V_{OS} error and then the main amplifier's V_{OS} error. Only two external capacitors are required to store the nulling error voltages. All active nulling circuitry, including switches and oscillators, are included on-chip.

TC915 does not require complicated processing and testing procedures associated with laser or "zener zap" V_{OS} trimming schemes. Simplified fabrication and high yields combine to make the TC915 one of the lowest-priced precision op amps available. It is available in 8-pin and 14-pin plastic or ceramic dual-in-line packages. Dice are available for hybrid applications.

ORDERING INFORMATION

Part No.	Package	Temperature Range	Max V_{OS}
TC915CPA	8-Pin Plastic DIP	0°C to +70°C	10 µV
TC915IJA	8-Pin CerDIP	–25°C to +85°C	10 µV
TC915MJA	8-Pin CerDIP	–55°C to +125°C	10 µV
TC915CPD	14-Pin Plastic DIP	0°C to +70°C	10 µV
TC915IJD	14-Pin CerDIP	–25°C to +85°C	10 µV
TC915MJD	14-Pin CerDIP	–55°C to +125°C	10 µV

PIN CONFIGURATION



NC = NO INTERNAL CONNECTION

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_S^+ to V_S^-) ..... +36V
Input Voltage ..... (V_S^+ +0.3V) to (V_S^- –0.3V)
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Current Into Any Pin ..... 10 mA
Operating Temperature Range
C Device ..... 0°C to +70°C
I Device ..... –25°C to +85°C
M Device ..... –55°C to +125°C

Package Power Dissipation (T_A = +25°C)
CerDIP ..... 500 mW
Plastic DIP ..... 375 mW

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_S = ±15V, T_A = +25°C, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{OS}	Input Offset Voltage		—	—	10	µV
TCV_{OS}	Input Offset Voltage vs Temperature Coefficient	0°C ≤ T_A ≤ +70°C	—	0.01	0.1	µV/°C
		–25°C ≤ T_A ≤ +85°C	—	—	0.3	µV/°C
I_B	Input Bias Current	T_A = +25°C	—	30	100	pA
		0°C ≤ T_A ≤ +70°C	—	—	—	pA
		–25°C ≤ T_A ≤ +85°C	—	—	10	pA
I_{OS}	Input Offset Current		—	50	100	pA
e_N	Input Voltage Noise	0.1 to 1 Hz, R_S ≤ 100Ω	—	0.2	—	μV_{P-P}
		0.1 to 10 Hz, R_S ≤ 100Ω	—	0.8	—	μV_{P-P}
CMRR	Common-Mode Rejection Ratio	V_S^- ≤ V_{CM} ≤ V_S^+–2	120	140	—	dB
CMVR	Common-Mode Voltage Range		V_S^-	—	V_S^+–2	V
A_{OL}	Open-Loop voltage Gain	R_L = 10 kΩ, V_O = ±10V	120	140	—	dB
V_{OUT}	Output Voltage Swing	R_L = 10 kΩ	V_S^-+1	—	V_S^+–1.2	V
BW	Closed-Loop Bandwidth	Closed-Loop Gain = +1	—	0.5	—	MHz
	Slew Rate	R_L = 10 kΩ, C_L = 50 pF	—	0.5	—	V/µs
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	120	140	—	dB
V_S	Supply Voltage Operating Range	(Note 1)	±3.5	—	±16	V
I_S	Quiescent Supply	V_S = ±15V	—	1	1.5	mA

NOTE: 1. Single supply operation: V_S^+ = +7V to +32V.

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Theory of Operation

Figure 1 shows the major elements of the TC915. There are two amplifiers: a main (signal) amplifier and a nulling amplifier. Both have offset-nulling capability. The main amplifier is always connected to the output. The nulling amplifier alternately samples and adjusts its own offset, then the offset of the main amplifier.

A two-phase operation nulls the main amplifier. During the first phase, the A pair of switches close, while the B switches open. The nulling amp's inputs are shorted and its output is fed back to the nulling input. Capacitor C_A charges to a voltage which will maintain the nulling amp in its nulled state.

During the second phase, the B switches close and the A switches open. The nulling amplifier's inputs now sample the offset voltage of the main amplifier. The nulling amplifier drives the main amplifier's nulling input to cancel the main amplifier's offset voltage. Capacitor C_B stores the nulling voltage of the main amplifier while the nulling amplifier is being nulled on the next cycle.

The TC915 design also incorporates an additional output buffer stage. The buffer provides a low-impedance output traditionally associated with bipolar op amps. Some CMOS chopper-stabilized amplifiers, such as the TC7650, have a high-output impedance which makes open-loop gain proportional to load resistance. The TC915's open-loop gain is not dependent on load resistance.

TC915

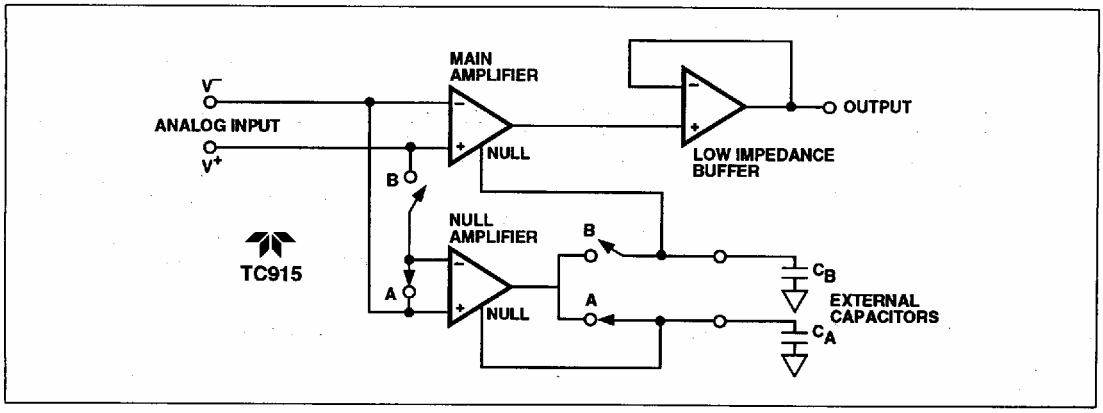

Figure 1 The TC915 Contains Nulling and Main Amplifiesr (Offset Correction Voltages Are Stored on Two External Capacitors)

Pin Compatibility

Since the TC915 operates from the same ±15V power supplies as bipolar op amps, upgrading existing circuits is simple. The bipolar op amp's nulling and compensation components are removed and the TC915's nulling capacitors are added.

On the 8-pin mini-DIP, the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open or used for offset potentiometer or compensation capacitor connections.

For OP05 and OP07 operational amplifiers, replacing the offset null potentiometer between pins 1 and 8 with two capacitors from the pins to V_S^- converts the OP05/07 pin configuration for TC915 operation. The 741 is easily upgraded by removing the nulling potentiometer between pin 4 and pins 1 and 5, then connecting capacitors from pin 4 to pins 1 and 8. For LM108 devices, the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pinouts are similarly modified by removing any circuit connections to pin 5. Pin 5 on the TC915 is the output clamp connection. Other operational amplifiers may use this pin as an offset or compensation point.

The minor modifications needed to retrofit a TC915 to existing sockets make prototyping and circuit verification straightforward.

Nulling Capacitors

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (pin 4) on the 8-pin packages and to capacitor return (C_{RET}, pin 8) on the 14-pin packages. The common connection should be made through a separate PC trace or wire, to avoid voltage drops. Internally, V_S^- is connected to C_{RET}.

C_A and C_B should be 0.1 µF film capacitors. Mylar capacitors are suitable.

Component Selection

The two required capacitors, C_A and C_B, have optimum values, depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 µF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock, if used. High-quality, film-type capacitors (such as Mylar) are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling at initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 µV.

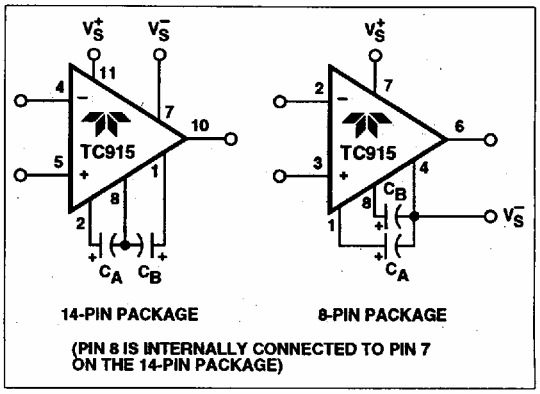

Figure 2 Nulling Capacitor Connection

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Clock Operation

The internal oscillator is set for a 1000 Hz nominal frequency on both the 8-pin and 14-pin DIPs. With the 14-pin device, the 250 Hz internal frequency is available at the INTERNAL CLOCK OUTPUT (pin 12). A 1000 Hz nominal signal will be present at the EXTERNAL CLOCK INPUT (pin 13) with INT/EXT high or open. This is the internal clock signal before a divide-by-four operation.

The 14-pin device can be driven by an external clock. The INT/EXT input (pin 14) has an internal pull-up and may be left open for internal clock operation. If an external clock is used, INT/EXT must be tied to V_S^- (pin 7) to disable the internal clock. The external clock signal is applied to the external clock input.

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ±6V, and between V_S^+ and V_S^+ –6V for higher supply voltages. When the external clock is generated by +5V logic, capacitive coupling to pin 13 (through a 0.1 µF capacitor) will provide adequate drive.

At low frequencies the external clock duty cycle is not critical, since an internal divide-by-four gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50% to 80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a stobe signal is connected at the external clock input, so that it is low during the time an overload signal is applied, neither capacitor will be charged. This function can be used to prevent input transients from overloading the nulling circuitry. Leakage currents at the capacitor pins are very low, minimizing offset voltage drift during strobe operation.

Output Clamp

Chopper-stabilized systems can show long overload recovery times. If the output is driven to either supply rail, output saturation occurs; the inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through the external-clamp connection, the TC915 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3, with typical inverting and noninverting circuit connections shown in Figures 4 and 5. For the clamp to be fully effective, the impedance across the clamp output should be >100 kΩ.

When the clamp is used, the clamp OFF leakage will add to input bias current. However, clamp leakage in the OFF state is typically only 1 pA.

Input Bias Current

The TC915 inputs are never disconnected from the main internal amplifier. The null amplifier samples the input offset voltage and corrects DC errors and drift by storing compensating voltages on external capacitors. However, the sampling causes charge transfer at the inputs.

The impulse current is not usually a problem, because the amount of charge transferred is very small. Care should be exercised, however, when replacing high-input bias current bipolar op amps. Conventional design practice is to cancel bias current by matching the input impedances (Figure 6a). The TC915 has an input bias current of only

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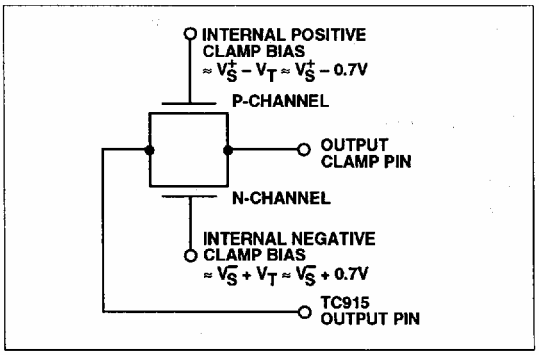

Figure 3 Internal Clamp Circuit

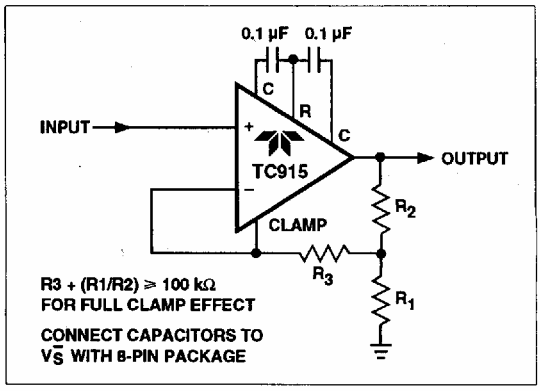

Figure 4 Noninverting Amplifier With Optional Clamp

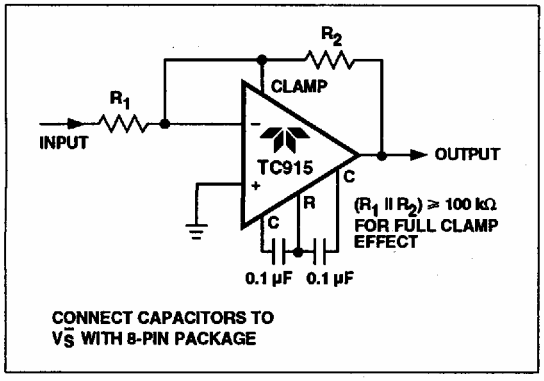

Figure 5 Inverting Amplifier With Optional Clamp

100 pA maximum, so the additional resistor is not necessary. In fact, including the resistor will make the charge injection current, passing through the impedance balancing resistor, appear as a noise source. When replacing an existing op amp with the TC915, either omit the resistor or bypass it to ground with a capacitor (Figure 6b).

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances, this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, voltages greater than 0.3V beyond the supply rails should not be applied to any pin. In general, the amplifier supplies must be established at the same time, or before, any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latch-up.

Static Protection

All device pins are static-protected. However, strong static fields and discharges should be avoided as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, educational materials, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. Two such companies are:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520

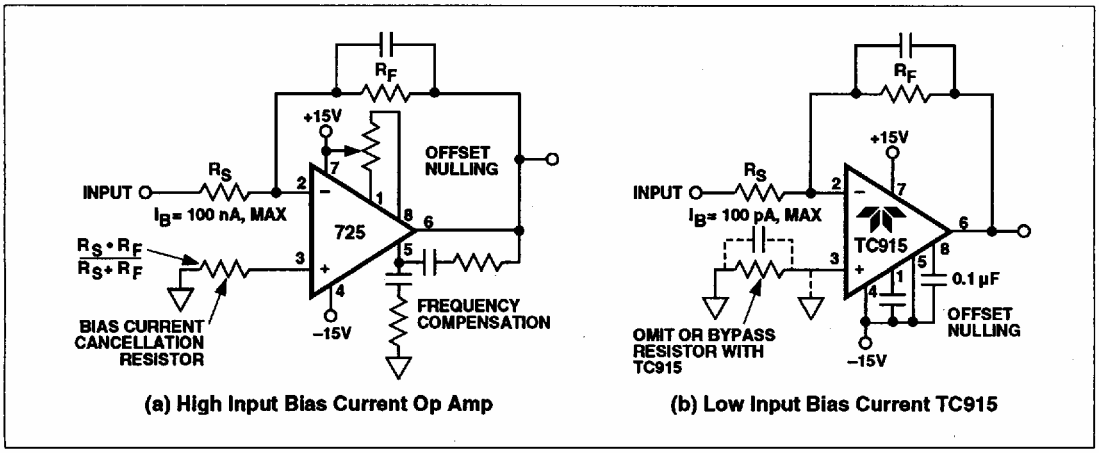

Figure 6 Input Bias Current Cancellation

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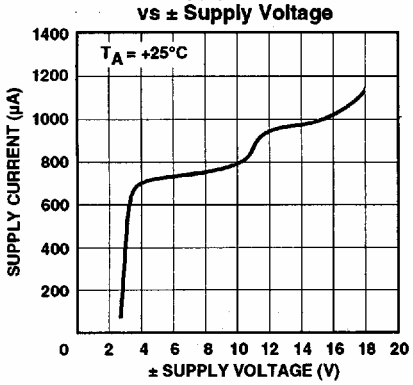
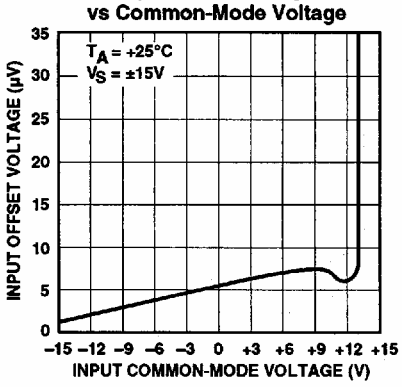
TYPICAL CHARACTERISTICS CURVES

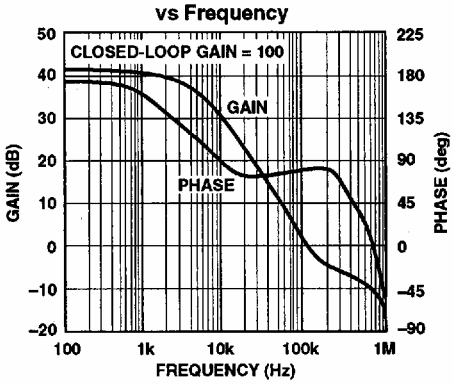
Supply Current vs ± Supply Voltage



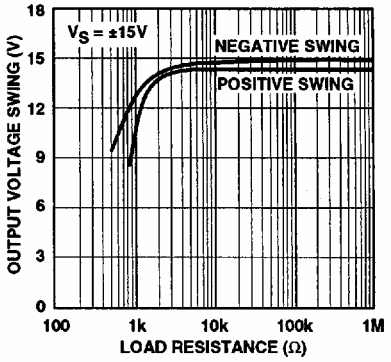
Input Offset Voltage vs Common-Mode Voltage



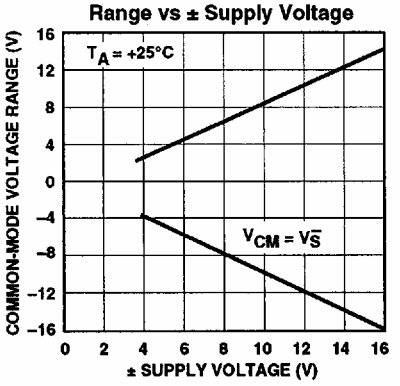
Gain and Phase vs Frequency



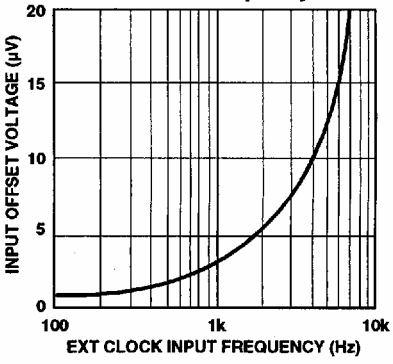
Output Voltage Swing vs Load Resistance



Input Common-Mode Voltage Range vs ± Supply Voltage



Input Offset Voltage vs Clock Frequency



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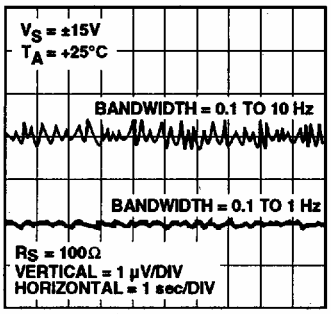
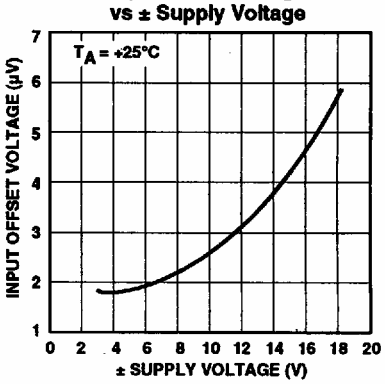
TC915

TYPICAL CHARACTERISTICS CURVES (Cont.)

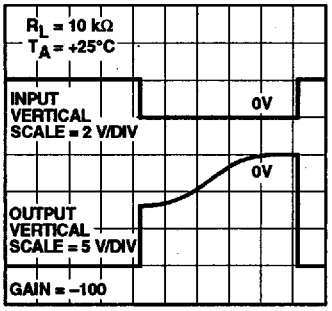
Input Voltage Noise



Input Offset Voltage vs ± Supply Voltage



Negative Overload Recovery Time



Positive Overload Recovery Time