

NOV 26 1990

Philips Components

Data sheet	
status	Preliminary specification
date of issue	October 1990

TDA4725T

SECAM-L chrominance processor for VHS video recorders

FEATURES

- Forced recording or playback mode input
- SECAM identification circuit
- One circuit for Bell and anti-Bell filter (1.07 MHz)
- Fully ESD protected
- Low power consumption (170 mW)
- 5 V supply.

GENERAL DESCRIPTION

The TDA4725 is a bipolar integrated circuit for chrominance processing of SECAM-L signals in SECAM-L or Multistandard VHS video recorders.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{18-24,26}	supply voltage		4.5	5.0	5.5	V
I ₁₈	supply current		-	34	-	mA
V _{25-24(p-p)} V _{21-24(p-p)}	chrominance input (peak-to-peak value)	record mode playback mode	- -	- 300	645 600	mV mV
V _{15-24(p-p)} V _{1-24(p-p)}	chrominance output (peak-to-peak value)	record mode playback mode	560 -	630 -	700 1000	mV mV
T _{amb}	operating ambient temperature range		0	-	70	°C
T _{stg}	storage temperature range		-25	-	+150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4725	28	DIL28	plastic	SOT117
TDA4725T	28	SO28	plastic	SOT136A

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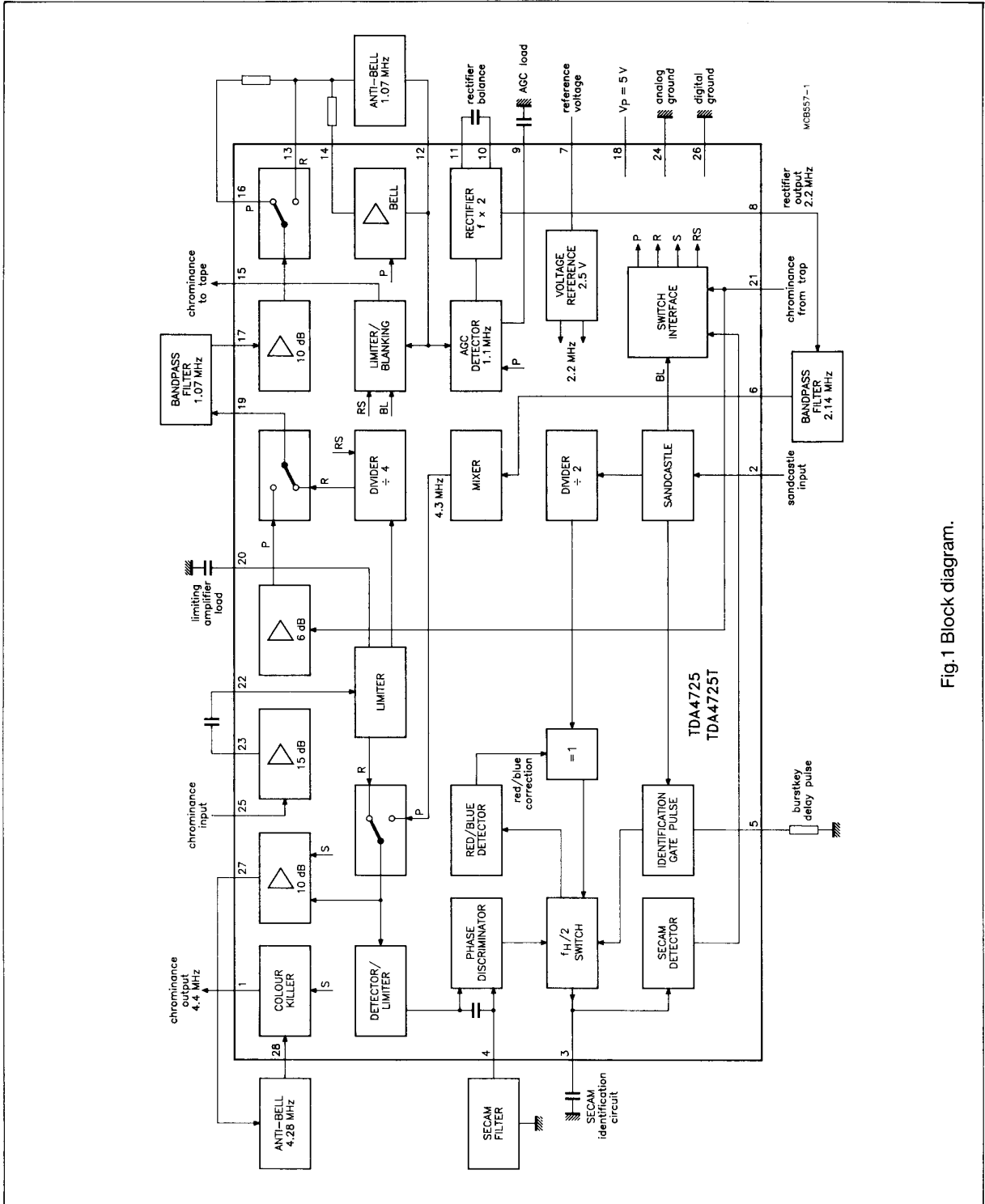


Fig.1 Block diagram.

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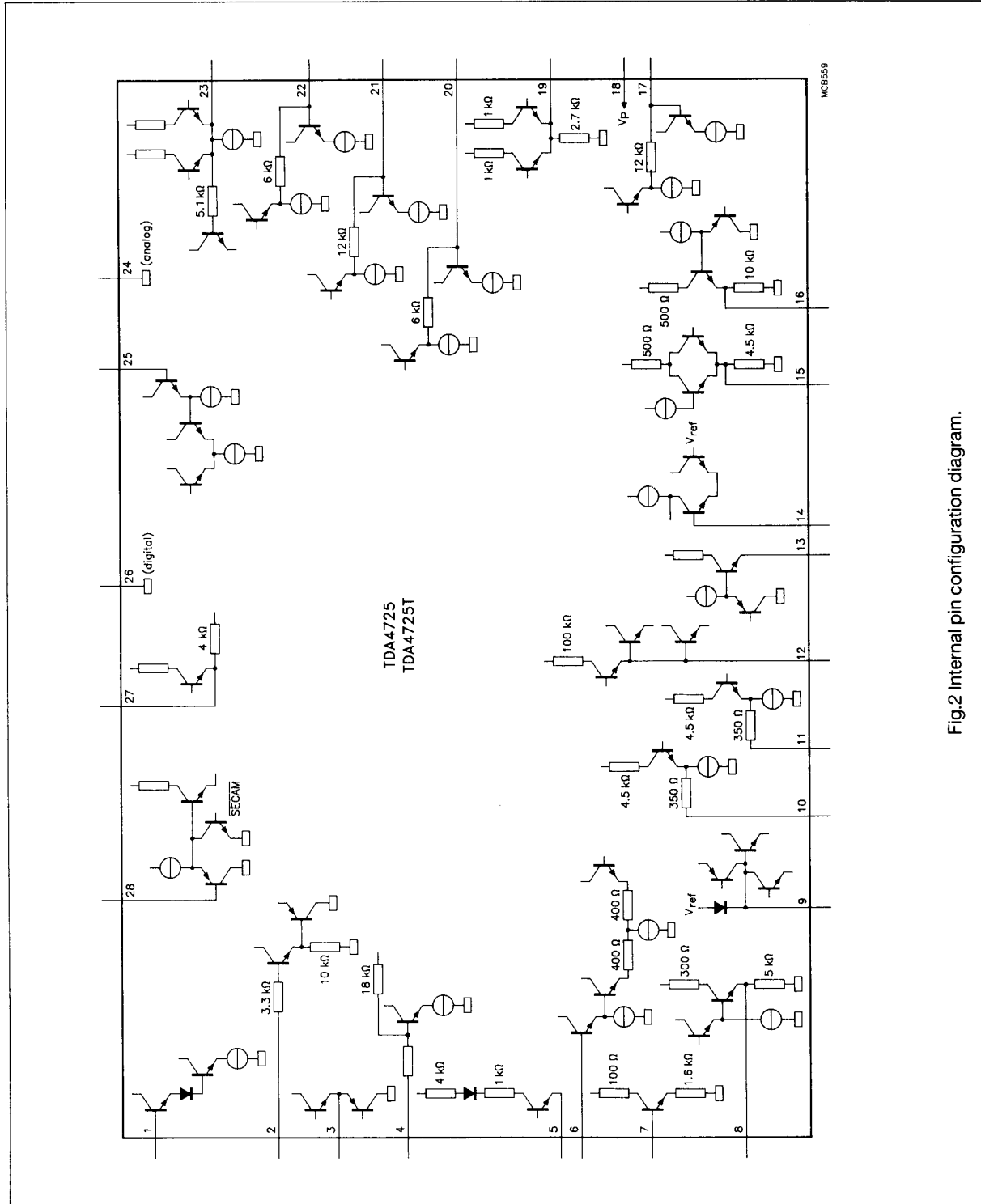


Fig.2 Internal pin configuration diagram.

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PINNING

PIN	DESCRIPTION
1	chrominance output (4.4 MHz)
2	sandcastle pulse or composite synchronization pulse input
3	connection for external load capacitor for the SECAM identification circuit
4	connection for external resonance circuit for the phase discriminator circuit
5	connection for resistor required for internal delay of burstkey pulse
6	mixer input
7	reference voltage
8	rectifier circuit output (2.2 MHz)
9	connection for external load capacitor for the AGC
10	connection for external balancing capacitor for the rectifier circuit
11	connection for external balancing capacitor for the rectifier circuit
12	output to passive anti-Bell circuit and limiter circuit (record mode) or output to Bell circuit and AGC circuit (playback mode)
13	10 dB amplifier output to anti-Bell circuit (record mode only)
14	virtual ground
15	chrominance signal output to tape (1.1 MHz)
16	output 10 dB amplifier and input active Bell filter (playback mode only)
17	input to 10 dB amplifier
18	power supply
19	divider output (record mode) or 6 dB amplifier output (playback mode)
20	external capacitor for limiting amplifier
21	chrominance signal input from tape
22	limiting amplifier input
23	15 dB amplifier output
24	analog ground
25	15 dB amplifier input
26	digital ground
27	10 dB amplifier output
28	input for colour killer circuit

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FUNCTIONAL DESCRIPTION (see Fig.1)

Recording mode

The chrominance signal is separated from the CVBS signal using an external bandpass filter and an external Bell circuit. The signal is applied to a divider ($\div 4$) via a 15 dB amplifier (pin 25) and limiter (pin 22). Once divided the 1.1 MHz signal is fed via an external bandpass filter (pins 17 and 19), an internal 10 dB amplifier (via pin 17), an external anti-Bell filter (pins 12 and 13) and a limiter/blanking stage. The blanking stage is active during the sandcastle pulses.

E to E mode

The 4.4 MHz signal is obtained from a tap in the limiter circuit and is applied to the chrominance output (pin 1) via the 10 dB amplifier, the external anti-Bell circuit and the colour-killer stage

Playback mode

The 1.1 MHz signal from the tape is applied, via a trap, to an internal 6 dB amplifier (via pin 21). Once amplified the signal is applied via an external bandpass filter and 10 dB amplifier to an operational amplifier (pins 12 and 14). The operational amplifier has an external anti-Bell circuit connected in its feedback path and, consequently, performs as a Bell circuit. From the operational amplifier the signal is applied to the AGC stage. The output signal from the AGC stage is applied to a rectifier where the frequency is doubled. Unwanted harmonics are removed by an external bandpass filter (pins 6 and 8) and the frequency is again doubled by the mixer at pin 6. The resultant 4.4 MHz signal is applied to the output stage at pin 1 via the 10 dB amplifier, the external anti-Bell circuit and the colour killer stage.

NOTE: The 1.07 MHz bandpass filter (pins 17 and 19) and the anti-Bell circuit (pins 12 and 13) are used in both the record and playback mode.

SECAM identification

For SECAM identification the input signal is phase shifted by an external resonant circuit [$f_0 = (f_b + f_r)/2$] and fed to the phase discriminator at pin 4. If the signal is a SECAM signal the positive- and negative-going pulses (with reference to the clamping voltage) are generated and rectified via the H/2 demodulator. The signal now consists of positive-going pulses only which are integrated via an external capacitor and applied to the SECAM detector at pin 3.

A non-SECAM signal (i.e. PAL) is removed from the phase discriminator having only positive-going pulses. After the H/2 demodulator, the signal has line-alternate positive- and negative-going pulses which compensate after integration.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Ratings System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage	-	6	V
P_{tot}	total power dissipation	-	250	mW
T_{stg}	storage temperature range	-25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C

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CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 1 V _{1-24(p-p)}	chrominance output signal (peak-to-peak value)	4.4 MHz sinusoidal signal	-	-	1	V
V ₁₋₂₄	DC level	SECAM signal non-SECAM signal	- -	V ₂₈₋₂₄ -	- 0.1	V V
R ₁₋₂₄	output resistance		-	V _t /I _e	-	Ω
α ₁	non-SECAM signal suppression		40	-	-	dB
Pin 2 V ₂₋₂₄	phase discriminator active voltage level		3.6	-	V _P	V
V ₂₋₂₄	blanking active voltage level		2.0	2.5	3.0	V
V ₂₋₂₄	blanking and phase discriminator inactive voltage level		-	-	1.5	V
R ₂₋₂₄	input resistance		20	-	-	kΩ
Pin 4 R ₄₋₂₄	input resistance		14	18	22	kΩ
Pin 5 R ₅₋₂₄	required resistance to ground	for 1 μs	-	26	-	kΩ
Pin 6 V ₆₋₂₄	input signal	2.2 MHz sinusoidal signal	-	300	-	mV
V ₆₋₂₄	DC level		-	V ₇₋₂₄	-	V
R ₆₋₇	input resistance		-	560	1200	Ω
C ₆₋₂₄	input capacitance		-	-	5	pF
Pin 7 V ₇₋₂₄	DC level		2.4	2.5	2.6	V
-I ₇	output current		-	-	5	mA
I ₇	input current		1	-	-	mA
R ₇₋₂₄	output resistance		-	-	1	Ω
Pin 8 V _{8-24(p-p)}	output signal voltage (peak-to-peak)	2.2 MHz	-	600	-	mV
V ₈₋₂₄	DC level		-	2.45	-	V
R ₈₋₂₄	output resistance		-	V _t /I _e	-	Ω
α ₈	1.1 MHz suppression		30	-	-	dB
α ₈	3.3 MHz suppression		30	-	-	dB
α ₈	4.4 MHz suppression		10	-	-	dB
Pin 12 V _{12-24(p-p)}	input signal (peak-to-peak value)	playback mode	24	-	320	mV
V ₁₂₋₂₄	DC level	record mode playback mode (closed loop)	- -	V ₁₃₋₂₄ V ₇₋₂₄	- -	V V
B	gain bandwidth (operational amplifier)	playback mode	40	-	-	MHz
R ₁₂₋₂₄	input resistance	record mode	100	-	-	kΩ
R ₁₂	open-loop output resistance		-	V _t /I _e	-	Ω

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SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 13 V ₁₃₋₂₄	DC level	record mode	-	V ₇₋₂₄ – 85 mV	-	V
G ₁₃₋₂₄	signal gain	record mode	-	10	-	dB
R _{t3-24}	output resistance	record mode	-	V _t /I _e	-	Ω
Pin 14 V ₁₄₋₂₄	DC level	playback mode	-	V ₇₋₂₄	-	V
Pin 15 V _{15-24(p-p)}	chrominance output (peak-to-peak value)		560	630	700	mV
V ₁₅₋₂₄	DC level		-	V ₇₋₂₄ – 80 mV	-	V
R ₁₅₋₂₄	output resistance		-	-	10	Ω
α ₁₅	playback suppression		30	-	-	dB
α ₁₅	non-SECAM suppression		40	-	-	dB
α ₁₅	blanking suppression		30	-	-	dB
Pin 16 V ₁₆₋₂₄	DC level	playback mode	-	V ₇₋₂₄ – 54 mV	-	V
G ₁₆₋₁₇	signal gain	playback mode	-	10	-	dB
R ₁₆₋₂₄	input resistance	record mode	-	10	-	kΩ
R ₁₆₋₂₄	output resistance	playback mode	-	V _t /I _e	-	Ω
Pin 17 V _{17-24(p-p)}	input signal (peak-to-peak value)		-	400	-	mV
V ₁₇₋₂₄	DC level		-	V ₇₋₂₄ – 30 mV	-	V
R ₁₇₋₂₄	input resistance		8	12	16	kΩ
C ₁₇₋₂₄	input capacitance		-	-	5	pF
Pin 19 V ₁₉₋₂₄	DC level	record mode playback mode	- -	1.82 1.7	- -	V V
V _{19-24(p-p)}	AC level (peak-to-peak value)	sinusoidal	-	800	-	mV
		block	-	621	-	mV
G ₁₉₋₂₄	signal gain	playback mode	-	6	-	dB
R ₁₉₋₂₄	output resistance		-	V _t /I _e	-	Ω
Pin 21 V _{21-24(p-p)}	input signal (peak-to-peak)	playback mode	-	300	600	mV
V ₂₁₋₂₄	DC level		-	3.25	-	V
V ₂₁₋₂₄	record mode active voltage level		-	-	1.5	V
V ₂₁₋₂₄	playback mode active voltage level		2.2	-	-	V
R ₂₁₋₂₄	input resistance		8	12	16	kΩ
C ₂₁₋₂₄	input capacitance		-	-	5	pF
Pin 25 V _{25-24(p-p)}	input signal (peak-to-peak value)		-	-	645	mV
V ₂₅₋₂₄	DC level		-	V ₇₋₂₄	-	V
R ₂₅₋₂₄	input resistance		100	-	-	kΩ
C ₂₅₋₂₄	input capacitance		-	-	5	pF

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SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Pin 27 R ₂₇₋₂₄	output resistance		-	-	10	Ω
RECORD MODE V _{27-24(p-p)}	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V ₂₂ = 600 mV (p-p)	-	1175	-	mV
V _{27-24(p-p)}	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V ₂₂ = 300 mV (p-p)	-	1110	-	mV
V _{27-24(p-p)}	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal; V ₂₂ = 30 mV(p-p)	-	272	-	mV
V ₂₇₋₂₄	DC level		-	1.65	-	V
PLAYBACK MODE V _{27-24(p-p)}	output signal (peak-to-peak value)	4.4 MHz sinusoidal signal	-	1175	-	mV
V ₂₇₋₂₄	DC level		-	3	-	V
G ₂₇₋₆	signal gain		-	12	-	dB
α_{27}	2.2 MHz suppression		23	-	-	dB
α_{27}	6.6 MHz suppression		30	-	-	dB
α_{27}	8.8 MHz suppression		10	-	-	dB
Pin 28 V _{28-24(p-p)}	input signal (peak-to-peak)		-	-	1000	mV
V ₂₈₋₂₄	DC level		-	V ₂₇₋₂₄	-	V
R ₂₈₋₂₄	input resistance		100	-	-	k Ω
C ₂₈₋₂₄	input capacitance		-	-	5	pF

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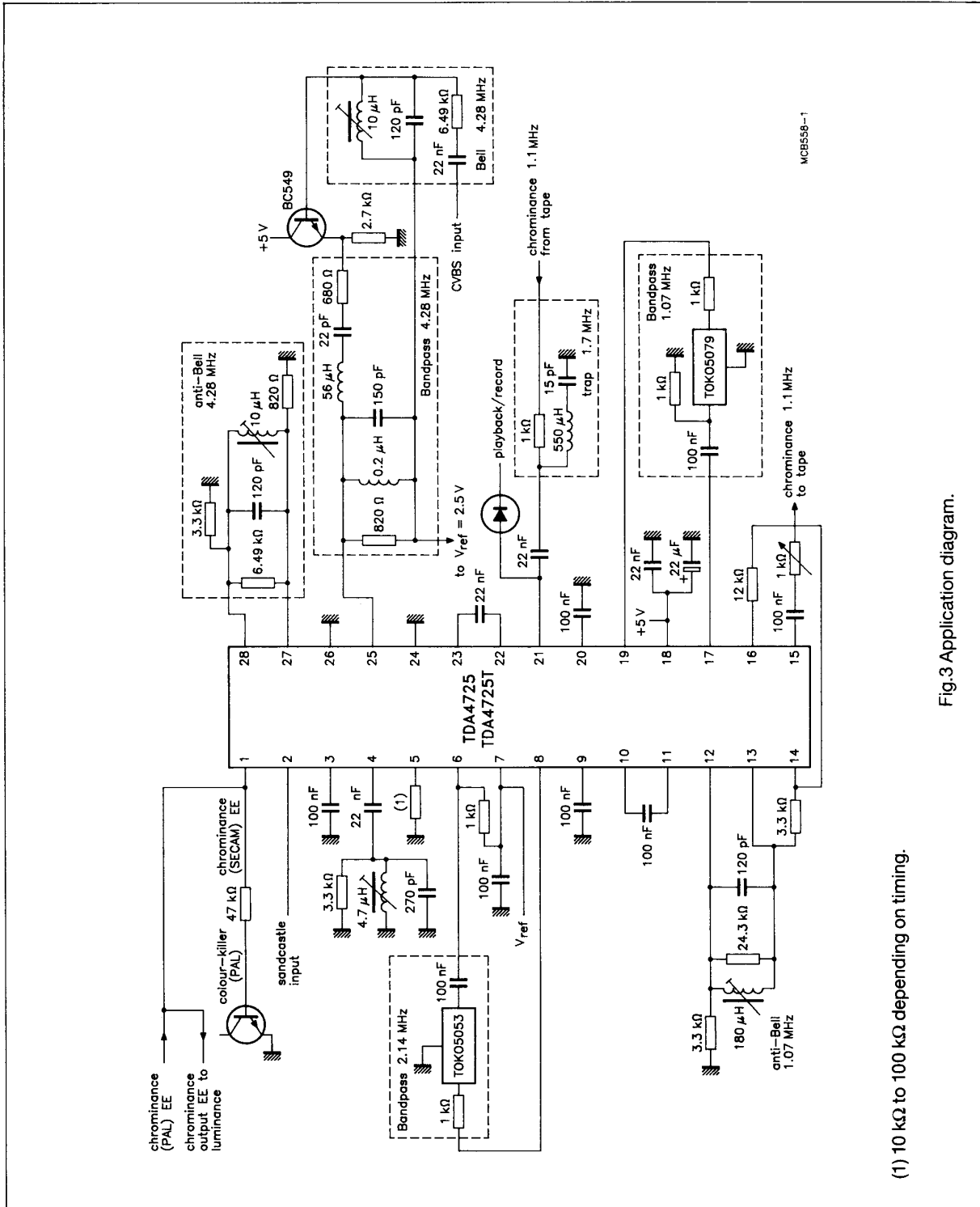


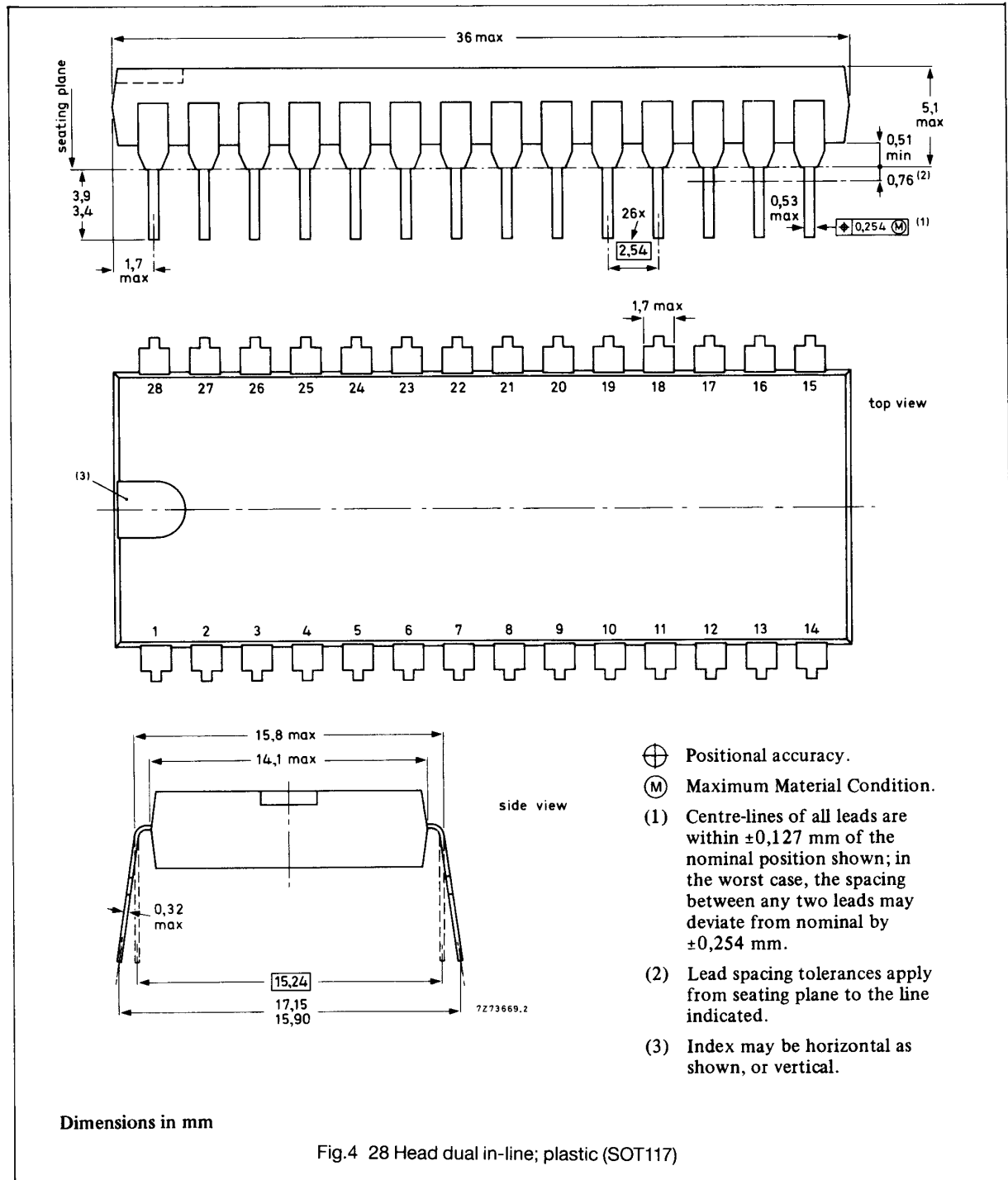
Fig.3 Application diagram.

(1) 10 kΩ to 100 kΩ depending on timing.

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PACKAGE OUTLINES



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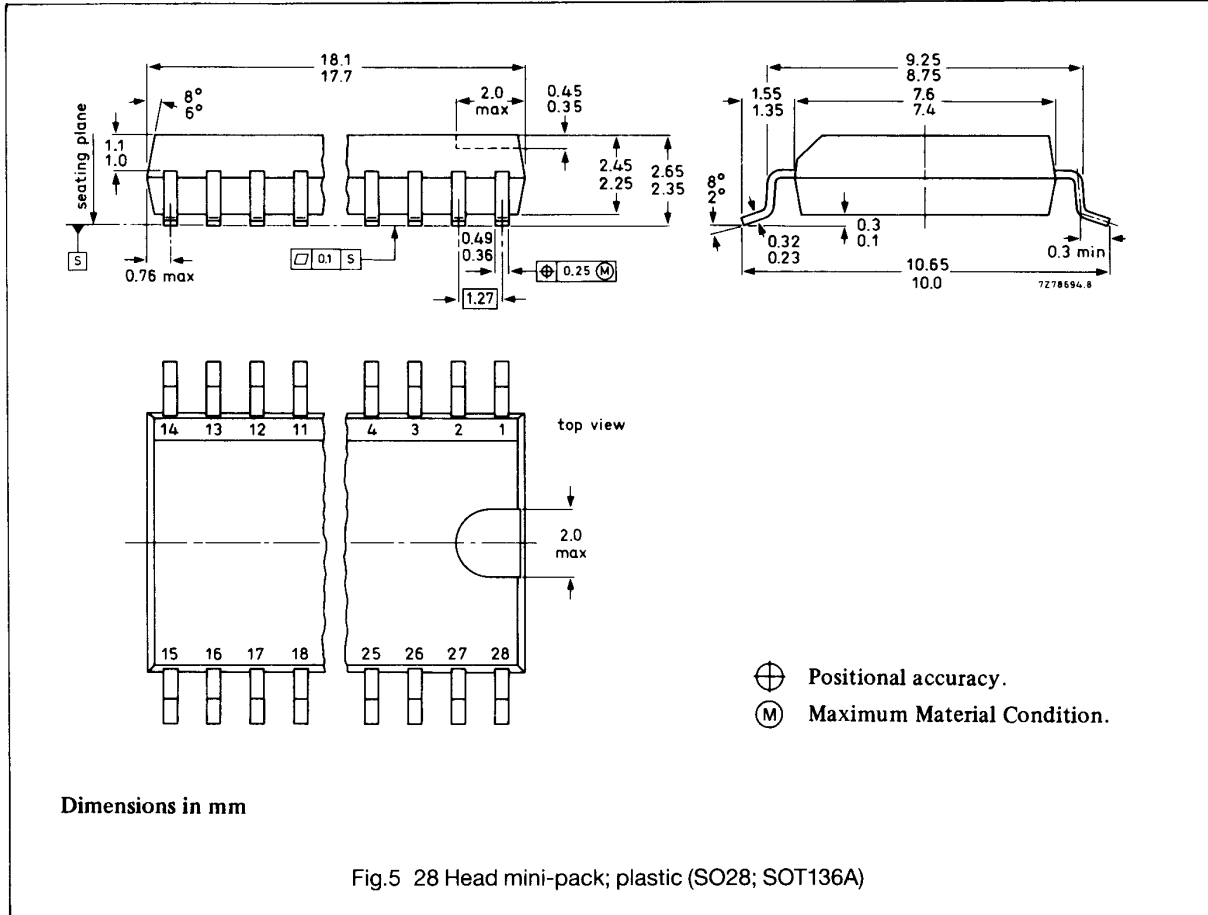


Fig.5 28 Head mini-pack; plastic (SO28; SOT136A)

**SECAM-L chrominance processor for VHS
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TDA4725T**SOLDERING PLASTIC MINI-
PACKS****By hand-held soldering iron or
pulse-heated solder tool**

Fix the component by first soldering two, diagonally opposite, end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared,

and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry the paste and evaporate the binding agent.

Pre-heating duration: 45 minutes at 45 °C.

Repairing soldered joints

The same precautions and limits apply as in (1) above.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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